



FRONTGRADE

WHITE PAPER

**UT8QNF8M8 NOR FLASH
TID Extension**

1/24/2025

Version #: 1.0.1

Table 1: Cross Reference of Applicable Products

Product Name	Manufacturer Part Number	SMD #	Device Type	Internal Pic Number
64Mb NOR FLASH	UT8QNF8M8	5962-12204	01 - 04	RQ10

Overview

The UT8QNF8M8 64Mbit NOR Flash Memory specifies a maximum total ionizing dose of 50 krad(Si) in an operational environment where the device is unpowered for 90% of its mission life. The application consistent with the NOR Flash being unpowered for the greater part of its design life is when the device is implemented as boot load memory. As the boot loader, the device is typically only accessed during system power up or processor reset. During the time after the boot code has been read by the processor, the device is idle and therefore may be powered down and isolated. A good method for the power down and isolation functionality is to implement the NOR Flash interface using a combination of Bus Switch products.

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Scope

This document outlines a design example for achieving 50 krad(Si) TID implementation of the Frontgrade Semiconductor Solutions UT8QNF8M8 64Mb NOR Flash memory device. The approach implements Frontgrade Semiconductor Solutions Bus Switches, that when disabled isolate the power and I/O signals to and from the NOR Flash.

Applicable Device(s)

- UT8QNF8M8 64Mb NOR Flash
 - <https://frontgrade.com/IsoveraURL/datasheets/UT8QNF8M8.pdf>

Referenced Documents

- UT54BS16245 16 bit Bus Switch
 - <https://frontgrade.com/IsoveraURL/datasheets/UT54BS16245.pdf>
- UT54BS32245 32 bit Bus Switch
 - <https://frontgrade.com/IsoveraURL/datasheets/UT54BS32245.pdf>
- UT04VS33P 4 channel Voltage Supervisor
 - <https://frontgrade.com/IsoveraURL/datasheets/vSupUT04VS33P.pdf>
- UT700 LEON 3FT Processor
 - <https://frontgrade.com/IsoveraURL/datasheets/leon/UT700LEON3FTDatasheet.pdf>
- Previously released Application Note (NOR Flash/Bus Switch Design Note)
 - https://frontgrade.com/IsoveraURL/appnotes/DesignNote_Bus_Switch_NOR_Flash.pdf

Acronyms

- TID Total Ionizing Dose
- GPIO General Purpose Input Output

Background Information

The UT8QNF8M8 NOR Flash TID performance is increased to 50 krad(Si) if the device is powered down during 90% of its design life. In order to prevent the UT8QNF8M8 device from being powered through the I/O signals, the entire device must be isolated not only from VDD but the I/O signals as well when it is not being accessed. One good way to implement this functionality is to use Bus Switches that when disabled, isolates power, as well as the paths for the I/O to and from the device.

Example of Notional Design Implementation

The example shown in Figure 1 implements a UT700 microprocessor interfacing to the NOR Flash using two Bus Switches. The additional device Frontgrade Semiconductor Voltage Supervisor, the UT04VS33, is an example of what is required to handle the power on reset condition.

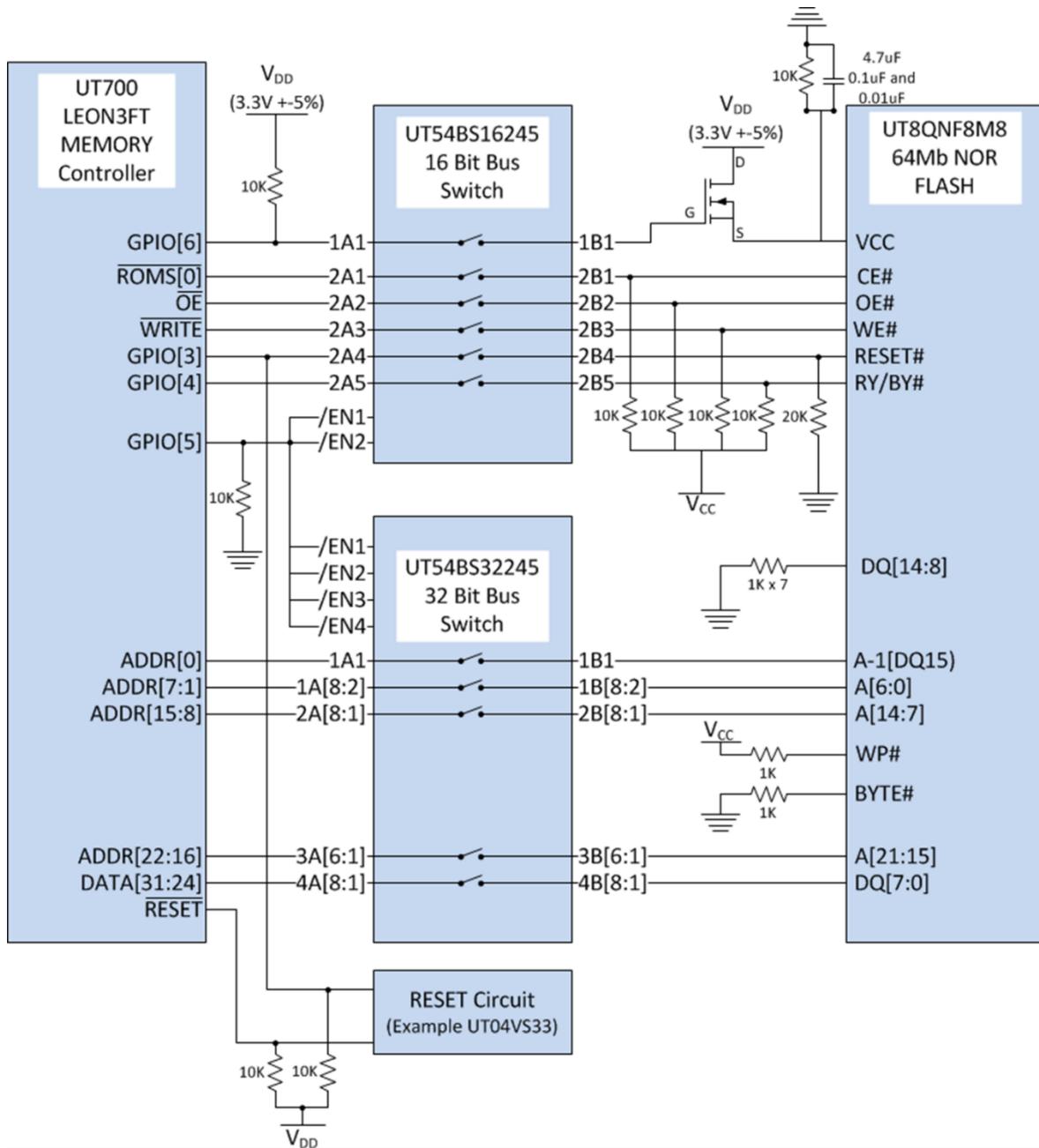


Figure 1. 50 krad(Si) TID Example Design

LEON 3FT UT700 Microprocessor Interface

The UT700 requires all of the signals shown in Figure 1 to access the NOR Flash connected to the appropriate Bus Switches. For the NOR Flash isolation example, additional signals in the form of GPIO are required to control when the processor requires access to the NOR Flash and when it enables the isolation feature.

Address, Data and Control

Connect the Address, Data and control signals from the UT700 Microprocessor are connected to the appropriate signals on the Bus Switch device identified in the drawing Figure 1.

GPIO

There are three GPIO signals required to implement the NOR Flash Isolation example design. Two of them are required for the isolation and the third is simply for interfacing to the NOR Flash device itself. Note, the pulldown 10K resistor is required for power up and enables the NOR Flash to be accessible by the UT700 Microprocessor after power is stable. In this example the NOR Flash is the boot ROM for the UT700.

GPIO[3]

The GPIO[3] signal manages the RESET# signal on the NOR Flash during accesses that do not involve power up. It gives users the ability to control when the UT700 resets the NOR Flash. For the power up reset condition, the Voltage Supervisor holds the RESET# low for the programmed duration and once that time has been reached, the 10K resistor will pull RESET# high. User's may then program GPIO[3] to toggle whenever they wish to reset the NOR. Note that the UT700 defaults all GPIO to inputs on power up or reset.

The timing of the resets from the Voltage Supervisor must be set such that the NOR Flash comes out of reset first and the reset to the UT700 is release some time after that. The timing must meet the specifications for both the UT700 and the NOR Flash.

GPIO[4]

The GPIO[4] signal is used to monitor the RY/BY# signal. The active low signal indicates when the NOR Flash is busy servicing a transaction.

GPIO[5]

The GPIO[5] signal is used to control when to enable or disable the isolation feature of the example design. All /EN signals on the Bus Switches are active low. The 10k ohm pulldown resistor ensures the Bus Switch has all of the signals and VCC enabled during power up. Note again that all GPIO signals on the UT700 are set as inputs during power up or reset.

GPIO[6]

The GPIO[5] signal is implemented to turn on the power FET which in turn controls the power on the NOR Flash. Notice the 10k pulldown which drives VCC low when the FET is turned off.

UT700 Reset

The RESET signal into the UT700 is controlled by the Voltage Supervisor. The UT700 must be reset on power up and as previously stated, the UT700 must come out of reset last on the board. Additional reset circuitry may be desired by individual users and are UT700 user implementation specific.

NOR Flash Interface

The NOR Flash requires some specific design setup in order for it to properly function when powered through the Bus Switch.

Address Bus

Addresses are connected directly from the Bus Switch to the address bus on the NOR Flash as shown in Figure 1.

Data Bus

The NOR Flash is set in 8 bit mode by connecting the BYTE# pin to ground using a 1k ohm pulldown resistor. This places the upper data bits (DQ[14:8]) in a tristate mode. The tri-stated DQ signals are also pulled low using 1k pulldown resistors. The other data bits are connected directly to the appropriate Bus Switch.

Control Signals

All control signals are pulled high using 10k ohm resistors. The result is unwanted accesses during power up of the device are disabled.

Write Protect (WP#)

For this example the write protect bit (WP#) is tied high using a 1K resistor disabling write protect. For designers that want to control this signal, one more Bus Switch channel is needed along with an additional GPIO on the UT700.

RESET#

The RESET# signal is handled by GPIO[3] or the voltage supervisor during the power on condition.

10k ohm VCC Pulldown

The pulldown resistor on the VCC supply of the NOR Flash is used to bleed off voltage on VCC when the device is powered down.

Board Layout Considerations

The layout of the NOR Flash must include a separate plane for the VCC power rail. Since the NOR Flash will be powered down during much of the mission life of the system, no other devices should be getting power from that plane.

Additional Notional Design Notes

It is always recommended to use series termination for the Address and Data lines as well as Control Signals from the UT700 to the NOR Flash. Users may also wish to have the data bus pulled high or low so that when data from memory interfaces is not being driven, the data bus is not floating.

Also please refer to a prior one-page design note referred to in Section 3, which is less detailed than this subject white paper, and uses sever parallel bus switch channels to supply power to the NOR Flash as opposed to the PowerFET reference in this paper.

Please note that this white paper and the prior design note are only recommended approaches that should User's chose to implement, that all implementations for broader system impact should be reviewed and accessed.

Conclusion

The UT8QNF8M8 NOR Flash offers excellent non-volatile memory density vs. footprint size for space flight applications. For designers requiring a non-volatile solution with 50 krad (Si) TID, the use of Bus Switches with the NOR Flash is a reasonable approach with limited impact on overall board real estate.

Revision History

Date	Revision #	Author	Change Description	Page #
08/26/2016	1.0.0		Initial Release	
1/24/2025	1.0.1	MJL	Converted to FG format	all

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