FRONTGRADE

UT32M0R500 RCCA Investigation Summary: Power Up Issue

Microelectronics Division
Frontgrade Technologies

April 2024

Product Information [D1]

Item	Information
PIC #	QS30
SMD #	5962-17212
UT PN	UT32M0R500
Failure Mode Reported	During power-up of the uC, the device periodically does not come out of reset mode.

Team Information [D1]

No.	Name	Role	Title
1	Bucky Young		Design Engineer
2	Bill Clulo/Marc Pevoteaux		Test Engineer
3	Brian Baranski		System Engineer
4	Anthony Wilson		Reliability/QA Engineer
5	Jose Betancourt/Jose Aguas/Owen Watry		Applications Engineer
6	Fiona Egan		Product Engineer
7	Robert Neubauer/Savannah Downing		Validation Engineer
8	Keith Ford		Program Manager

Problem Description [D2]

- During power-up of the uC, the device periodically does not come out of reset mode.
  - Issue is intermittent with a low occurrence rate
  - Occurs under various conditions

Containment Actions [D3]

No.	Containment Action Description	Status	Date Complete	Note/Comments
1	Trace all material shipped to affected customers to wafer lots	Complete	13 July 2023	All orders traced, no particular wafer/lot dependence seen
2	Identify inventory of wafers and finished product	Complete	13 July 2023	~ 24 prototype parts in inventory for use in this investigation
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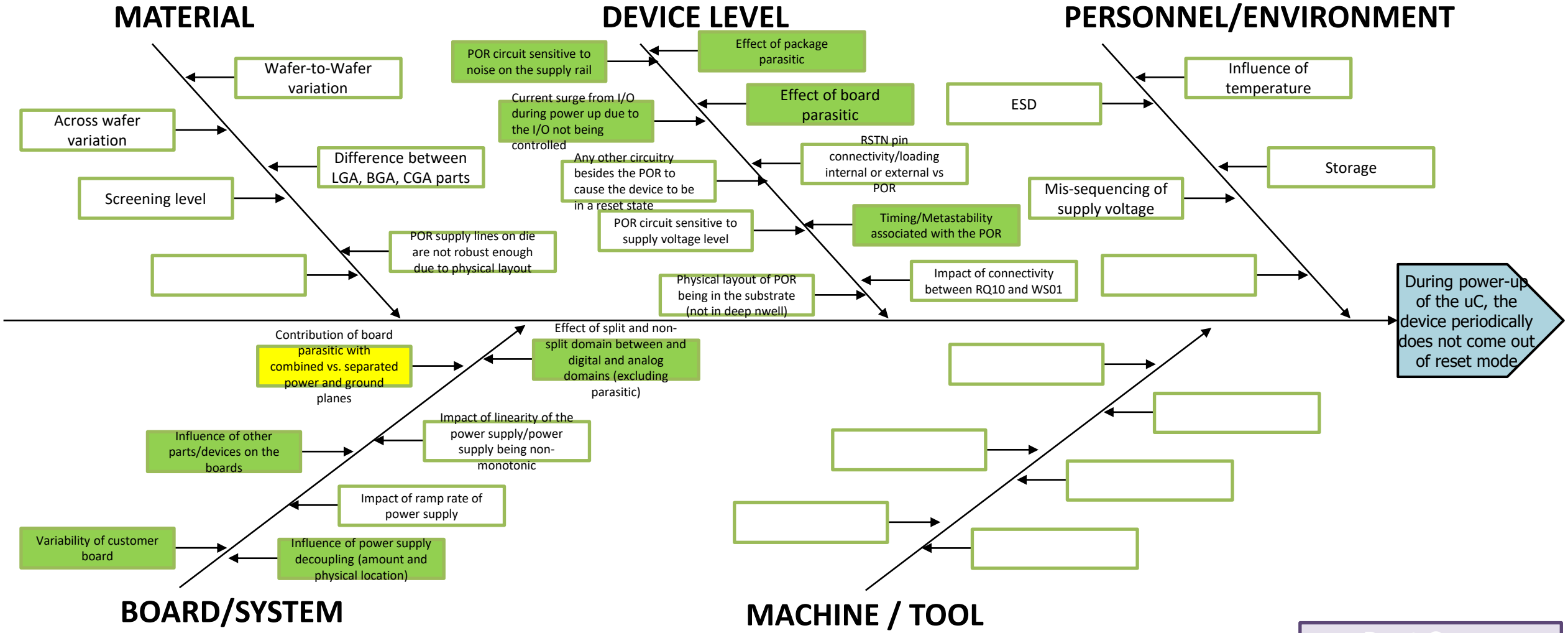
Root Cause Investigation [D4]

Fishbone Diagram



Least Likely | Likely | Most Likely

Root Cause

Root Cause Investigation [D4]

Root Cause Tracking List

Factor	Hypothesis	Likelihood	Action	Status	Notes
Device Level	POR circuit sensitive to noise on the supply rail	Likely	1. Simulation with device layout pkg and/or board parasitic	Complete	Simulations with parasitic extracted netlists of POR cell, resistance in supply connections, package wirebond model estimates. Noise added to supply voltages, repeated with LDO regulator. Added fast large glitches to supplies. No problems found, POR function OK
			2. Simulation with noise injection on supply	Complete	
			3. Bench test with board with and without common ground rail with noise injection on the supply	No action	Previously performed without any findings
	Current surge from I/O during power up due to the I/O not being controlled	Likely	1. Investigate/document the state of the I/O during power up	No action	Determined to be lower rank action
	Effect of package parasitic	Likely	1. Simulate circuit design with package parasitic	Complete	Simulations were performed using an estimated package model. No problems found, POR function OK
	Timing/Metastability associated with the POR	Likely	1. Investigate timing sensitivity using simulation	Complete	No timing issues found
	POR circuit sensitive to supply voltage level	Least Likely		No action	
	POR circuit sensitive to process variation	Least Likely	1. Perform probing on die of various intermediate nodes within the POR circuitry	No action	No dependence seen
	Any other circuitry besides the POR to cause the device to be in a reset state	Least Likely		No action	POR_SHUTDOWN isolates POR from other circuitry
	RSTN pin connectivity/loading internal or external vs POR	Least Likely		No action	

Root Cause Investigation [D4]

Root Cause Tracking List

Factor	Hypothesis	Likelihood	Action	Status	Notes
Board/System	Contribution of board parasitic with combined vs. separated power and ground planes	Most Likely	1. Respin one of the eval boards with and without ground planes	Complete	Detailed in test section
			2. Shorting pins together on existing eval board	Complete	No problems found
			3. Adding coupling caps between the two different grounds and adding caps between the two different supply voltages	Complete	No problems found
	Effect of split and non-split domain between and digital and analog domains (excluding parasitic)	Likely	1. Investigate the effect of difference in supply voltage levels by testing at the board level	Complete	Ramped the supply voltage with no difference in POR performance.
	Influence of other parts/devices on the boards	Likely	1. Investigate with a known bad part, then add or subtract components on the board to see effect	Complete	See "QS30_RCCA_Functional_Test_Summary.docx"
	Influence of power supply decoupling (amount and physical location)	Likely	1. Investigate adding and/or subtracting capacitance on supply	Complete	Analysis indicated that capacitance would have minimum impact on issue.
			2. Review placement of caps on various boards	Complete	
	Impact of linearity of the power supply/power supply being non-monotonic	Likely	1. Perform power-up simulation using a non-linear supply ramp	Complete	simulated non-linear power supply startups During start up time, one or two supplies dropped below detector threshold & returned to high value; ran all combinations. POR begins functioning over again and completes normally. Also, simulated combinations of supply power-up sequencing. No problems found. POR function OK.
			2. Perform power-up testing in lab with non-linear supply ramp	Complete	Performed a "piece-wise" linear step of the power supply to mimic a non-linear supply. No problems found.
	Variability of customer board	Likely			
	Effect of board parasitic	Likely	1. Simulate circuit design with board parasitic	Complete	Simulation including parasitics that would mimic board were performed. See followings slides on "Simulation Conditions/Details"

Root Cause Investigation [D4]

Root Cause Tracking List

Factor	Hypothesis	Likelihood	Action	Status	Notes
Material	Fabrication process has significant variation	Least Likely		No Action	No correlation found
	Wafer-to-Wafer variation	Least Likely		No Action	No correlation found
	Across wafer variation	Least Likely		No Action	No correlation found
	POR supply lines on die are not robust enough due to physical layout	Least Likely		No Action	
	Difference between LGA, BGA, and CGA	Least Likely		No Action	No correlation found
	Screening Level	Least Likely	1. Investigate ATE program for automatic power cycle per the program	Complete	No anomalies found in test program or hardware
Personnel/Environment	Mis-Sequencing of supply voltage causing an issue	Least Likely		No Action	
	ESD	Least Likely		No Action	
	Influence of temperature	Least Likely		No Action	Characterized
	Storage	Least Likely		No Action	

Root Cause Investigation [D4]

Simulation Conditions/Details

Simulations summation

- First simulations are looking for indications of any problems; discussing that application problems for some particular devices are found to be at narrow temperature ranges
  - Simulated with temperature sweeps from -50C to 120C by 10C steps
  - Then repeated simulations for power-up supply ramps 0V-VDD 1ms, 10ms, 100ms
  - Additional simulated with added supply noise 100kHz, 100mVpp (later 10 - 100MHz 100mV, 250mV)
  - Results: No problems found

- Simulation of POR:
  - With parasitic RC extracted
  - Also added noise to supply 100kHz, 100mVpp
  - Results: No problems found

Root Cause Investigation [D4]

Simulation Conditions/Details cont'd

- Added resistance to ground and supplies, sweeping 10, 30, 100 ohm using pex netlist, ramp supplies 0V-VDD over 1ms
  - Results: No problems found, all results ok

- Inspected microcontroller physical layout for resistance in power supply connections outside the por cell, estimate < 10 ohm -- continued with series 10 ohm added into other sims
  - Results ok.

- additional simulation saved signals into hierarchy at counter flip-flops. Inspecting the asynchronous clear which is asserted at beginning of reset delay for influence of noise. Added wirebond parasitics 1nH, 100mohm.
  - Results ok.

Root Cause Investigation [D4]

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Simulation Conditions/Details cont'd

- Simulated with fast ramping the supplies 0V-VDD at 10ns & 100ps
  - attempting to upset the early operation & timing
  - Results: Did not affect the function of reset being released after an initial power-on delay

- Checked power up sequencing with relative delay between three supplies
  - Simulated six combinations, such as VDDC delayed 10ms, VDDC & VDDA delayed 10ms, etc.
  - Results: No problems found.

- Simulated large & fast noise glitches on supplies during clocking
  - Results: Did not change por reset function. Internal digital signals changed states, but FFs didn't latch wrong values.

Root Cause Investigation [D4]

Simulation Conditions/Details cont'd

- Forced operating delay counters into illegal all-ones state.
  - Requires overcoming triplicate redundancy and using artificial stimulus or shorting the circuitry during simulation.
  - Unable to force this state using "noise" on the supplies.
  - 1. if only one of three triplicated redundant LFSR counter is stuck then the POR recovers and reset is released.
  - 2. if two of the three counters enters the all-ones stuck state, then the resetb is never released (and the por internal clock never stops)
  - Examining the flip-flop clocks and SET-filter/buffer, adding noise 10 - 100MHz, 100mV, 250mV, etc. was able to cause false edges disrupting ff clocking.
  - Results: POR is able to be artificially stuck by injecting/forcing internal nodes. Not able to replicate with external connections

- Simulated non-linear power supply startups
  - One or two supplies dropped below detector threshold & returned to high value; ran all combinations.
  - Results: POR begins functioning over again and completes normally.

- Examined the por start-up signals and FF asynchronous clear timing (powerpoint "por functional timing")
  - Results: No anomalies found, POR function properly

Root Cause Investigation [D4]

Simulation Conditions/Details cont'd

- Simulations with LDO (powerpoint "output SR latch and clock signals")
  - Added LDO regulator which supplies the internal 1.5V supply VDDC and noise to the supply. Looking for how noise may couple into the POR system externally. The regulator provides rejection, for example noise on 3.3V supply 250mV, 100MHz is reduced to ~15mV at 1.5V core supply. Added impedance at external supplies and ground.
  - Results: Did not cause errors in POR function.

Root Cause Investigation [D4]

Bench Test Results

- Test procedure involved 500 power cycles per temperature, with 5 degree temperature steps from -30C to 80C. (Temperature range optimized from feedback on where customers were seeing issues)
- Anomaly was only able to be duplicated on a customer supplied board.
- New boards with a similar design and layout were fabricated but no failures were observed on these boards.
- Failing customer board was reworked (twice) with new parts that had passed on Frontgrade boards. 1 part showed no failures, second part had a low failure rate (23% at worst temperature, 1.6% over all temps)
- Original failing part on customer board did not fail on Frontgrade board.
- The bench testing demonstrated that there is some level of board interaction with the device as related to the POR anomaly but no definitive conclusions were able to be drawn.

Material Disposition [D4]

- Material dispositioned to use “as is” with the following actions:
  - Update of the datasheet to include notes on use of POR_SHUTDOWN pin – Complete
  - Update of datasheet to include notes on the use of separate digital and analog ground planes – Complete
  - Creating of ADEPT/GIDEP (#GB4-P-23-02) advisory of the issue and similar notes as mentioned above - Complete

Validation [D5]

- Validation of the use of the POR_SHUTDOWN with external reset has been confirmed through bench level testing

Corrective Actions [D6]

No.	Corrective Action Description	Status	Date Complete	Note/Comments
1	Include wording in datasheet for use of the POR_SHUTDOWN pin to mitigate issue	Complete	May 07, 2024	
2	Include wording in datasheet for use of separate analog and digital ground planes	Complete	May 07, 2024	
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Preventative Actions [D7]

No.	Preventative Action Description	Status	Date Complete	Note/Comments
1	Use of the POR_SHUTDOWN pin and external reset will prevent issue	Complete	May 07, 2024	
2	Overall failure rate is low. If POR_SHUTDOWN is not an option additional power cycles may be required to use as is	Complete	May 07, 2024	
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Closure [D8]

- This 8D is closed with the following:
  - Issue related to anomalous behavior of the POR not coming out of reset was confirmed
  - Investigation at the circuit level was performed without a “direct” link to the issue
  - Various simulations were performed without a “direct” link to the issue
  - Various hardware configurations were tested without a “direct” link to the issue
  - Determination from the investigation is the issue has contributing factors from the design architecture interacting with the board design and board parasitic
  - Recommended solution is to use the POR_SHUTDOWN pin to mitigate the issue all together or use as is with potential for extra power cycles required.