FRONTGRADE

TECHNICAL NOTE

UT8SDMQ64M4x

Bit Errors Due to Aging

2/27/2024
Version #: 1.3.0

Table 1: Cross Reference of Applicable Devices

Product Name	Manufacturer Part Number	SMD Number	Device Type	Frontgrade Product Identification Code
2.5 Gigabit SDRAM MCM	UT8SDMQ64M40	N/A	SDRAM	QS18
3.0 Gigabit SDRAM MCM	UT8SDMQ64M48	N/A	SDRAM	QS19

Summary

An aging study was performed on the Frontgrade UT8SDMQ64M4x SDRAM product. The purpose of this study was to evaluate the increase of bit errors over time (aging) as a function of temperature when biased. Aging of the SDRAM product was performed on a total of 45 devices pulled from three different wafer lots. The devices were stressed at bias conditions of maximum supply voltage = 3.6 V and at a temperature = 125°C for an equivalent of 8008 hours when de-rated to a temperature of 105°C. The results of the study showed that all 45 devices increased in the number of bit errors as a function of stress time. Based on in-depth testing of 6 devices in obtaining the exact bit errors across the array, analysis indicated that the bit errors increased over time in an approximate linear fashion. In analyzing the data, a model was developed to calculate the number of bit errors as a function of time (t) and temperature (T) using a linear model for the bit errors and an Arrhenius based model for temperature. The model predicts a maximum of 8522 bit errors when operating continuously for 15 years at 105°C. The bit error prediction model was used in combination with a binomial distribution to calculate the probability of 1, 2, and 3 bit errors per 8-bit, 40-bit, and 48-bit words.

Overview/Background

Synchronous dynamic random access memory (SDRAM) devices are used in a wide range of space applications. SDRAM is a type of volatile memory that needs to be periodically refreshed to retain its contents.

As with any memory device, bit errors are major concern, especially for high reliable systems. A bit error is an event that leads to one or more memory bits being read differently from how they were last written. Concern for bit errors stems from the fact that they can manifest from various events including aging.

In an effort to understand the bit errors due to aging in the UT8SDMQ64M48 SDRAM, Frontgrade conducted an experiment. This document provides a summary of the experiment. This information is also applicable to the UT8SDMQ64M40 device.

Product Description

The product used in this experiment was the UT8SDMQ64M48 SDRAM, which is an MCM single package device utilizing six 512Mb SDRAM die.

Experiment

The main objective of this experiment was to investigate bit errors as a function of operational use hours (i.e. aging). Additionally, product lifetime models were developed to predict reliability (bit errors) in both long-term and harsh

environments. Dynamic burn-in stress was utilized throughout the entire experiment in which all memory cells were continuously operated under accelerated temperature conditions.

Sample Selection

For this experiment, 45 UT8SDMQ64M48 devices were selected from production material. Device selection was based on a number of factors in order to insure the experiment population included a wide mix of material. The selection process covered items such as:

- Material from different wafer lots
- Material from different package assembly lots
- Material from different process flows (i.e. Q, Q+ level flows)
- Devices that passed 3-temperature electrical test (aside from bit failures)
- Material that exhibited bit failures at each of the production temperatures

Table 2 summarizes the mix of devices included in the experiment.

Table 2: Summary Information from Production Material Used in This Work.[1]

Description	Quantity
Number of wafer lots[2]	3
Package Styles	2
Process Flows[3]	2
Devices Passing All Electrical Tests across Temperature	17
Devices with only Bit Failures	28
Package Assembly Lots	6

Note

1. Based on the wafer lot information and data collected, this document is applicable to devices produced from wafer lots: 8009340, 8009350, 8009360, 8009370, 8009380, 8009390, 8009400.
2. Wafer lots included in the aging study are: 8009360, 8009380, and 8009390.
3. Includes QML Q and QML Q with additional screening as defined in SMD Section 4.1.2.

The selected devices were taken from available production material, which had been processed through different points in the manufacturing flow. This indicates that the selected devices experienced various amounts of testing and burn-in prior to their selection for the experiment. The wafer lots and devices included in the aging study were 8009360 (SN2), 8009380 (SN10, SN21, SN25, SN138), and 8009390 (SN24). Based on the collected data from the aging study and distribution of wafer lots used, the results of the aging study are applicable to the following wafer lots: 8009340, 8009350, 8009360, 8009370, 8009380, 8009390, 8009400.

Test and Stress Methodology

For this experiment, a stress-measure-stress (SMS) methodology was utilized. Detailed in Figure 1 is an outline of the experiment flow.

The experiment included 8 stress cycles with both electrical and bit location testing conducted after each stress cycle. The experiment had defined stress times of 0, 168, 336, 504, 672, 840, 1008, 2508, and 4008 hours. During the stress cycles, devices were stressed at an accelerated temperature of 125°C to facilitate data collection for performing lifetime analysis.

Each of the stress cycles correspond to a read point which are referenced from RP0 to RP8 for each of the post stress read point.

The electrical test was performed across three temperatures (-40°C, 25°C, 105°C) using the same electrical test program used for production. Product level electrical testing was performed on all 45 devices at the end of each stress cycle. An important note is that the 45 devices only went through RP0 – RP6.

In addition to the use of the production electrical test program, a bit location test program was developed for this experiment. The bit location test program contains a collection of 32 patterns that when combined together test all memory bits in a device for both zeros and ones. The bit location testing was performed on 6 devices at the end of each stress cycle. With an important note that the 6 devices went through all read points RP0 – RP8.

The bit location patterns activate/write/read the data in each row/column in the same order each time. Each pattern writes values into the memory, reads the expected values, writes new values to the memory, and reads the expected values. These patterns use a 10 MHz clock frequency for writes and a 100 MHz clock frequency for reads. This combination of clock frequencies and patterns translates into a refresh time of 13.9 ms, product maximum refresh time is 32 ms.

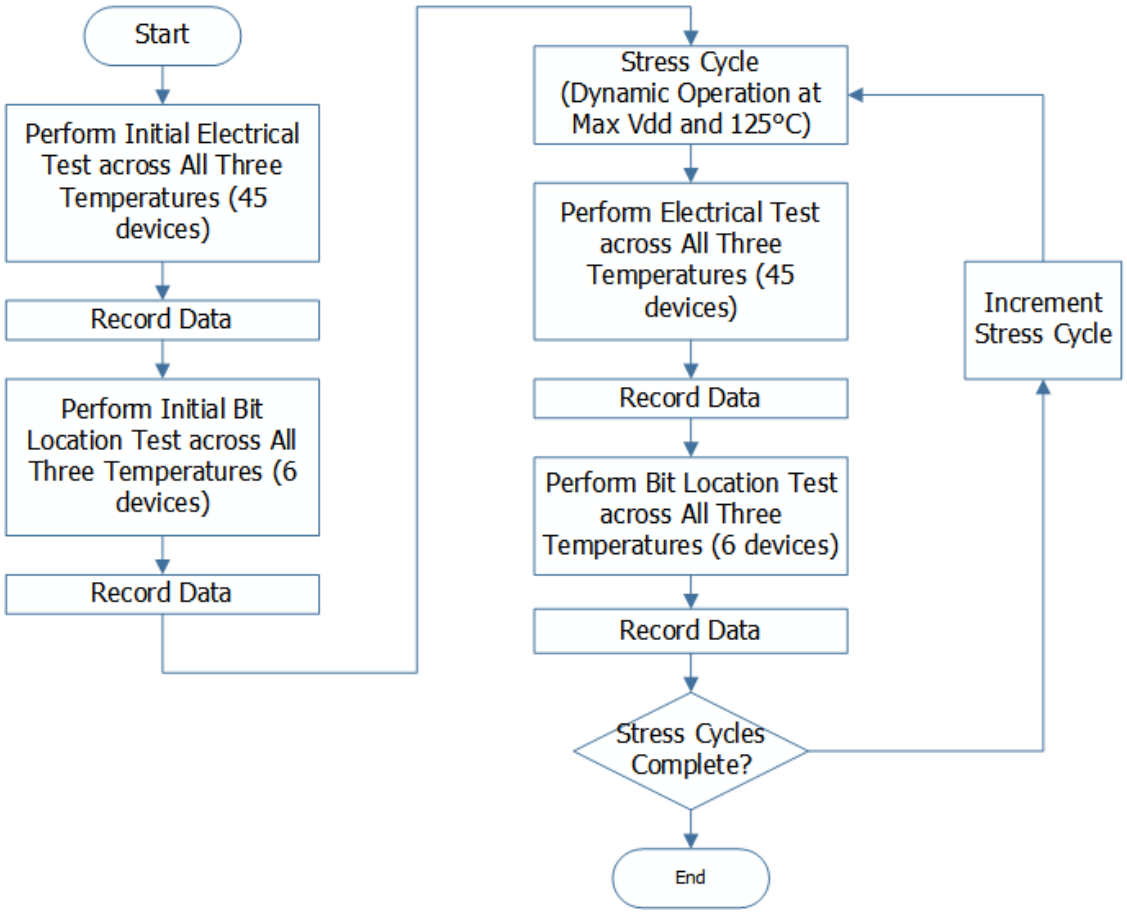

Figure 1: Flow diagram of experiment stress-measure-stress cycles.

At the end of each stress cycle, product engineering performed a review of the electrical test data and retested any devices that were suspected of being false failures. This was done in an effort to minimize failure signatures that were not representative of device performance.

Results and Analysis

Observations from Production Electrical Test

From the production testing using data from RP0 to RP6, the data showed that the number of devices having bit failures increased over time. Figure 2 shows this in both graphical and table formats.

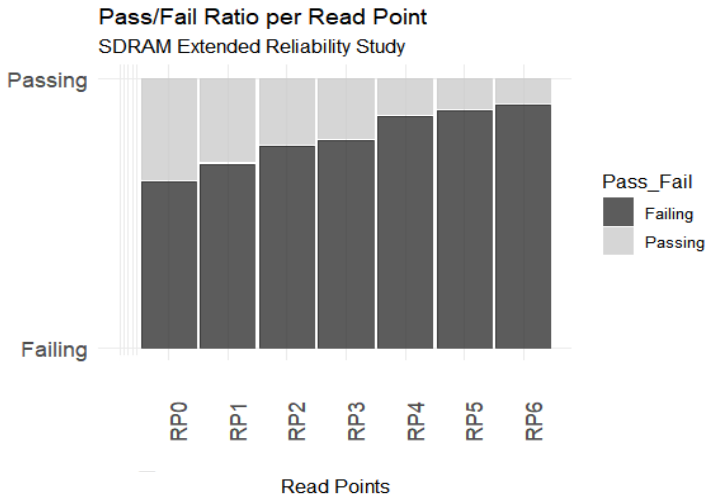

Figure 2a

Read Point	Passing	Failing
RP0	17	28
RP1	14	31
RP2	11	34
RP3	10	35
RP4	6	39
RP5	5	40
RP6	4	41

Figure 2b

Note:
Figure 2: Trend results from production testing showing increasing bit errors at the end of each stress cycle. (a) Mosaic plot showing passing and failing trend. (b) Numerical account of passing and failing.

In addition to the bit failure increase across the stress cycles, the following trends were observed when analyzing the data one temperature at a time:

- Passing devices changed to failing
- Failing devices changed to passing
- Passing devices remained passing
- Failing devices remained failing

The nature of the bit failures causing passing devices to change to failing and then reverse across the different stress intervals was observed. This is discussed in a later section.

Observations from Bit Location Testing

Failure Mode Classifications

Two unique failure modes were identified from the bit location test results. The first failure mode (“Bit-to-Bit” Mode) is classified as having two bits that appear to have a variable resistive connection between them that share the same column address on neighboring row addresses. The Bit-to-Bit failure mode was observed during electrical testing at all 3 temperatures, with hot being the worst case and cold being the best.

Shown in Figure is a graph of the observed bit failures for the Bit-to-Bit Mode. The graph groups the rows for the specified pattern signature and shows the number of bit failures for each test temperature at each of the stress cycles. The graph provides information that some of the bit errors disappear after appearing. In addition, the graph illustrates that the bit errors range from 1 to 3, with a single occurrence of a 3 bit error.

Observations of the Bit-to-Bit failure mode suggests that a variable resistive bridging occurring between neighboring bit cells causes a progression of symptoms as the resistance values decreases. Based on the observations of the bit error changes over time, the progression appears to follow the resistive pattern illustrated in Figure .

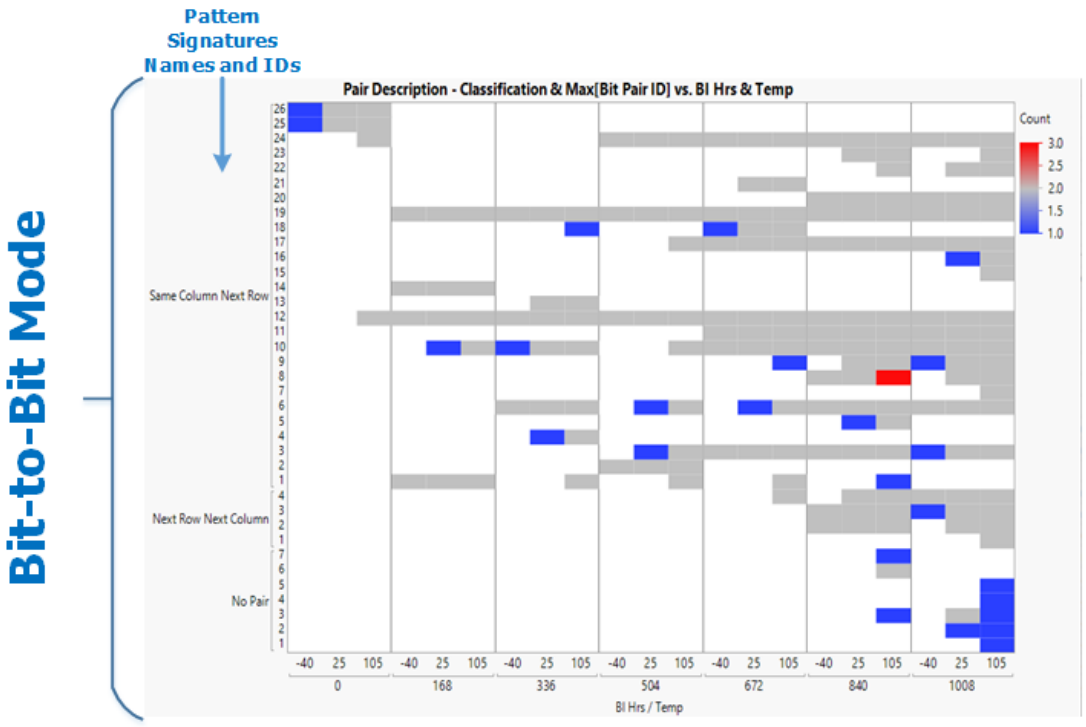

Figure 3: Graph showing Bit-to-Bit Mode bit errors for each stress cycle as a function of temperature. Numbers in the y-axis are row numbers associated with the pattern signature.

Resistance Between Neighboring Bit Cells			
High Resistance →			→ Low Resistance
No failure observed	One bit observed failure once	Two bits observed failure once each	One bit observed failing twice
Resistance between bits is high enough to prevent changes to the measured values	Bit fails when it should have been in charged state	Bits fail when they should have been in the charged state	Bit fails once for the charged state, once for the discharged state

Figure 4: Illustration of impact of bit-to-bit bridging resistance on bit errors.

The variable resistance illustration shown in Figure is used to help explain the occurrence of the 1 bit failures and 3 bit failures, where by as the resistance decreases then one bit can fail twice while two bits fail once.

The second observed failure mode (“Cold” Mode) was classified as having multiple bit errors on multiple column addresses, all on the same row address. This failure mode was observed only at cold (i.e. “Cold” Mode), and were only observed after some of the stress cycles. Another characteristic of the failure mode is that the bit errors often appeared and then disappeared as a function of the stress cycles. This is illustrated in Figure .

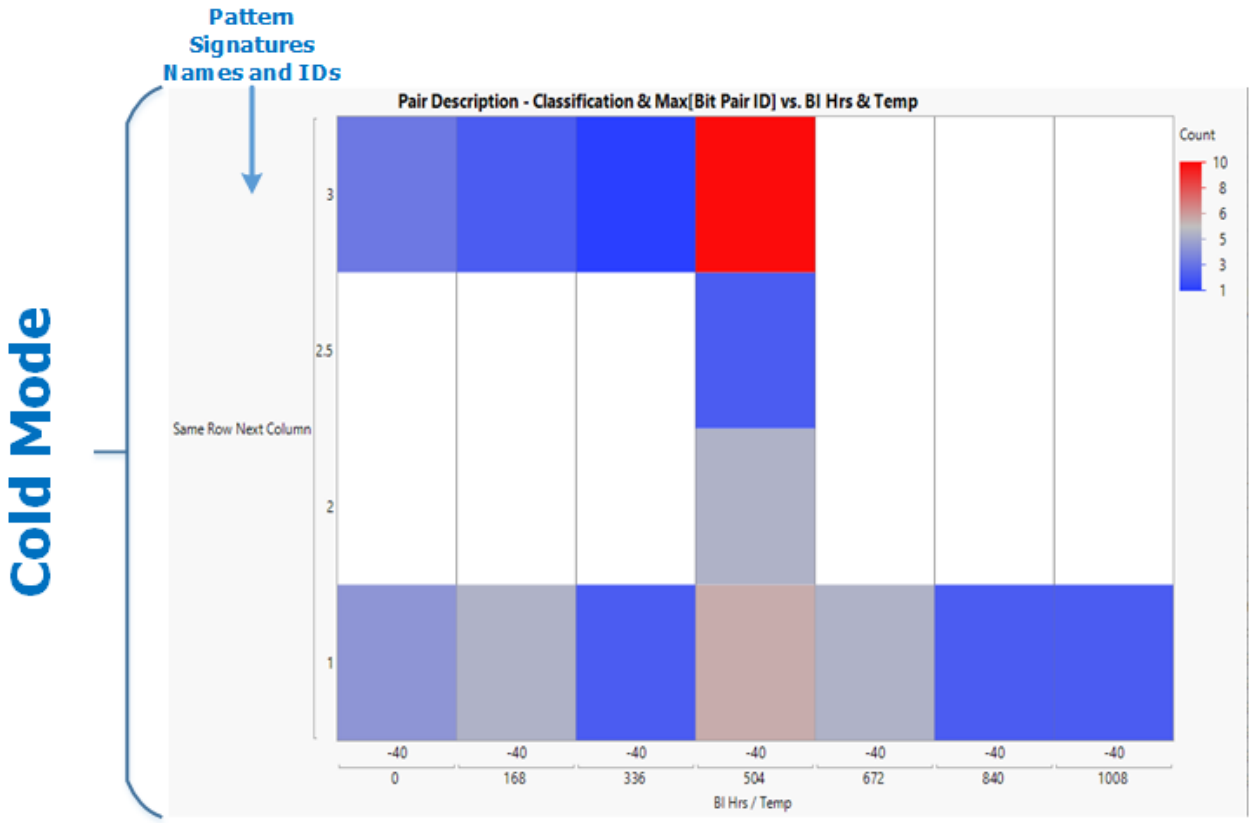

Figure 5: Graph showing Cold Mode bit errors for each stress cycle as a function of temperature. Numbers in the y-axis are row numbers associated with the pattern signature.

Row Locations for Unique Failing Bits

Further observations of the data indicated that a majority of the bit errors occurred in row 0 and row 1 of the memory array. Figure shows the number of bit errors captured for each unique row across all the die (6 devices * 6 die = 36 total die) across all of the read points across all of the electrical test temperatures. Further analysis of the data indicated the ~51% of the observed failing bits were located in row 0 and row 1. Further details on the row locations can be in Table A.1.

Bit Fails per Die

As each device contains six die, the data from the bit location testing was also analyzed to determine if there was any trend of the bit fails at the die level. The bit errors were aggregated across the 36 die for each read point and for the three electrical test temperatures performed as read point. Shown in Figure for data collected at 105°C, no observable trend was found that indicated that any of the six die had a majority of bit errors. It is observed that die 5 (D5) did not show any bit errors until RP3 and die 1 (D1) did not show any bit errors until RP7. Further details on the bit fails per die can be in Table A.2.

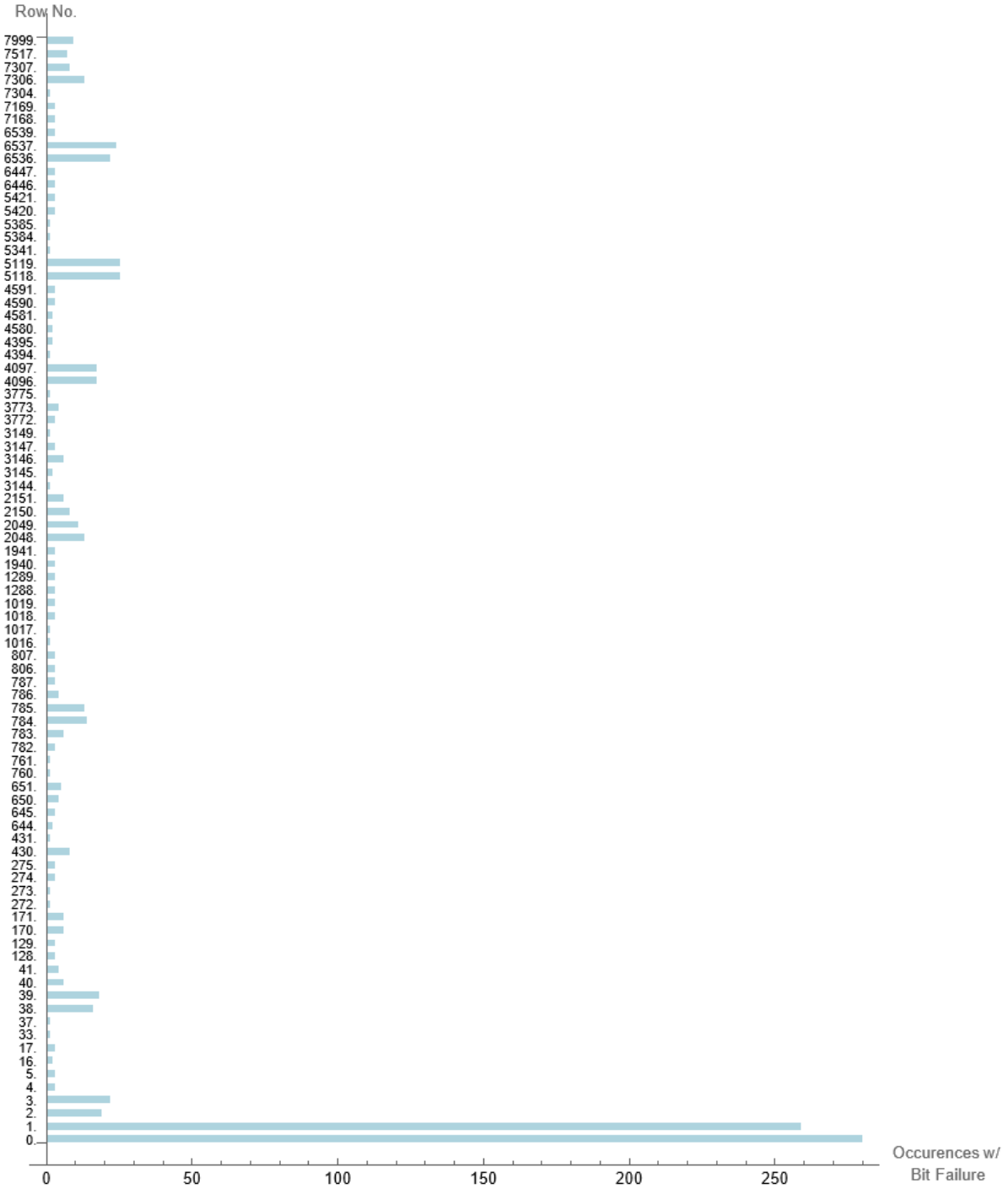

Figure 6: Graph showing all unique rows with bit errors from the bit location testing (across all three temperatures tested).

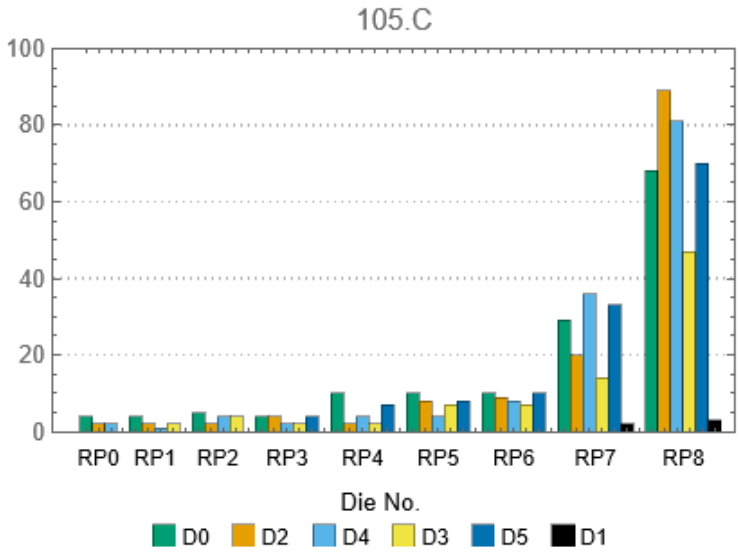

Figure 7: Distribution of Bit Fails per Die for each Read Point at 105°C

Bit Fails per Bank

As each die contains four banks, the data from the bit location testing was analyzed to determine if there was any trend of the bit fails at the bank level. The bit errors were aggregated across the 144 banks for each read point and for the three electrical test temperatures performed at each read point. Shown in Figure 8below for data collected at 105°C, no observable trend was found that indicated that any one of the four banks had a majority of bit errors. Further details on the bit fails per bank can be in Table A.3.

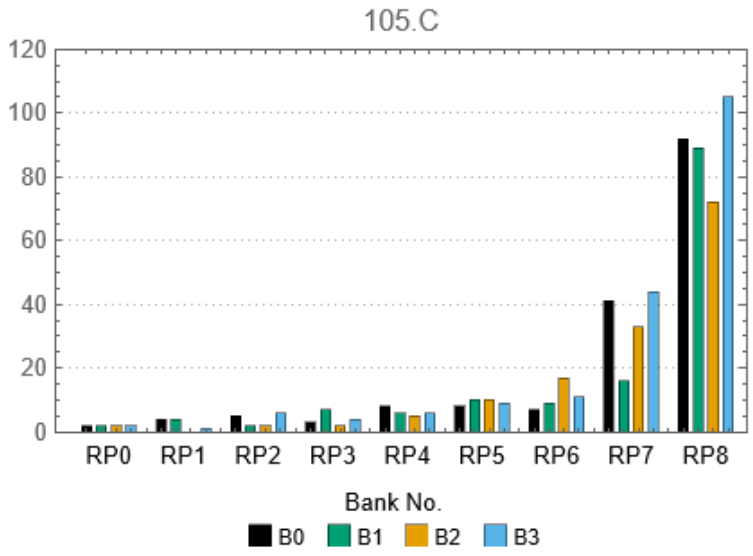

Figure 8: Distribution of Bit Fails per Bank for each Read Point at 105°C

Failing Bit Pairs

Failing bit pairs were observed between row number modulo 4 = 0&1 and 2&3. And based on review of the memory architecture, these are consistent with rows where one row stores true data while the other stores complement data. No failing bit pairs were observed between row number modulo 4 = 1&2 or 3&0. These row combinations are consistent with rows that use the same charge/logic (true data or complement data).

Given the charge/logic mapping and the test program methods, it is more likely that resistive bridging would be found between rows where the row number modulo 4 is 0&1 or 2&3.

Based on the test program used for the experiment, detection of resistive bridging between any two rows is expected to be observed on half of the rows. Therefore, the probability of observing failures between any given row is 50%. And although the presence of a majority of the failing bits occurred on row 0 and row 1 giving strong evidence that these failures are dependent on row position, the 50% estimate is to provide a conservative approach for the bit error prediction analysis described in upcoming sections.

Bit Pair DQs

Based on memory architecture reference material, it suggests that certain DQ pins are near each other as depicted in Figure . The reference material also suggests that in a given bank, the bits related to 4 DQ pins are located in the top half of the bank, and the bits related to the other 4 DQ pins are located in the bottom half of the bank.

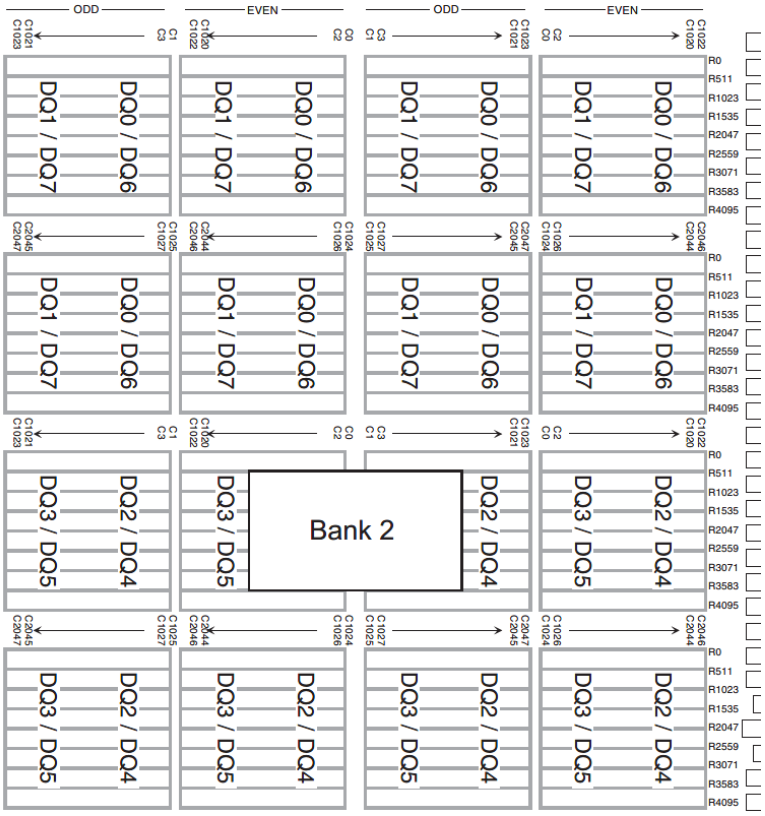

Figure 9: Illustration of DQ relationship in the memory architecture.

Assuming that all DQ7 and DQ1 are adjacent and then all DQ6 and DQ0 are also all adjacent, the probability that the bit location program would find an existing failure would be near zero (1/2048). This is an estimate for the lowest probability. For a high side estimate, it is assumed that DQ7/DQ1 is interleaved with DQ6/DQ0 and the expectation for observing a failure would be half of the time.

Bit Error Prediction Model

Regression analysis of stress data over time allows for creating lifetime predictive modeling. For this experiment, time is based on the equivalent time at a use temperature of 105°C. Therefore, the total accumulated time that the devices were under temperature acceleration is normalized to the use temperature is based on an Arrhenius based temperature acceleration model:

$$AF_{Temp}=Exp\left[\frac{E_a}{k_B} * \left(\frac{1}{T_{reference}} - \frac{1}{T_{use}}\right)\right] \quad \textbf{(1)}$$

Where

- E_a = activation Energy in eV = 0.45 eV
- k_B = Boltzmann's constant = 8.62 x 10^{-5} eV/K
- T_{use} = use temperature in K
- $T_{reference}$ = reference temperature in K = (378K = 105°C + 273)

Using an assumed and conservative activation energy of 0.45 eV, the equivalent device hours at 105°C were calculated and analysis performed for the bit error results for each temperature. Figure shows the worst case bit error results which occurred at 105°C. Below, in Table 3, is a list showing the regression parameters for each of the devices.

Table 3: Listing of Regression Analysis Results for Each Device. (Growth Rate * time + Intercept)

Device	Growth Rate (bits/hr)	Intercept
L3lki-rel_SN138	0.0403	-34.20
L3lki-rel_SN2	0.0260	-7.12
L3lki-rel_SN25	0.0024	11.20
L3lki-rel_SN24	0.0556	-43.72
L3lki-rel_SN10	0.0656	-103.00

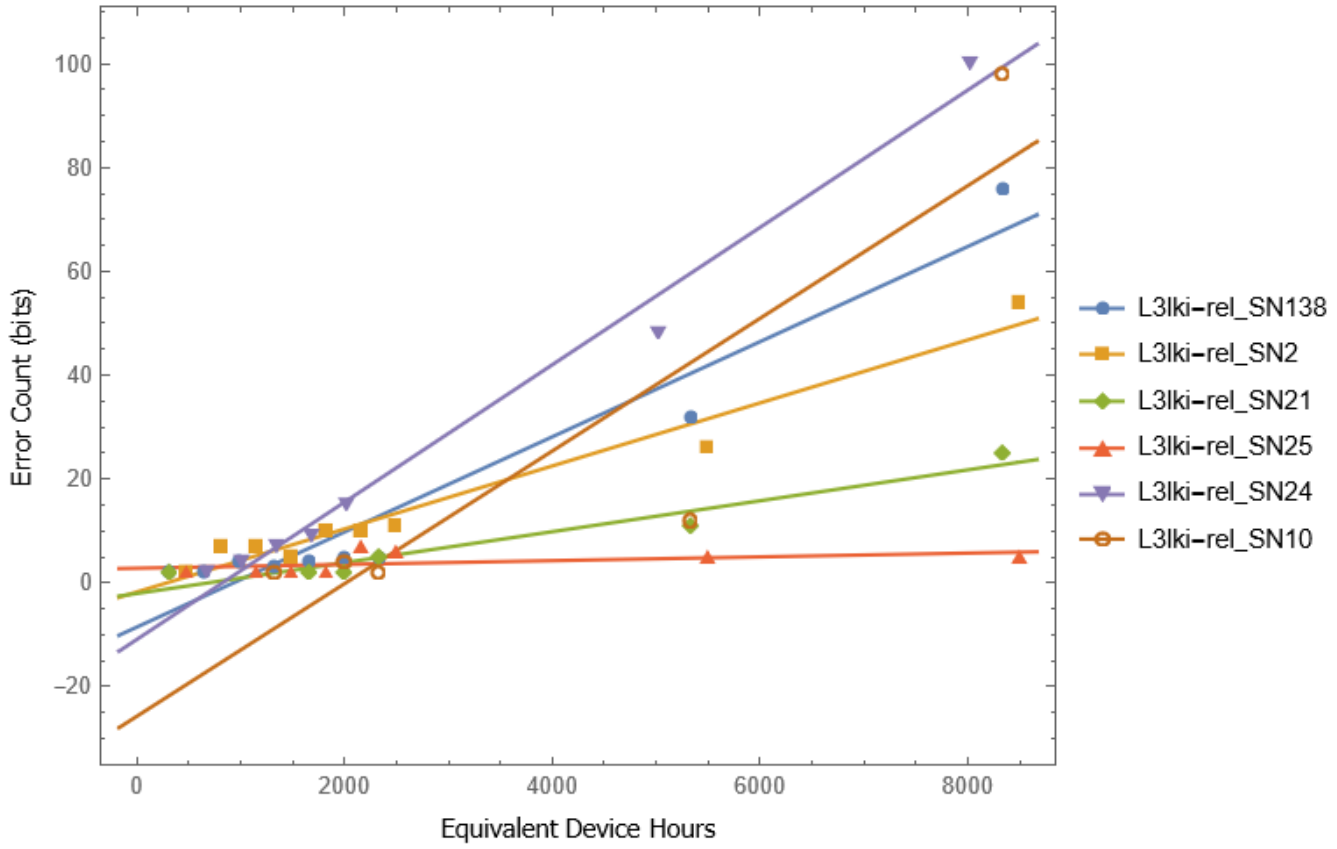

Figure 10: Plot of bit errors and regression models for the each of the devices. Data is from the 105°C bit location testing.

Based on the regression analysis, the error rates given in errors/hour were determined based on the slopes of the regression line. This analysis was performed on the data for each of the electrical test temperatures (-40°C, 25°C, and 105°C). Analysis was performed with all the data and with the Cold Mode data removed. And with the Cold Mode data removed only the -40°C error rate changed. Shown in Table 4 in the maximum error rate calculated from the data collected during the electrical test for each temperature. This data gives an indication that there is a slight temperature dependence in overall performance after stress has been applied. And as a note, the error rates in Table 4 does include the 4x factor as discussed in Section Bit Error Prediction Model.

Table 4: Calculated Error Rates from the Bit Location Data for Test Data Collected at Each Test Temperature.

Temperature	All Data			With Cold Mode Data Removed		
Electrical Test Temperature (°C)	Error Rate (error/hr)	Bit Error Rate[1] (error/bit-hr)	Bit Error Rate[1,2] (error/bit-day)	Error Rate (error/hr)	Bit Error Rate[1] (error/bit-hr)	Bit Error Rate[1] (error/bit-day)
-40	0.031	9.6 x 10-12	2.3 x 10-10	0.0088	2.8 x 10-12	6.7 x 10-11
25	0.047	1.4 x 10-11	3.5 x 10-10	No Change		
105	0.066	2.0 x 10-11	4.9 x 10-10	No Change		

Note:

1. Total number of bits per device = 3,221,225,472
2. This bit error rate includes a 4x factor to account for potentially missed errors due to the test pattern used.

Using the worst-case linear regression results (from SN10 at 105°C), the resultant model is:

$$\text{No. of Bit Errors}_{105°C} = -25.7 + 0.016 * t \quad \textbf{(2)}$$

Where *t* is time in hours. As mentioned in previous sections, it was observed that there was the possibility that 75% of bit errors may not have been observed. To account for this, the linear regression model is increased by 4x resulting in:

$$\text{No. of Bit Errors}_{105°C} = -103 + 0.066 * t \quad \textbf{(3)}$$

As an example, assuming continuous use at 105°C and a 15 year mission life, the total bit errors is estimated as 8569 using equation (3). Whereas the following gives an example of using the AF_{Temp} to calculate the number of bit errors for a given temperature and mission life.

For example, what are the estimated number of bit errors at the end of the mission life, assuming a constant use temperature of 80C and a mission life to 5 years?

First, using equation (3), determine the number of bit errors for the mission life (this is still at the reference temperature of 105°C):

$$\text{No. of Bit Errors}_{105°C} = -103 + 0.066 * (5 * 365 * 24) = 2788$$

Then, using equation (1), calculate the AF_{Temp} for 80°C:

$$AF_{Temp=80°C} = \text{Exp}\left[\frac{0.45}{8.62 \times 10^{-5}} * \left(\frac{1}{(105+273.15)} - \frac{1}{(80+273.15)}\right)\right] = 0.38$$

Then multiply the bit errors at 105°C by the temperature acceleration factor to get the bit errors at the use temperature of 80°C:

$$\text{No. of Bit Error}_{80°C} = AF_{Temp=80°C} * 2788 = 0.38 * 2788 = 1059$$

Bit Error Probability

For memory type devices, to estimate the probability of a bit error within a word, the binomial distribution can be used:

$$Pr(x)= \binom{n}{k} Pe^{k}(1-Pe)^{n-k} \quad \textbf{(4)}$$

Where

- Pe = probability that a bit failed
- n = number of bits per word (= 48)
- k = number of occurrences per n

To use the binomial distribution, first the bit error probability (Pe) must be determined based on:

$$Pe= \frac{\text{\# of bit errors}}{\text{total bits}} \quad \textbf{(5)}$$

And for this experiment, due to the large percentage of bit errors associated with row 0 and row 1, the bit error probability will be determined based on two different approaches:

- Approach #1 – Single bit error probability
  - Pe = worst case bit error probability across all rows

- Approach #2 – Separate bit error probability based on row segmentation
- $Pe_{rows0,1}$ = bit error probability using only bit errors associated with row 0 and row 1
  - P_{erows} = bit error probability using bit errors associated with rows >= 2

For each approach, the number of bit errors will be based on the linear regression equation (3).

Approach #1

For this approach, using equations (3) and (5), the Pe is given by:

$$Pe = \frac{-103+0.066*t}{3{,}221{,}225{,}472} \quad \textbf{(6)}$$

As seen by the time dependence for the Pe, the probability of a bit failure is also time dependent. As such, the follow graphs show the probability (Pr) of failure for 1, 2, and 3 bit errors per 48-bit word as a function of time. Where the total bits used in the denominator is the total bits in the SDRAM.

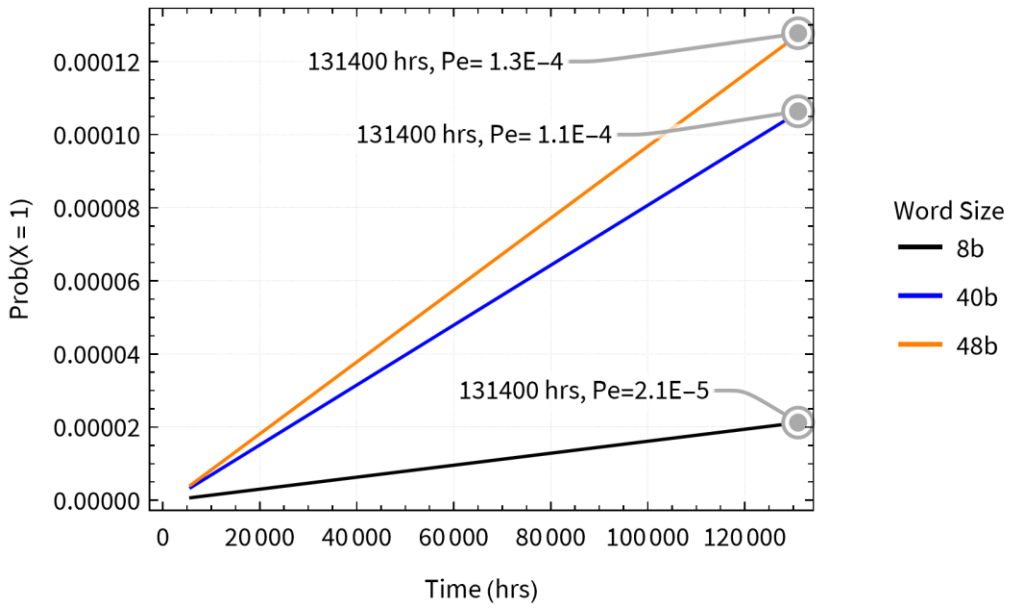

Figure 11: Plot of equation (6) showing probability of 1-bit error in an 8-bit (black), 40-bit (blue) or 48-bit (orange) word over time.

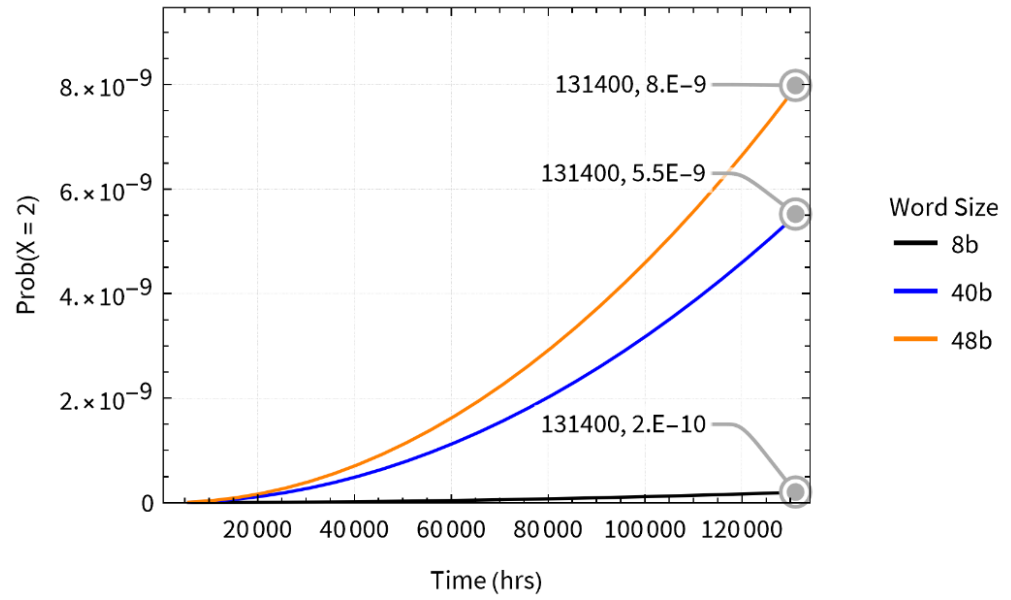

Figure 12: Plot of equation (6) showing probability of 2-bit errors in an 8-bit (black), 40-bit (blue) or 48-bit (orange) word over time.

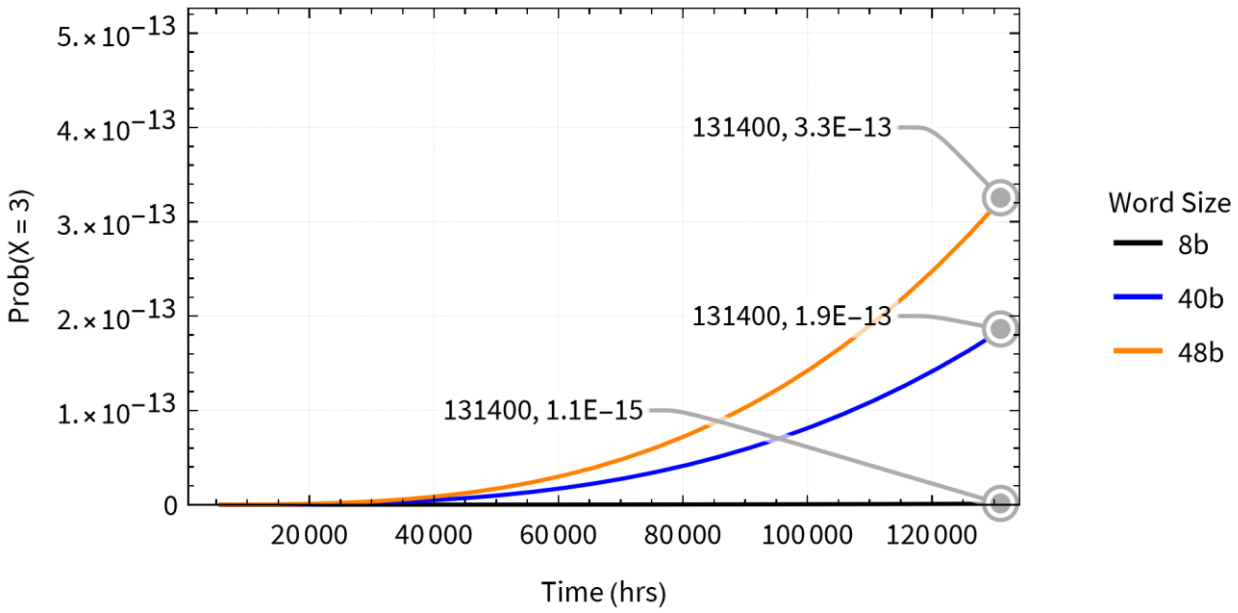

Figure 13: Plot of equation (6) showing probability of 3-bit errors in a 8-bit (black), 40-bit (blue) or 48-bit (orange) word over time.

Approach #2

The second approach partitions the bit errors based on the observation that row 0 and row 1 had majority (51%) of the errors. As such the two different Pe values are calculated as:

$$Pe_{rows0,1} = \frac{0.51^* (-103+0.066^*t)}{786,432} \quad \textbf{(7)}$$

$$Pe_{rows\geq 2} = \frac{0.49^* (-103+0.066^*t)}{3,220,439,040} \quad \textbf{(8)}$$

Similar to the first approach, Pe has a time dependence, therefore the probability of a bit failure is also time dependent. As such, the follow graphs show the probability (Pr) of failure for 1, 2, and 3 bit errors per 48-bit word as a function of time. Where the total bits used in Eq. (7) are based on rows 0 and 1 and for Eq. (8) the total bits are based on the remaining rows.

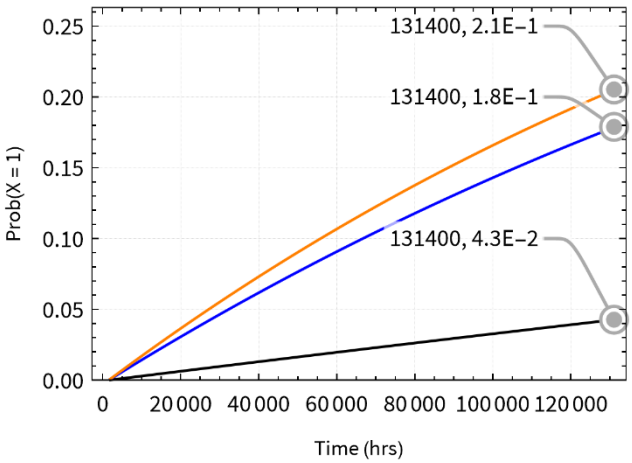

Figure 14a

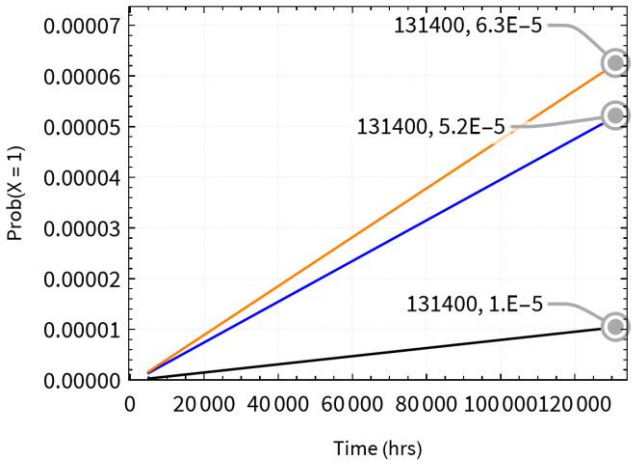

Figure 14b

Note:

Figure 14: Plot of probability of 1-bit error in a 8-bit (black), 40-bit (blue) or 48-bit (orange) word over time for (a) Rows 0 and 1 only using equation (7) and (b) all other rows using equation (8).

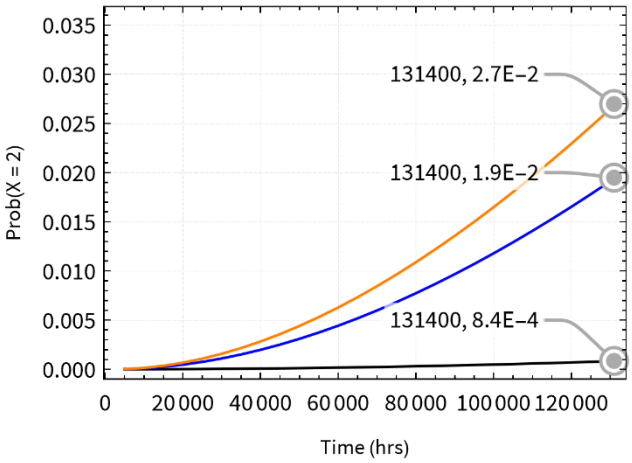

Figure 15a

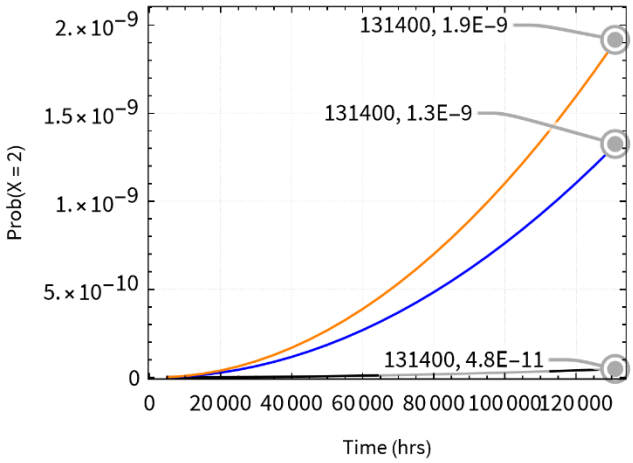

Figure 15b

Note:

Figure 15: Plot of probability of 2-bit errors in a 8-bit (black), 40-bit (blue) or 48-bit (orange) word over time for (a) Rows 0 and 1 only using equation (7) and (b) all other rows using equation (8).

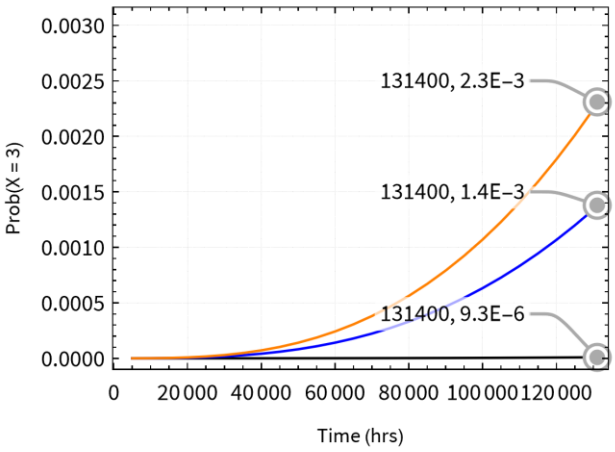

Figure 16a

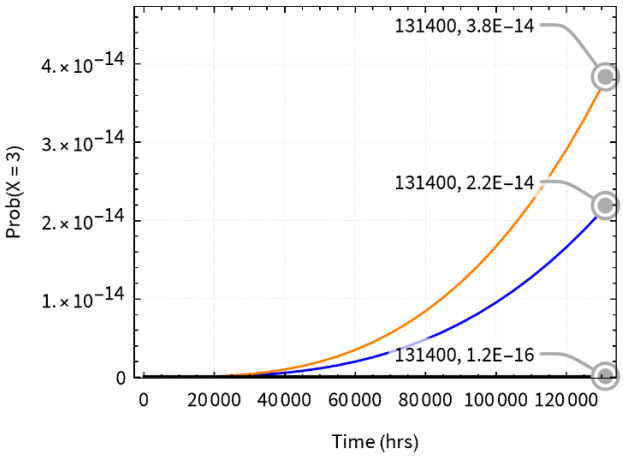

Figure 16b

Note:
Figure 16 Plot of probability of 3-bit errors in a 8-bit (black), 40-bit (blue) or 48-bit (orange) word over time for (a) Rows 0 and 1 only using equation (7) and (b) all other rows using equation (8).

Multi-Bit Errors

The following sections investigate the number of multi-bit errors occurrences within a word. A multi-bit error (MBE) is defined as when >= 2 bits occur within a given word size. Per the available data, only word sizes of 4-bits, 8-bits, and 48-bits were analyzed.

MBE in a 48-bit Word

Shown in Table 5 is the total number of MBEs that occurred at each read point for each device and each electrical test temperature for a 48-bit word. The 48-bit word is based on the 8 bits from the six die within the device. The maximum number of bit errors for any MBE is 2 bits.

Table 5: Summary of Number of MBE Occurrences for a 48-bit Word

Lot#_SN	Electrical Test Temperature(°C)	RP0	RP1	RP2	RP3	RP4	RP5	PR6	PR7	RP8
L3lki-rel_SN10.	-40	0	0	0	0	1	0	0	0	4
L3lki-rel_SN10.	25	0	0	0	0	0	0	0	0	5
L3lki-rel_SN10.	105	0	0	0	0	0	0	0	0	6
L3lki-rel_SN24.	-40	0	0	0	1	0	0	0	0	1
L3lki-rel_SN24.	25	0	0	0	0	0	0	0	0	3
L3lki-rel_SN24.	105	0	0	0	0	0	0	0	0	4

Lot#_SN	Electrical Test Temperature(°C)	RP0	RP1	RP2	RP3	RP4	RP5	PR6	PR7	RP8
L3lkm-rel_SN138.	105	0	0	0	0	0	0	0	1	6
L3lkm-rel_SN138.	-40	0	0	0	0	0	0	0	0	2
L3lkm-rel_SN138.	25	0	0	0	0	0	0	0	0	5
L3lkm-rel_SN2.	25	0	0	0	0	0	0	0	1	2
L3lkm-rel_SN2.	105	0	0	0	0	0	0	0	1	3
L3lkm-rel_SN2.	-40	0	0	0	0	0	0	0	0	2
L3lkm-rel_SN25.	105	0	0	0	0	0	0	0	1	1

MBE in an 8-bit Word

Shown in the table below is the total number of MBEs that occurred at each read point for each device and each electrical test temperature for an 8-bit word. The maximum number of bit errors for any MBE is 2 bits.

Table 6: Summary of Number of MBE Occurrences for a 8-bit Word

Lot#_SN	Electrical Test Temperature (°C)	RP0	RP1	RP2	RP3	RP4	RP5	PR6	PR7	RP8
L3lki-rel_SN10.	-40	0	0	0	0	1	0	0	0	4
L3lki-rel_SN10.	25	0	0	0	0	0	0	0	0	5
L3lki-rel_SN10.	105	0	0	0	0	0	0	0	0	6
L3lki-rel_SN24.	-40	0	0	0	1	0	0	0	0	1
L3lki-rel_SN24.	25	0	0	0	0	0	0	0	0	3
L3lki-rel_SN24.	105	0	0	0	0	0	0	0	0	4
L3lkm-rel_SN138.	105	0	0	0	0	0	0	0	1	6
L3lkm-rel_SN138.	-40	0	0	0	0	0	0	0	0	2
L3lkm-rel_SN138.	25	0	0	0	0	0	0	0	0	5
L3lkm-rel_SN2.	25	0	0	0	0	0	0	0	1	2
L3lkm-rel_SN2.	105	0	0	0	0	0	0	0	1	3
L3lkm-rel_SN2.	-40	0	0	0	0	0	0	0	0	2
L3lkm-rel_SN25.	105	0	0	0	0	0	0	0	1	1

In comparing Table 5 and Table 6, the results indicate that the MBEs in the 48-bit word are isolated to 8-bits segments.

MBE in a 4-bit (Nibble)

Shown in Table 7 is the total number of MBEs that occurred at each read point for each device and each electrical test temperature for a 4-bit word. The maximum number of bit errors for any MBE is 2 bits.

The four bits for a nibble are defined as:

- N1 = DQ0, 1, 2, 3
- N2 = DQ4, 5, 6, 7

Table 7: Summary of Number of MBE Occurrences for a 4-bit Word

Lot#_SN	Electrical Test Temperature(°C)	Nibble	RP0	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8
L3lki-rel_SN10.	-40	N1	0	0	0	0	2	0	0	0	0

Conclusion

This technical note provides a summary of bit errors observed during temperature accelerated stress testing of the UT8SDMQ64M48. It was observed that the bit errors increase over time. From the data, a lifetime predictive model was developed for estimating the bit errors as a function of time and temperature. Additionally, the linear model was utilized to illustrate the change in the error probability over time. Furthermore, the linear model was using in combination with a binomial distribution to predict the probability of bit errors within a 48-bit word for 1, 2, and 3 bit errors.

Revision History

Date	Revision #	Author	Change Description	Page #
05/17/2022	1.0	AW/NG/ML	Initial Release	
05/26/2022	1.1	AW	Updated Table 2 by increasing the rates by 4x to reflect the final error rates that are possible; Updated Figure 11 with the correct error value as shown on the figure.	
06/09/2022	1.2	AW	Change the bit errors from 5518 to 5497 in section 4.3.	
02/25/2025	1.3	AW	Updated report based on additional data from new read points up to 4000 hours; Updated probability plots to include 8-bit and 40-bit estimations; Added sections on MBEs for die level and bank level as observed from the data; Added table listing the linear regression coefficient for each device.	

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time

	Definition
	without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

Appendix A.

Table A.1 Frequency Table for Rows with Bit Errors

Row	Frequency	% of Total	Total Cumulative (%)
0	280	27.424	27.424
1	259	25.367	52.791
2	19	1.861	54.652
3	22	2.155	56.807
4	3	0.294	57.101
5	3	0.294	57.395
16	2	0.196	57.591
17	3	0.294	57.884
33	1	0.098	57.982
37	1	0.098	58.080
38	16	1.567	59.647
39	18	1.763	61.410
40	6	0.588	61.998
41	4	0.392	62.390
128	3	0.294	62.684
129	3	0.294	62.977
170	6	0.588	63.565
171	6	0.588	64.153
272	1	0.098	64.251
273	1	0.098	64.349
274	3	0.294	64.643
275	3	0.294	64.936
430	8	0.784	65.720
431	1	0.098	65.818
644	2	0.196	66.014
645	3	0.294	66.308
650	4	0.392	66.699
651	5	0.490	67.189
760	1	0.098	67.287
761	1	0.098	67.385

Row	Frequency	% of Total	Total Cumulative (%)
782	3	0.294	67.679
783	6	0.588	68.266
784	14	1.371	69.638
785	13	1.273	70.911
786	4	0.392	71.303
787	3	0.294	71.596
806	3	0.294	71.890
807	3	0.294	72.184
1016	1	0.098	72.282
1017	1	0.098	72.380
1018	3	0.294	72.674
1019	3	0.294	72.968
1288	3	0.294	73.262
1289	3	0.294	73.555
1940	3	0.294	73.849
1941	3	0.294	74.143
2048	13	1.273	75.416
2049	11	1.077	76.494
2150	8	0.784	77.277
2151	6	0.588	77.865
3144	1	0.098	77.963
3145	2	0.196	78.159
3146	6	0.588	78.746
3147	3	0.294	79.040
3149	1	0.098	79.138
3772	3	0.294	79.432
3773	4	0.392	79.824
3775	1	0.098	79.922
4096	17	1.665	81.587
4097	17	1.665	83.252
4394	1	0.098	83.350
4395	2	0.196	83.546
4580	2	0.196	83.741

Row	Frequency	% of Total	Total Cumulative (%)
4581	2	0.196	83.937
4590	3	0.294	84.231
4591	3	0.294	84.525
5118	25	2.449	86.974
5119	25	2.449	89.422
5341	1	0.098	89.520
5384	1	0.098	89.618
5385	1	0.098	89.716
5420	3	0.294	90.010
5421	3	0.294	90.304
6446	3	0.294	90.597
6447	3	0.294	90.891
6536	22	2.155	93.046
6537	24	2.351	95.397
6539	3	0.294	95.690
7168	3	0.294	95.984
7169	3	0.294	96.278
7304	1	0.098	96.376
7306	13	1.273	97.649
7307	8	0.784	98.433
7517	7	0.686	99.119
7999	9	0.881	100.000

Table A.2 Bit Errors Per Die for Each Temperature from Bit Location Testing of the 6 Devices

Die	Temp	RP0	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8
D0	-40	0	2	3	3	7	8	8	14	38
D0	25	0	3	4	3	8	10	10	22	54
D0	105	4	4	5	4	10	10	10	29	68
D1	-40	3	2	1	9	0	0	0	0	2
D1	25	0	0	0	0	0	0	0	0	2
D1	105	0	0	0	0	0	0	0	2	3
D2	-40	1	2	2	9		4	4	7	52
D2	25	2	2	2	3	1	7	6	13	63

Die	Temp	RP0	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8
D2	105	2	2	2	4	2	8	9	20	89
D3	-40	0	2	0	0	0	4	1	6	27
D3	25	0	2	2	0	0	4	4	10	32
D3	105	0	2	4	2	2	7	7	14	47
D4	-40	5	7	4	8	9	6	6	14	49
D4	25	2	1	3	2	4	4	5	27	61
D4	105	2	1	4	2	4	4	8	36	81
D5	-40	0	0	0	0	4	4	4	14	34
D5	25	0	0	0	1	6	6	8	21	45
D5	105	0	0	0	4	7	8	10	33	70

Table A.3 Bit Errors Per Bank for Each Temperature from Bit Location Testing of the 6 Devices

Bank	Temp	RP0	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8
B0	-40	3	4	4	18	5	6	4	14	57
B0	25	0	3	4	2	8	6	8	25	71
B0	105	2	4	5	3	8	8	7	41	92
B1	-40	0	4	0	3	4	6	6	6	44
B1	25	0	4	0	3	4	8	6	9	58
B1	105	2	4	2	7	6	10	9	16	89
B2	-40	5	5	4	6	7	10	8	13	43
B2	25	2	0	2	1	3	10	13	22	51
B2	105	2	0	2	2	5	10	17	33	72
B3	-40	1	2	2	2	4	4	5	22	58
B3	25	2	1	5	3	4	7	6	37	77
B3	105	2	1	6	4	6	9	11	44	105