FRONTGRADE

DATASHEET

UT8QNF8M8

64Mbit NOR Flash Memory

4/25/2022

Version #: 1.0.0

Features

- 64Mbits organized as either 8M x 8-bits or 4M x16-bits
- Fast 60ns read/write access time
- Functionally compatible with traditional single power supply Flash devices
- Simultaneous read/write operations
- Flexible bank architecture
- Single 3.3V power supply
- Ultra low power consumption
- Near zero power standby operation
- Full HiRel temperature range (-40℃ to 105℃)
- Data retention > 20 years @ +90℃ (See Table 13)
- Programming Endurance: 10k cycles per sector
- Operational environment:
  - Total dose: 10 or 50 krad(Si)
  - SEL Immune: 80 MeV-cm^2/mg @ 105℃
  - SEU Immune: Memory Cell 102 MeV-cm^2/mg @25℃
- 48-pin ceramic flatpack package
- Standard Microelectronic Drawing (SMD), 5962-12204
  - QML Q and Q+

Introduction

The Frontgrade 64Mbit, 3.3 volt-only flash memory device, can be organized as 4,194,304 words of 16-bits each or 8,388,608 bytes of 8-bits each. Word mode data appears on DQ[15:0]; byte mode data appears on DQ[7:0]. The device is designed to be programmed in-system with the standard 3.3 volt V_{CC} supply and can also be programmed in standard PROM programmers. The device is available with an access time of 60 ns and is offered in a 48-pin ceramic flatpack package. Standard control pins—Chip Enable (CE#), Write Enable (WE#), and Output Enable (OE#)—control normal read and write operations, and avoid bus contention issues. The device operates from a single 3.3 volt power supply.

Application

The UT8QNF8M8 64Mbit Flash Memory is compatible for use with the UT699 LEON 3FT microprocessor. In a typical application, the microprocessor transfers an image of the application program or kernel from non-volatile memory, such as flash, to volatile memory, such as SRAM. The Frontgrade 64Mbit NOR Flash is intended to provide customers with a non volatile solution that has a memory capacity large enough to house a typical application program or kernel.

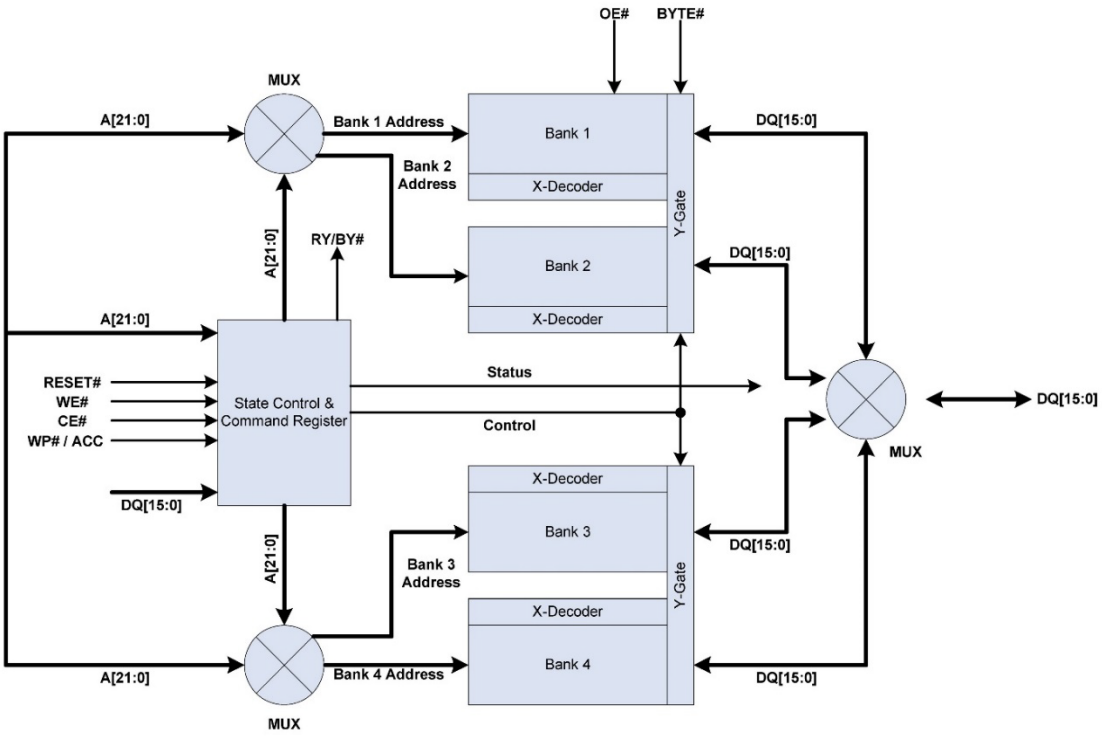


Figure 1: UT8QNF8M8 Flash Block Diagram

48-Lead Flatpack Top View

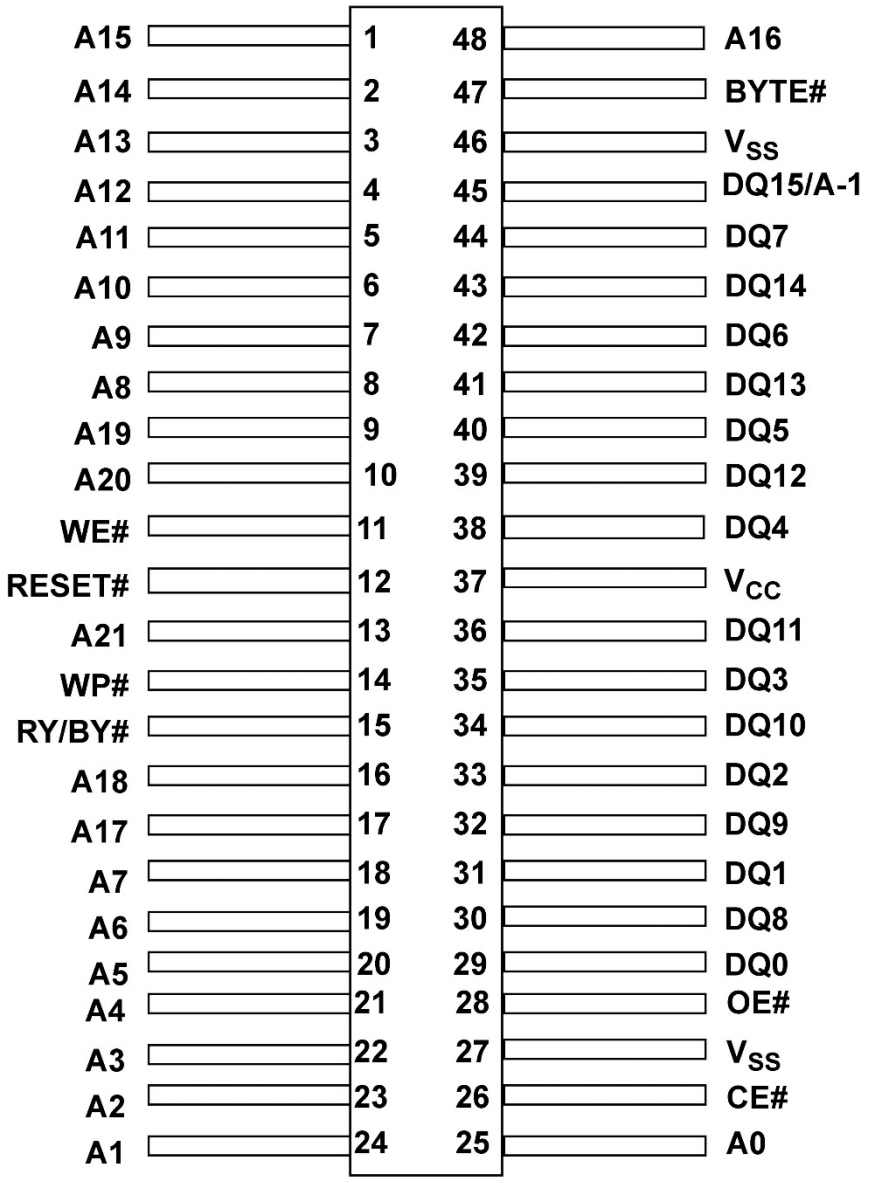


Figure 2: UT8QNF8M8 Pinout (48)

Table 1. Pin Descriptions

Signal	Function
A[21:0]	22 Address pins
DQ[14:0]	15 Data Inputs/Outputs, (x16-mode only)
DQ15/A-1	DQ15 (Data Input/Output, word mode), A-1 (LSB Address Input, byte mode)
CE#	Chip Enable, Active Low
OE#	Output Enable, Active Low
WE#	Write Enable, Active Low
WP#	Hardware Write Protect
RESET#	Hardware reset pin, Active Low
BYTE#	Select 8-bit or 16-bit mode, Active Low
RY/BY#	Ready/Busy Output, Active Low
V_{CC}	3.3 volt only single power supply (see supply tolerances)
V_{SS}	Device Ground

Simultaneous Read/Write Operations with Zero Latency

The Simultaneous Read/Write architecture provides simultaneous operation by dividing the memory space into four banks, two 8 Mb banks with small and large sectors, and two 24 Mb banks of large sectors. Sector addresses are fixed, system software can be used to form user-defined bank groups.

During an Erase/Program operation, any of the three non-busy banks may be read from. Note that only two banks can operate simultaneously. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from the other bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

The UT8QNF8M8 is organized as a dual boot device with both top and bottom boot sectors.

Table 2. Bank Architecture

Bank 1	8 Mb	Eight 8 kbyte/4 kword, Fifteen 64 kybte/32 word
Bank 2	24 Mb	Forty-eight 64 kbyte/32 kword
Bank 3	24 Mb	Forty-eight 64 kbyte/32 kword
Bank 4	8 Mb	Eight 8 kbyte/4 kword, Fifteen 64 kbyte/32 kword

UT8QNF8M8 Features

The device offers complete compatibility with the JEDEC 42.4 single-power-supply Flash command set standard. Commands are written to the command register using standard microprocessor write timings. Reading data out of the device is similar to reading from other Flash or EPROM devices.

The host system can detect whether a program or erase operation is complete by using the device status bits: RY/BY# pin, DQ7 (Data# Polling) and DQ6/DQ2 (toggle bits). After a program or erase cycle has been completed, the device automatically returns to the read mode. The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in sectors 0, 1, 140, and 141. The Erase Suspend/Erase Resume feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the automatic sleep mode. The system can also place the device into the standby mode. Power consumption is greatly reduced in both modes.

Device Bus Operation

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 3 lists the device bus operations, the inputs and control levels they require, and the resulting output.

Table 3. UT8QNF8M8 Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	WP#	Addresses 1	DQ[15:8]		DQ[7:0]
							BYTE# = V_{IH}	BYTE# = V_{IL}	
Read	L	L	H	H	L/H	AIN	D_{OUT}	DQ[14:8] = High-Z, DQ15 = A-1	D_{OUT}
Write	L	H	L	H	(Note 2)	AIN	D_{IN}		D_{IN}
Standby	V_{CC} ± 0.3V	X	X	V_{CC} ± 0.3V	L/H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	L/H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	L/H	X	High-Z	High-Z	High-Z

Notes:

1. Addresses are A21:A0 in word mode (BYTE# = V_{IH}), A21:A-1 in byte mode (BYTE# = V_{IL}).
2. If WP# = V_{IL}, sectors 0, 1, 140, and 141 remain protected.

Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins operate in the byte or word configuration. If the BYTE# pin is set at logic 1, the device is in word configuration, DQ[15:0] are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins [DQ7:0] are active and controlled by CE# and OE#. The data I/O pins [DQ14:8] are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function. The BYTE# pin must be connected to either the system V_{CC} or ground.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are altered.

Refer to Read-Only Operations for timing specifications and to Figure 7 for the timing diagram. ICC1 represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. Refer to Word/ Byte Configuration.

The device features an Unlock Bypass mode to facilitate faster programming. Once a bank enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. Byte/ Word Program Command Sequence has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 4 indicates the address space that each sector occupies. Similarly, a sector address is the address bits required to uniquely select a sector. Command Definitions section has details on erasing a sector or the entire chip, or suspending/ resuming the erase operation.

The device address space is divided into four banks. A bank address is the address bits required to uniquely select a bank.

I_{CC2} represents the active current specification for the write mode. AC Characteristics section contains timing specification tables and timing diagrams for write operations.

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register which is separate from the memory array on [DQ15:0]. Standard read cycle timings apply in this mode. Refer to the Autoselect Command Sequence section for more information.

Simultaneous Read/Write Operations with Zero Latency

This device is capable of reading data from one bank of memory while programming or erasing in another bank of memory. An erase operation may also be suspended to read from or program to another location within the same bank except the sector being erased. Figure 13 shows how read and write cycles may be initiated for simultaneous operation with zero latency.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at V_{CC} ± 0.3V. This is a more restricted voltage range than V_{IH}. If CE# and RESET# are held at V_{IH}, but not within V_{CC} ± 0.3V, the device will be in the standby mode, but the standby V_{IH} current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. ICC5 represents the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS} ±0.3V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS} ±0.3V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory. The CE# pin should only go to V_{IL} after RESET# has gone to V_{IH}. Keeping CE# at V_{IL} from power up through the first read could cause the first read to retrieve erroneous data.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a logic 0 (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is logic 1), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}. Refer to Hardware Reset section for reset# parameters and to Figure 8 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 4. UT8QNF8M8 Sector Architecture

Bank	Sector	Sector Address A21-A12	Sector Size (kbytes/kwords)	(x8) Address Range	(x16) Address Range
	SA0	000000000	8/4	000000h-001FFFh	00000h-00FFFh
	SA1	000000001	8/4	002000h-003FFFh	01000h-01FFFh
	SA2	000000010	8/4	004000h-005FFFh	02000h-02FFFh
	SA3	000000011	8/4	006000h-007FFFh	03000h-03FFFh
	SA4	000000100	8/4	008000h-009FFFh	04000h-04FFFh
	SA5	000000101	8/4	00A000h-00BFFFh	05000h-05FFFh
	SA6	000000110	8/4	00C000h-00DFFFh	06000h-06FFFh
	SA7	000000111	8/4	00E000h-00FFFFh	07000h-07FFFh
	SA8	000001xxx	64/32	010000h-01FFFFh	08000h-08FFFh
	SA9	000010xxx	64/32	020000h-02FFFFh	10000h-17FFFh
	SA10	000011xxx	64/32	030000h-03FFFFh	18000h-1FFFFh
Bank 1	SA11	000100xxx	64/32	040000h-04FFFFh	20000h-27FFFh
	SA12	000101xxx	64/32	050000h-05FFFFh	28000h-2FFFFh
	SA13	000110xxx	64/32	060000h-06FFFFh	30000h-37FFFh
	SA14	000111xxx	64/32	070000h-07FFFFh	38000h-3FFFFh
	SA15	001000xxx	64/32	080000h-08FFFFh	40000h-47FFFh
	SA16	001001xxx	64/32	090000h-09FFFFh	48000h-4FFFFh
	SA17	001010xxx	64/32	0A0000h-0AFFFFh	50000h-57FFFh
	SA18	001011xxx	64/32	0B0000h-0BFFFFh	58000h-5FFFFh

Bank	Sector	Sector Address A21-A12	Sector Size (kbytes/kwords)	(x8) Address Range	(x16) Address Range
	SA19	001100xxx	64/32	0C0000h-0CFFFFh	60000h-67FFFh
	SA20	001101xxx	64/32	0D0000h-0DFFFFh	68000h-6FFFFh
	SA21	001110xxx	64/32	0E0000h-0EFFFFh	70000h-77FFFh
	SA22	001111xxx	64/32	0F0000h-0FFFFFh	78000h-7FFFFh
	SA23	0010000xxx	64/32	100000h-10FFFFh	80000h-87FFFFh
	SA24	0010001xxx	64/32	110000h-11FFFFh	880000h-8FFFFh
	SA25	0010010xxx	64/32	120000h-12FFFFh	90000h-97FFFh
	SA26	0010011xxx	64/32	130000h-13FFFFh	980000h-9FFFFh
	SA27	0010100xxx	64/32	140000h-14FFFFh	A0000h-A7FFFh
	SA28	0010101xxx	64/32	150000h-15FFFFh	A8000h-AFFFFh
	SA29	0010110xxx	64/32	160000h-16FFFFh	B0000h-B7FFFh
	SA30	0010111xxx	64/32	170000h-17FFFFh	B8000h-BFFFFh
	SA31	0011000xxx	64/32	180000h-18FFFFh	C0000h-C7FFFh
	SA32	0011001xxx	64/32	190000h-19FFFFh	C8000h-8FFFFh
	SA33	0011010xxx	64/32	1A0000h-1AFFFFh	D0000h-D7FFFh
	SA34	0011011xxx	64/32	1B0000h-1BFFFFh	D8000h-DFFFFh
	SA35	0011000xxx	64/32	1C0000h-1CFFFFh	E0000h-E7FFFh
	SA36	0011101xxx	64/32	1D0000h-1DFFFFh	E8000h-EFFFFh
	SA37	0011110xxx	64/32	1E0000h-1EFFFFh	F0000h-F7FFFh
	SA38	0011111xxx	64/32	1F0000h-1FFFFFh	F8000h-FFFFFh
	SA39	0100000xxx	64/32	200000h-20FFFFh	100000h-107FFFh
	SA40	0100001xxx	64/32	210000h-21FFFFh	108000h-10FFFFh
	SA41	0100010xxx	64/32	220000h-22FFFFh	110000h-117FFFh
	SA42	0100011xxx	64/32	230000h-23FFFFh	118000h-11FFFFh
	SA43	0100100xxx	64/32	240000h-24FFFFh	120000h-127FFFh
	SA44	0100101xxx	64/32	250000h-25FFFFh	128000h-12FFFFh
	SA45	0100110xxx	64/32	260000h-26FFFFh	130000h-137FFFh
Bank 2	SA46	0100111xxx	64/32	270000h-27FFFFh	138000h-13FFFFh
	SA47	0101000xxx	64/32	280000h-28FFFFh	140000h-147FFFh
	SA48	0101001xxx	64/32	290000h-29FFFFh	148000h-14FFFFh

Bank	Sector	Sector Address A21-A12	Sector Size (kbytes/kwords)	(x8) Address Range	(x16) Address Range
	SA49	0101010xxx	64/32	2A0000h-2AFFFFh	150000h-157FFFh
	SA50	0101011xxx	64/32	2B0000h-2BFFFFh	158000h-15FFFFh
	SA51	0101100xxx	64/32	2C0000h-2CFFFFh	160000h-167FFFh
	SA52	0101101xxx	64/32	2D0000h-2DFFFFh	168000h-16FFFFh
	SA53	0101110xxx	64/32	2E0000h-2EFFFFh	170000h-177FFFh
	SA54	0101111xxx	64/32	2F0000h-2FFFFFh	178000h-17FFFFh
	SA55	0110000xxx	64/32	300000h-30FFFFh	180000h-187FFFh
	SA56	0110001xxx	64/32	310000h-31FFFFh	188000h-18FFFFh
	SA57	0110010xxx	64/32	320000h-32FFFFh	190000h-197FFFh
	SA58	0110011xxx	64/32	330000h-33FFFFh	198000h-19FFFFh
	SA59	0110100xxx	64/32	340000h-34FFFFh	1A0000h-1A7FFFh
	SA60	0110101xxx	64/32	350000h-35FFFFh	1A8000h-1AFFFFh
	SA61	0110110xxx	64/32	360000h-36FFFFh	1B0000h-1B7FFFh
	SA62	0110111xxx	64/32	370000h-37FFFFh	1B8000h-1BFFFFh
	SA63	0111000xxx	64/32	380000h-38FFFFh	1C0000h-1C7FFFh
	SA64	0111001xxx	64/32	390000h-39FFFFh	1C8000h-1CFFFFh
	SA65	0111010xxx	64/32	3A0000h-3AFFFFh	1D0000h-1D7FFFh
	SA66	0111011xxx	64/32	3B0000h-3BFFFFh	1D8000h-1DFFFFh
	SA67	0111100xxx	64/32	3C0000h-3CFFFFh	1E0000h-1E7FFFh
	SA68	0111101xxx	64/32	3D0000h-3DFFFFh	1E8000h-1EFFFFh
	SA69	0111110xxx	64/32	3E0000h-3EFFFFh	1F0000h-1F7FFFh
	SA70	0111111xxx	64/32	3F0000h-3FFFFFh	1F8000h-1FFFFFh
	SA71	1000000xxx	64/32	400000h-40FFFFh	200000h-207FFFh
	SA72	1000001xxx	64/32	410000h-41FFFFh	208000h-20FFFFh
	SA73	1000010xxx	64/32	420000h-42FFFFh	210000h-217FFFh
	SA74	1000011xxx	64/32	430000h-43FFFFh	218000h-21FFFFh
	SA75	1000100xxx	64/32	440000h-44FFFFh	220000h-227FFFh
	SA76	1000101xxx	64/32	450000h-45FFFFh	228000h-22FFFFh
	SA77	1000110xxx	64/32	460000h-46FFFFh	230000h-237FFFh
	SA78	1000111xxx	64/32	470000h-47FFFFh	238000h-23FFFFh

Bank	Sector	Sector Address A21-A12	Sector Size (kbytes/kwords)	(x8) Address Range	(x16) Address Range
	SA79	1001000xxx	64/32	480000h-48FFFFh	240000h-247FFFh
	SA80	1001001xxx	64/32	490000h-49FFFFh	248000h-24FFFFh
	SA81	1001010xxx	64/32	4A0000h-4AFFFFh	250000h-257FFFh
	SA82	1001011xxx	64/32	4B0000h-4BFFFFh	258000h-25FFFFh
	SA83	1001100xxx	64/32	4C0000h-4CFFFFh	260000h-267FFFh
	SA84	1001101xxx	64/32	4D0000h-4DFFFFh	268000h-26FFFFh
	SA85	1001110xxx	64/32	4E0000h-4EFFFFh	270000h-277FFFh
	SA86	1001111xxx	64/32	4F0000h-4FFFFFh	278000h-27FFFFh
	SA87	1010000xxx	64/32	500000h-50FFFFh	280000h-28FFFFh
	SA88	1010001xxx	64/32	510000h-51FFFFh	288000h-28FFFFh
	SA89	1010010xxx	64/32	520000h-52FFFFh	290000h-297FFFh
	SA90	1010011xxx	64/32	530000h-53FFFFh	298000h-29FFFFh
	SA91	1010100xxx	64/32	540000h-54FFFFh	2A0000h-2A7FFFh
	SA92	1010101xxx	64/32	550000h-55FFFFh	2A8000h-2AFFFFh
	SA93	1010110xxx	64/32	560000h-56FFFFh	2B0000h-2B7FFFh
Bank 3	SA94	1010111xxx	64/32	570000h-57FFFFh	2B8000h-2BFFFFh
	SA95	1011000xxx	64/32	580000h-58FFFFh	2C0000h-2C7FFFh
	SA96	1011001xxx	64/32	590000h-59FFFFh	2C8000h-2CFFFFh
	SA97	1011010xxx	64/32	5A0000h-5AFFFFh	2D0000h-2D7FFFh
	SA98	1010101xxx	64/32	5B0000h-5BFFFFh	2D8000h-2DFFFFh
	SA99	1011100xxx	64/32	5C0000h-5CFFFFh	2E0000h-2E7FFFh
	SA100	1011101xxx	64/32	5D0000h-5DFFFFh	2E8000h-2EFFFFh
	SA101	1011110xxx	64/32	5E0000h-5EFFFFh	2F0000h-2F7FFFh
	SA102	1011111xxx	64/32	5F0000h-5FFFFFh	2F8000h-2FFFFFh
	SA103	1100000xxx	64/32	600000h-60FFFFh	300000h-307FFFh
	SA104	1100001xxx	64/32	610000h-61FFFFh	308000h-30FFFFh
	SA105	1100010xxx	64/32	620000h-62FFFFh	310000h-317FFFh
	SA106	1100011xxx	64/32	630000h-63FFFFh	318000h-31FFFFh
	SA107	1100100xxx	64/32	640000h-64FFFFh	320000h-327FFFh
	SA108	1100101xxx	64/32	650000h-65FFFFh	328000h-32FFFFh

Bank	Sector	Sector Address A21-A12	Sector Size (kbytes/kwords)	(x8) Address Range	(x16) Address Range
	SA109	1100110xxx	64/32	660000h-66FFFFh	330000h-337FFFh
	SA110	1101111xxx	64/32	670000h-67FFFFh	338000h-33FFFFh
	SA111	1101000xxx	64/32	680000h-68FFFFh	34000h-347FFFh
	SA112	1011101xxx	64/32	690000h-69FFFFh	348000h-34FFFFh
	SA113	1101010xxx	64/32	6A0000h-6AFFFFh	350000h-357FFFh
	SA114	1101011xxx	64/32	6B0000h-6BFFFFh	358000h-35FFFFh
	SA115	1101100xxx	64/32	6C0000h-6CFFFFh	36000h-367FFFh
	SA116	1101101xxx	64/32	6D0000h-6DFFFFh	368000h-36FFFFh
	SA117	1101110xxx	64/32	6E0000h-6EFFFFh	37000h-377FFFh
	SA118	1101111xxx	64/32	6F0000h-6FFFFFh	37800h-37FFFFh
	SA119	1110000xxx	64/32	700000h-70FFFFh	380000h-387FFFh
	SA120	1110001xxx	64/32	710000h-71FFFFh	388000h-38FFFFh
	SA121	1110010xxx	64/32	720000h-72FFFFh	390000h-397FFFh
	SA122	1110011xxx	64/32	730000h-73FFFFh	39800h-39FFFFh
	SA123	1110100xxx	64/32	740000h-74FFFFh	3A0000h-3A7FFFh
	SA124	1110101xxx	64/32	750000h-75FFFFh	3A8000h-3AFFFFh
	SA125	1110110xxx	64/32	760000h-76FFFFh	3B0000h-3B7FFFh
	SA126	1110111xxx	64/32	770000h-77FFFFh	3B8000h-3BFFFFh
	SA127	1111000xxx	64/32	780000h-78FFFFh	3C0000h-3C7FFFh
	SA128	1111001xxx	64/32	790000h-79FFFFh	3C8000h-3CFFFFh
	SA129	1111010xxx	64/32	7A0000h-7AFFFFh	3D0000h-3D7FFFh
Bank 4	SA130	1110101xxx	64/32	7B0000h-7BFFFFh	3D8000h-3DFFFFh
	SA131	1111100xxx	64/32	7C0000h-7CFFFFh	3E80000h-3E7FFFh
	SA132	1111110xxx	64/32	7D0000h-7DFFFFh	3E8000h-3EFFFFh
	SA133	1111110xxx	64/32	7E0000h-7EFFFFh	3F0000h-3F7FFFh
	SA134	1111111000	8/4	7F0000h-7F1FFFh	3F8000h-3F8FFFh
	SA135	1111111001	8/4	7F2000h-7F3FFFh	3F9000h-3F9FFFh
	SA136	1111111010	8/4	7F4000h-7F5FFFh	3FA000h-3FAFFFh
	SA137	1111111011	8/4	7F6000h-7F7FFFh	3FB000h-3FBFFFh
	SA138	1111111100	8/4	7F8000h-7F9FFFh	3FC000h-3FCFFFh

Bank	Sector	Sector Address A21-A12	Sector Size (kbytes/kwords)	(x8) Address Range	(x16) Address Range
	SA139	1111111101	8/4	7FA000h-7FBFFFh	3FD000h-3FDFFFh
	SA140	1111111110	8/4	7FC000h-7FDFFFh	3FE000h-3FEFFFh
	SA141	1111111111	8/4	7FE000h-7FFFFFh	3FF000h-3FFFFFh

Table 5. Bank Address

Bank	A21-A19
1	000
2	001, 010, 011
3	100, 101, 110
4	111

Write Protect (WP#)

The Write Protect function provides a hardware method of protecting. If the system asserts V_{IL} on the WP# pin, the device disables program and erase functions in sectors 0, 1, 140, and 141. WP# pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Table 6. WP# Modes

VIL	Disables programming and erasing in SA0,SA1, SA140, SA141
V_{IH}	Enables programming and erasing in SA0, SA1, SA140, SA141.

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes. Refer to Table 11 for command definitions. In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up

Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 7 to Table 10. To terminate reading CFI data, the system must write the reset command. The CFI Query mode is not accessible when the device is executing an Embedded Program or embedded Erase algorithm.

The system can also write the CFI query command when the device is in the autoselect mode via the command register only (high voltage method does not apply). The device enters the CFI query mode, and the system can read CFI data at the addresses given in Table 7 to Table 10. The system must write the reset command to return to reading array data.

Table 7. CFI Query Identification String

Addresses (word mode)	Addresses (byte mode)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query unique ASII string "QRY"
13h 14h	26h 28h	002h 000h	Primary OEM command set
15h 16h	2Ah 2Ch	0040h 0000h	Address for primary extended table

Addresses (word mode)	Addresses (byte mode)	Data	Description
17h 18h	2Eh 30h	000h 000h	Alternate OEM command set (00h = none exists
19h 1Ah	32h 34h	000h 000h	Address for alternate OEM extended table (00h = none exists

Table 8. System Interface String

Addresses (word mode)	Addresses (byte mode)	Data	Description
1Bh	36h	0027h	V_{CC} min (write/erase) D7-D4: volt, D3-D0:100 millivolt
1Ch	38h	0036h	V_{CC} max (write/erase) D7-D4: volt, D3-D0:100 millivolt
1Dh	3Ah	0000h	V_{PP} min, voltage (00h=no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} max, voltage (00h=no V_{PP} pin present)
1Fh	3Eh	0003h	Typical timeout per single byte/word write 2^N µs
20h	40h	0000h	Typical timeout per min. size buffer write 2^N µs (00h = not supported)
21h	42h	0009h	Typical timeout per individual block erase 2^N ms
22h	44h	000Fh	Typical timeout per full chip erase 2^N ms (00h = not supported)
23h	46h	0004h	Max timeout for byte/word 2^N times typical
24h	48h	0000h	Max timeout per buffer write 2^N times typical
25h	4Ah	0004h	Max timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max timeout for full chip erase 2^N times typical support (00h = not supported)

Table 9. Device Geometry Definition

Addresses (word mode)	Addresses (byte mode)	Data	Description
27h	4Eh	0017h	Device size = 2^N byte
28h 29h	50h 52h	0002h 0000h	Flash device interface description
2Ah 2Bh	54h 56h	0000h 0000h	Max number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	0003h	Number of erase block regions within device

Addresses (word mode)	Addresses (byte mode)	Data	Description
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	0007h 0000h 0020h 0000H	Erase block region 1 information
31h 32h 33h 34h	62h 64h 66h 68h	007Dh 0000h 0000h 0001h	Erase block region 2 information
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0007h 0000h 0020h 0000h	Erase block region 3 information
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase block region 4 information

Table 10. Primary Vendor-Specific Extended Query

Addresses (word mode)	Addresses (byte mode)	Data	Description
40h 41h 42h	80h 82h 84h	050h 052h 049h	Query-unique ASCII string "PRI"
43h	86h	031h	Major version number, ASCII (reflects modifications to the silicon)
44h	88h	033h	Major version number, ASCII (reflects modifications to the CFI table)
45h	8Ah	00C0h	Address sensitive unlock (Bits 1-0) 0 = required 1 = not required Process technology (Bits 7-2) 0011 = 0.11 µm floating gate
46h	8Ch	0002h	Erase suspend 0 = not supported 1 = to read only 2 = to read & write
47h	8Eh	0001h	Sector protect 0 = not supported X = number of sectors per group
48h	90h	0001h	Sector temporary unprotected 00 = not supported 01 = supported

Addresses (word mode)	Addresses (byte mode)	Data	Description
49h	92h	0004h	Sector protect/ unprotected scheme 01 = 29F040 mode, 02 = 29F016 mode, 03 = 29F0400 04 = 29LV800 mode
4Ah	94h	0007h	Simultaneous operation 0 = not supported X = number of sectors (excluding Bank 1)
4Bh	96h	0000h	Burst mode type 00 = not supported 01 = supported
4Ch	98h	0000h	Page mode type 00 = not supported 01 = 4 word page 02 = 8 word page
4Dh	9Ah	00xxh	Reserved
4Eh	9Ch	00xxh	Reserved
4Fh	9Eh	0001h	Top/bottom boot sector flat 00h = uniform device, 01h = 8 x 8 kbyte sectors, top and bottom boot with write protect, 02h = bottom boot device, 03h = top boot device, 04h = both top and bottom
50h	A0h	0000h	Program suspend 0 = not supported, 01 = supported
57h	AEh	0004h	Bank organization 00 = Data at 4Ah is zero, X = number of banks
58h	B0h	0017h	Bank 1 region information X = number of sectors in bank 1
59h	B2h	0030h	Bank 2 region information X = number of sectors in bank 2
5Ah	B4h	0030h	Bank 3 region information X = number of sectors in bank 3
5Bh	B6h	0017h	Bank 4 region information X = number of sectors in bank 4

Command Definitions

Writing specific address and data sequences into the command register initiates device operations. Table 11 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to AC Characteristics for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspended mode, after which the system can read data from any non-erase-suspended sector within the same bank. The system can read array data using the standard read timing, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See Erase Suspend/Erase Resume Commands for more information.

The system must issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See Reset Command for more information.

See Requirements for Reading Array Data or more information. Read-Only Operations provides the read parameters, and Figure 7 shows the timing diagram.

Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don’t cares for this command. The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the Autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the bank to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend). The RY/BY# signal remains low until this reset is issued.

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend read mode. The autoselect command may not be written while the device is actively programming or erasing in another bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. The system may read any number of autoselect codes without re-initiating the command sequence.

Table 11 shows the address and data requirements. To determine sector protection information, the system must write to the appropriate bank address (BA) and sector address (SA). Table 4 shows the address range and bank number associated with each sector. The system must write the reset command to return to the read mode or erase suspend-read mode if the bank was previously in Erase Suspend.

Byte/Word Program Command Sequence

The system may program the device by word or byte, depending on the state of the BYTE# pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 11 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. Refer to Write Operation Status for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. A hardware reset immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity. The autoselect and CFI functions are unavailable when a program operation is in progress. Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from 0 back to a 1. Attempting to do so may cause that bank to set DQ5 to a logic 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read shows that the data is still 0. Only erase operations can convert a 0 to a 1.

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes or words to a bank faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. That bank then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 11 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. See Table 11.

Figure 3 illustrates the algorithm for the program operation. Refer to Erase and Program Operations for parameters, and Figure 11 for timing diagrams.

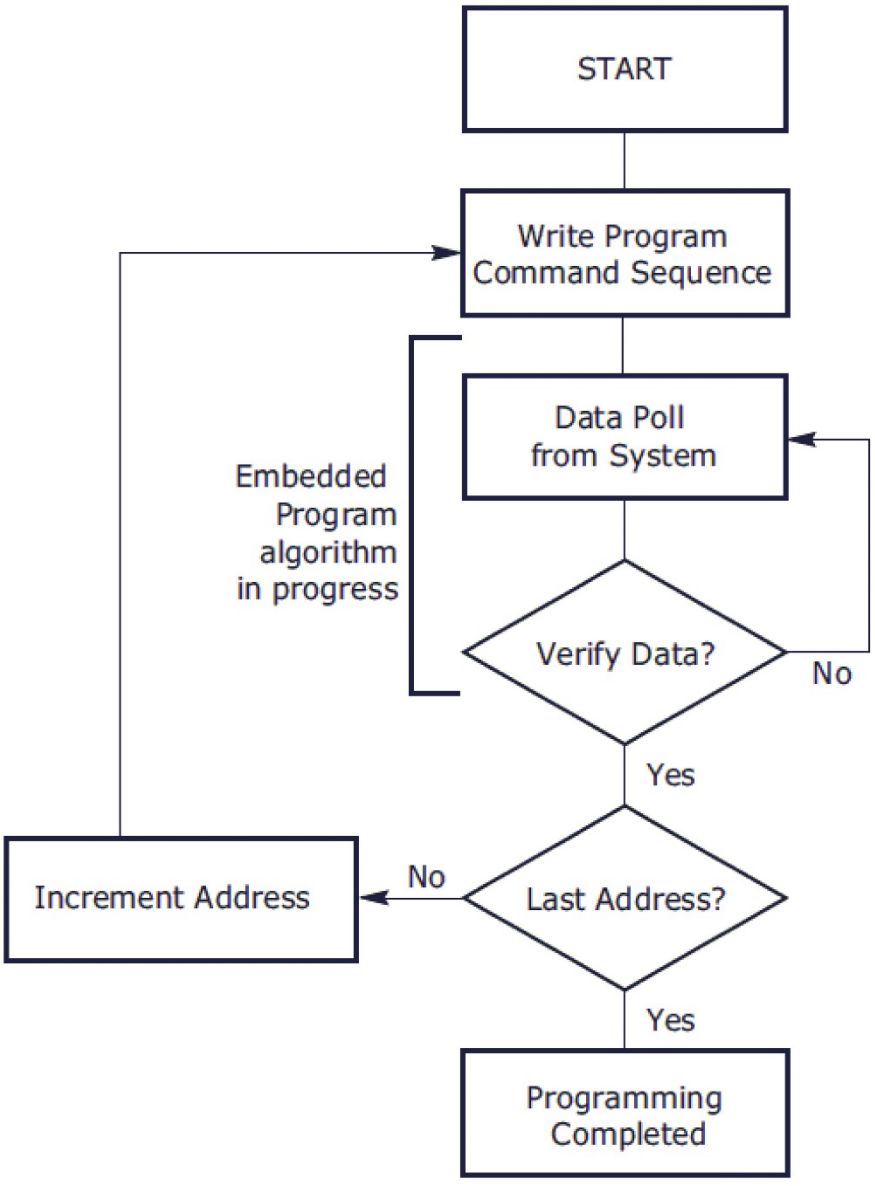


Figure 3: Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 11 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/ BY#. Refer to Write Operation Status section for detailed information on these status bits.

Any commands written during the chip erase operation are ignored. However, a hardware reset immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity. CFI functions are unavailable when an erase operation is in progress.

Figure 4 illustrates the algorithm for the erase operation. Refer to Erase and Program Operations for parameters, and Figure 9 for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 11 shows the address and data requirements for the sector erase command sequence.

The device does not require the system to pre-program prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 80µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 80µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If any command other than 30h, B0h, F0h is input during the time-out period, the normal operation will not be guaranteed. The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer.). The time-out begins from the rising edge of the final WE# or CE# pulse (first rising edge) in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. While the Embedded Erase operation is in progress, the system can read data from the non-erasing bank. The system can determine the status of the erase operation by reading DQ7, DQ6, DQ2, or RY/BY# in the erasing bank. Refer to Operation Status for more information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, a hardware reset immediately terminates the erase operation. If that occurs, the sector erase command

sequence should be reinitiated once that bank has returned to reading array data to ensure data integrity. CFI functions are unavailable when an erase operation is in progress.

Figure 4 illustrates the algorithm for the erase operation. Refer to Erase and Program Operations on for parameters, and Figure 12 for timing diagrams.

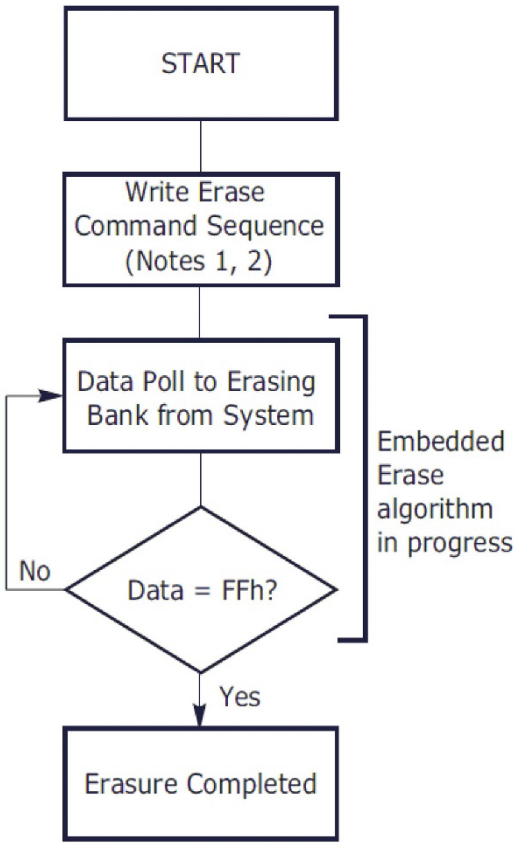


Figure 4: Erase Operation

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the 80µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. The bank address must contain one of the sectors currently selected for erase.

When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 35µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. The device erase suspends all sectors selected for erasure. Reading at any address within erase suspended sectors produces status information on [DQ7:0]. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase suspended. Refer to Write Operation Status for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard Byte Program operation.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. Refer to Autoselect Command Sequence for details.

To resume the sector erase operation, the system must write the Erase Resume command. The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Table 11. Command Definitions

Command Sequence			Cycles	Bus Cycles											
				First		Second		Third		Fouth		Fifth		Sixth	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read			1	RA	RD										
Reset			1	XXX	F0										
Autoselect	Manufacturer ID	Word	4	555	AA	2AA	55	(BA)555	90	(BA)555	01				
		Byte		AAA		555		(BA)AAA							
	Device ID	Word	6	555	AA	2AA	55	(BA)555	90	(BA)X01	7E	(BA)X0E	02	(BA)X0F	01
		Byte		AAA		555		(BA)AAA		(BA)X02		(BA)X1C		(BA)X1E	
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Unlock Bypass		Word	3	555	AA	2AA	55	555	20						
		Byte		AAA		555		AAA							
Unlock Bypass Program			2	XXX	A0	PA	PD								
Unlock Bypass Reset			2	XXX	90	XXX	00								
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
		Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
		Byte		AAA		555		AAA		AAA		555			
Erase Suspend			1	BA	B0										
Erase Resume			1	BA	30										
CFI Query		Word	1	55	98										
		Byte		AAA											

Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 12 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1µs, then that bank returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a 0 on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a 1 on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 3 ms, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at [DQ15:0] (or

[DQ7:DQ0] for x8-only mode) on the following read cycles. Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with [DQ15:8] (or DQ7:0 for x8-only mode) while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on [DQ15:0] may be still invalid. Valid data on [DQ15:0] (or [DQ7:0] for x8-only mode) will appear on successive read cycles.

Table 12 shows the outputs for Data# Polling on DQ7. Figure 5 shows the Data# Polling algorithm. Figure 14 shows the Data# Polling timing diagram.

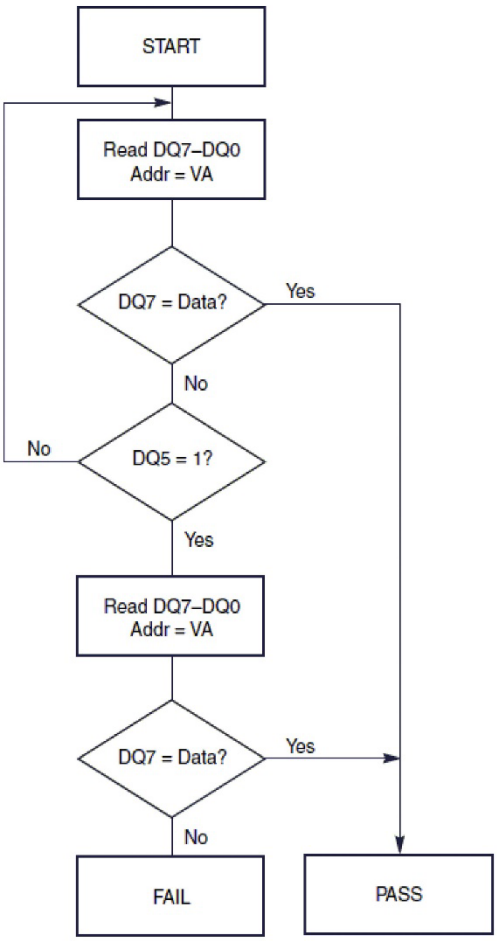


Figure 5: Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. This includes programming in the Erase Suspend mode. If the output is high (Ready), the device is in the read mode, the standby mode, or one of the banks is in the erase-suspend-read mode. Table 12 shows the outputs for RY/BY#.

When DQ5 is set to a logic 1, RY/BY# will be in the BUSY state, or a logic 0.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation) and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 3 ms, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7.

If a program address falls within a protected sector, DQ6 toggles for approximately 1µs after the program command sequence is written, then returns to reading array data. DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

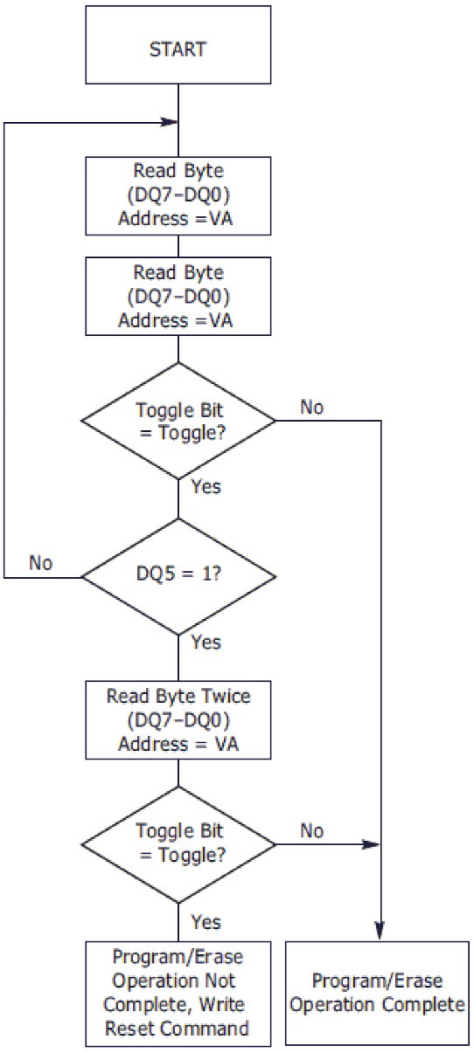


Figure 6: Toggle Bit Algorithm

DQ2: Toggle Bit II

The Toggle Bit II on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing. That is, the Embedded Erase algorithm is in progress, or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. The system may use either OE# or CE# to control the read cycles. DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information.

Figure 6 shows the toggle bit algorithm in flowchart form. Figure 15 shows the toggle bit timing diagram. Figure 16 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Whenever the system initially begins reading toggle bit status, it must read [DQ15:0] (or[DQ7:0] for x8-only mode) at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on [DQ15:0] (or [DQ7:0] for x8-only mode) on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high. If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation. Please refer to Figure 6.

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a 1, indicating that the program or erase cycle was not successfully completed.

The device may output a 1 on DQ5 if the system tries to program a 1 to a location that was previously programmed to 0. Only an erase operation can change a 0 back to a 1. Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a 1. Under both these conditions, the system must write the reset command to return to the read mode or to the erase-suspend-read mode if a bank was previously in the erasesuspend-program mode.

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. The sector erase timer does not apply to the chip erase command. If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a 0 to a 1. If the time between additional sector erase commands from the system can be assured to be less than 50µs, the system need not to monitor DQ3. Refer to Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is 1, the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is 0, the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. The RY/BY# pin will be in the BUSY state under this condition.

Table 12 shows the status of DQ3 relative to the other status bits.

Table 12: Write Operation Status

Status			DQ7	DQ6	DQ5	DQ3	DQ2	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	In busy erasing sector	0	Toggle	0	1	Toggle	0
		In not busy erasing sector	0	Toggle	0	1	No toggle	0
Erase Suspend Mode	Erase-Suspend-Read	Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A	0

Special Handling and Device Information

The UT8QNF8M8 64Mbit flash memory device does not receive radiographic inspection from Frontgrade. Frontgrade will not warrant devices that receive radiographic inspections. Devices are delivered in the all F's (erased) state.

Table 13: Endurance and Retention

Paramater	Condition	Limit	Units
Minimum data retention [1,2]	T_C=105°C	5	Years
	T_C=90°C	21	
	T_C=75°C	85	
	T_C=60°C	350	
Minimum endurance	T_C=-40°C to 105°C	10k	Cycles per sector

Note:

1. Data retention table is predicted on initial user programmed cycle of the device.
2. To achieve optimal data retention performance, Frontgrade recommends users perform "Double Programming". Please reference Frontgrade application note, Double Programming for High Reliability Systems.

Operational Environment

Parameter	Limit	Units
Total Ionizing Dose (TID) [3]	10 or 50	krad(Si)
Single Event Latchup (SEL) [1]	≤80	MeV-cm²/mg @ 105℃
Single Event Upset (SEU) [2]	≤102	MeV-cm²/mg @ 25℃

Notes:

1. The UT8QNF8M8 will not latch up during radiation exposure under recommended operating conditions.
2. 90% worst case particle environments, geosynchronous orbit, 100 Mils of aluminum.
3. Irradiated per MIL-STD-883 Method 1019 Condition C at 50-300 krad(Si) using an in-situ 900 rad(Si) device unpowered and 100 rad(Si) device statistically biased duty cycle repeated 50 times to achieve a TID level of 50 krad(Si). This irradiation in- situ biasing method is predicated on an application which may allow the device to be unpowered during 90% of the mission life.

Absolute Maximum Ratings[1]

(Referenced to VSS)

Symbol	Parameter	Limits
T_{STG}	Storage temperature	-65℃ to +150℃
V_{CC}	DC Supply voltage	-0.3V to +4.0V
V_{IO}	Voltage on any pin	-0.3V to V_{CC} +0.3V
I_{OS} [2]	Output short circuit current	200 mA
I_I	DC input current	+10 mA
ΘJC	Thermal resistance, junction to case	8 ℃/W
P_D	Power dissipation permitted at Tc=105℃	1 W
T_J	Maximum junction temperature	+150℃
ESD_{HBM} [3]	ESD Rating	2000V

Notes:

1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.
2. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
3. Meets ESD testing per MIL-STD-883, Method 3015, Class 2.

Recommended Operating Conditions

Symbol	Parameter	Limits
T_C	Operating case temperature	-40 to +105°C
V_{CC}	Operating supply voltage	3.0V to 3.6V
V_{IN}	DC input voltage	V_{SS} to V_{CC}

DC Electrical Characteristics

V_{CC} = 3.3V ± 0.3V; -40°C ≤ T_C ≤ +105°C

Symbol	Parameter	Condition		MIN	MAX	Unit
I_{IN}	Input leakage current	VIN = V_{SS} to V_{CC}, V_{CC} = V_{CC} max			±1.0	µA
I_{OZ}	Output leakage current	VOUT = V_{SS} to V_{CC}, V_{CC} = V_{CC} max, OE# = V_{IH}			±1.0	µA
I_{CC1} [1]	V_{CC} active read current	CE# = V_{IL}, OE# = V_{IH}, Byte Mode	5MHz		16	mA
			1 MHz		4	mA
		CE# = V_{IL}, OE# = V_{IH}, Word Mode	5 MHz		16	mA
			1 MHz		4	mA
I_{CC2} [1, 2]	V_{CC} active write current/erase current	CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IL}			30	mA
I_{CC3} [1, 4]	V_{CC} standby current	CE#, RESET# = V_{CC} ± 0.3V	Room & -40°C		5	µA
			105°C		20	µA
I_{CC4} [1, 4]	V_{CC} reset current	RESET# = V_{SS} ± 0.3V	Room & -40°C		5	µA
			105°C		20	µA
I_{CC5} [1, 3, 4]	Automatic sleep mode	V_{IH} = V_{CC} ± 0.3V; V_{IL} = V_{SS} ± 0.3V;	Room & -40°C		5	µA
			105°C		20	µA
V_{IH}	Input high voltage			2.1		V
V_{IL}	Input low voltage				0.8	V
V_{OL}	Output low voltage	I_{OL} = 2.0 mA, V_{CC} = V_{CC} min			0.45	V
V_{OH1}	Output high voltage	I_{OH} = 2.0 mA, V_{CC} = V_{CC} min		2.4		V
V_{OH2}	Output high voltage	I_{OH} = 100 µA, V_{CC} = V_{CC} min		V_{CC}-0.4		V
V_{LKO} [5]	Low V_{CC} lock-out voltage				1.8	V

Notes:

1. Maximum ICC specifications are tested with V_{CC} = V_{CC}max.
2. ICC active while embedded erase or embedded program is in progress.
3. Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30ns. Typical sleep mode current is 200 nA.
4. Post radiation limits are the 105℃ temperature limits when specified.
5. Guaranteed by functional test only.

AC Characteristics — Read Only Operations

(V_{CC}=3.3V ± 0.3V; -40℃ ≤ T_C ≤ +105℃)

Symbol	Parameter	MIN	MAX	Unit
t_{RC} [1]	Read cycle tine	60		ns
t_{ACC}	Address to output delay		60	ns
t_{CE}	Chip enable to output delay		60	ns
t_{OE}	Output enable to output delay		25	ns
t_{DFCE} [1, 2]	Chip enable to output High-Z		20	ns
t_{DFOE} [1, 2]	Output enable to output High-Z		16	ns
t_{OH}	Output hold time from addresses, CE# or OE#, whichever occurs first	0		ns
t_{OEH} [1]	Output enable hold time — read	0		ns
	Output enable hold time — toggle and data# polling	5		ns

Notes:

1. Guaranteed by functional test only.
2. Measurements performed by placing a 50 ohm termination on the data pin with a bias of V_{CC}/2 or equivalent. The time from control high to the data bus transitioning to V_{CC}/2 ±100 mV is taken as tDFXX.

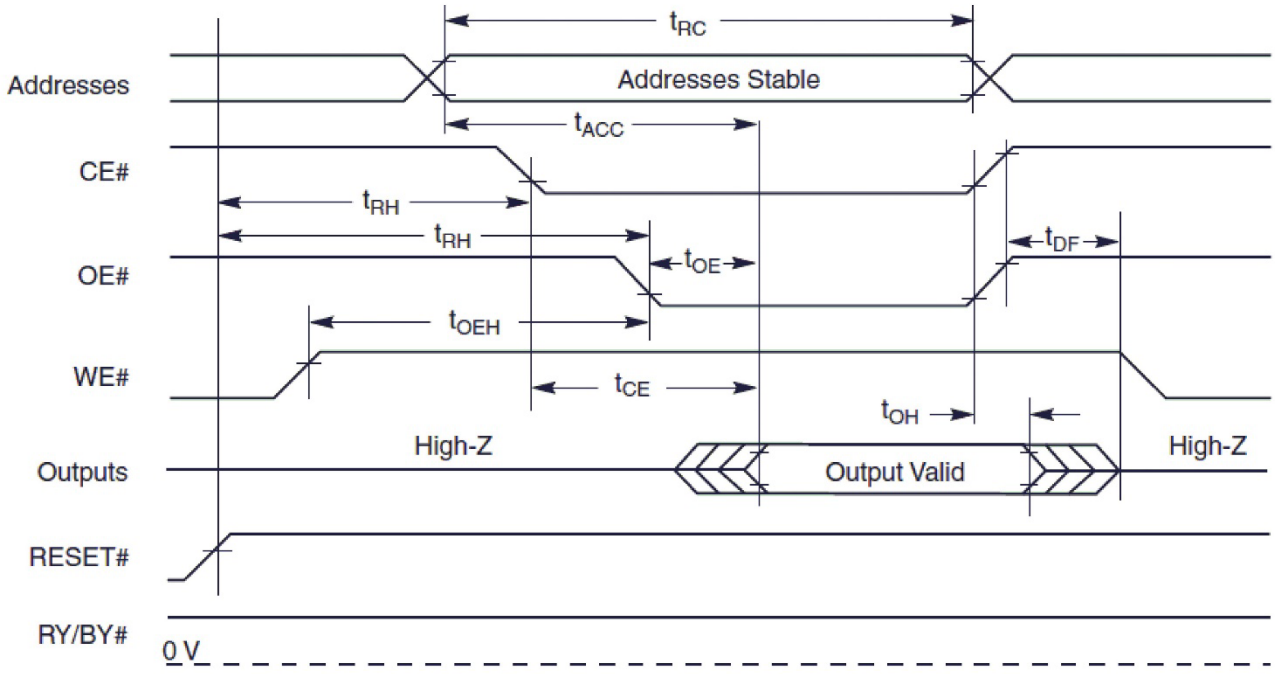


Figure 7: Read Operations Timing

AC Characteristics — Hardware Reset

(V_{CC}=3.3V ± 0.3V; -40°C ≤ T_C ≤ +105°C)

Symbol	Parameter	MIN	MAX	Unit
t_{READY} 1	RESET# pin low (during embedded algorithms) to read mode		35	µs
t_{READY} 1	RESET# pin low (NOT during embedded algorithms) to read mode		500	ns
t_{RP}	RESET# pulse width	500		ns
t_{RH}	RESET high time before read	60		ns
t_{RPD}	RESET # low to standby mode	35		µs
t_{RB}[1]	RY/BY# recover time	0		ns

Note:

1. Guaranteed by functional test only.

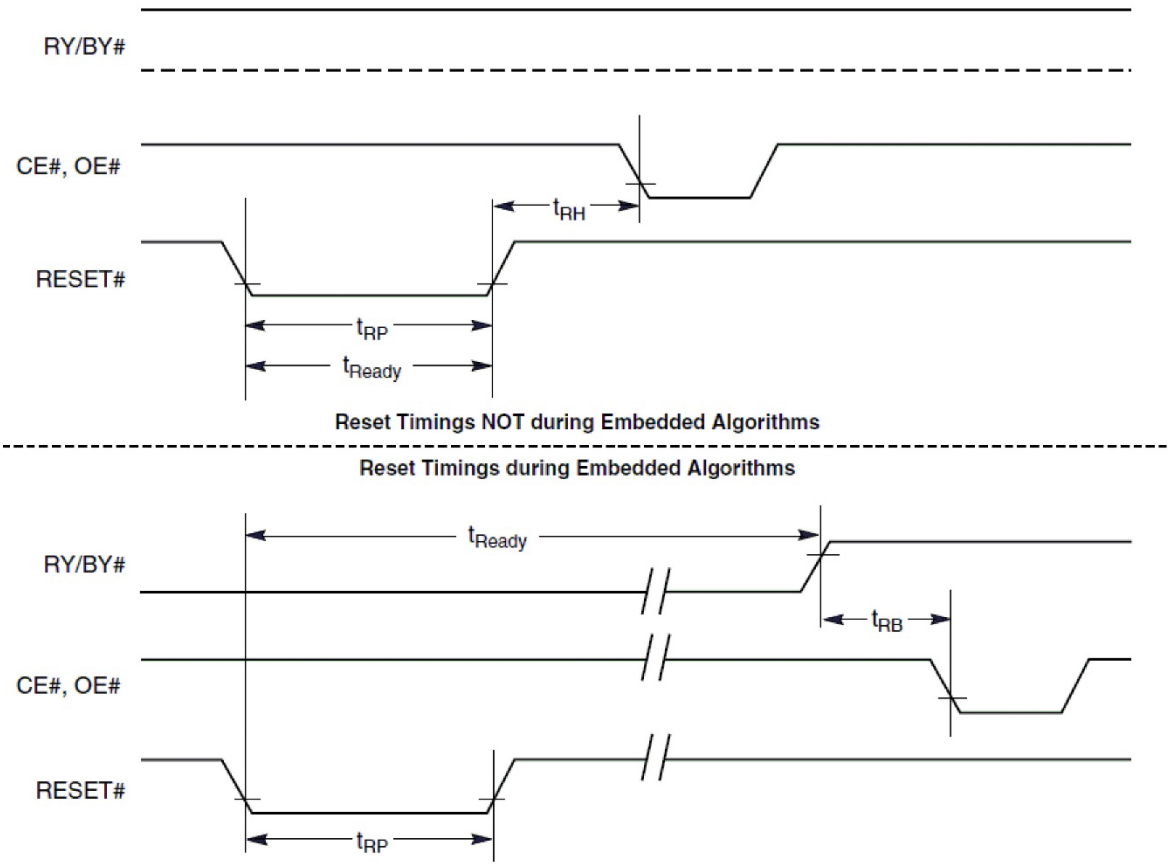


Figure 8: Reset Timings

AC Characteristics — Word/Byte Configuration (Byte #)

(V_{CC}=3.3V ± 0.3V; -40°C ≤ T_C ≤ +105°C)

Symbol	Parameter	MIN	MAX	Unit
t_{ELFL}/t_{ELFH} [1]	CE# to BYTE# switching low or high		5	ns
t_{FLQZ} [2]	BYTE# switching low to output High-Z		16	ns
t_{FHQV}	BYTE# switching high to output active	60		ns

Notes:

1. Guaranteed by functional test only.
2. Measurements performed by placing a 50 ohm termination on the data pin with a bias of $V_{CC}/2$ or equivalent. The time from control high to the data bus transitioning to $V_{CC}/2$ ±100 mVis taken as t_{ELXX}.

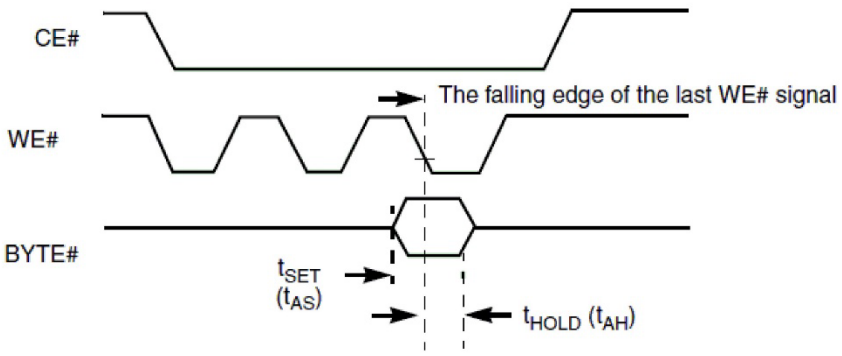


Figure 9: Byte# Timings for Read Operations

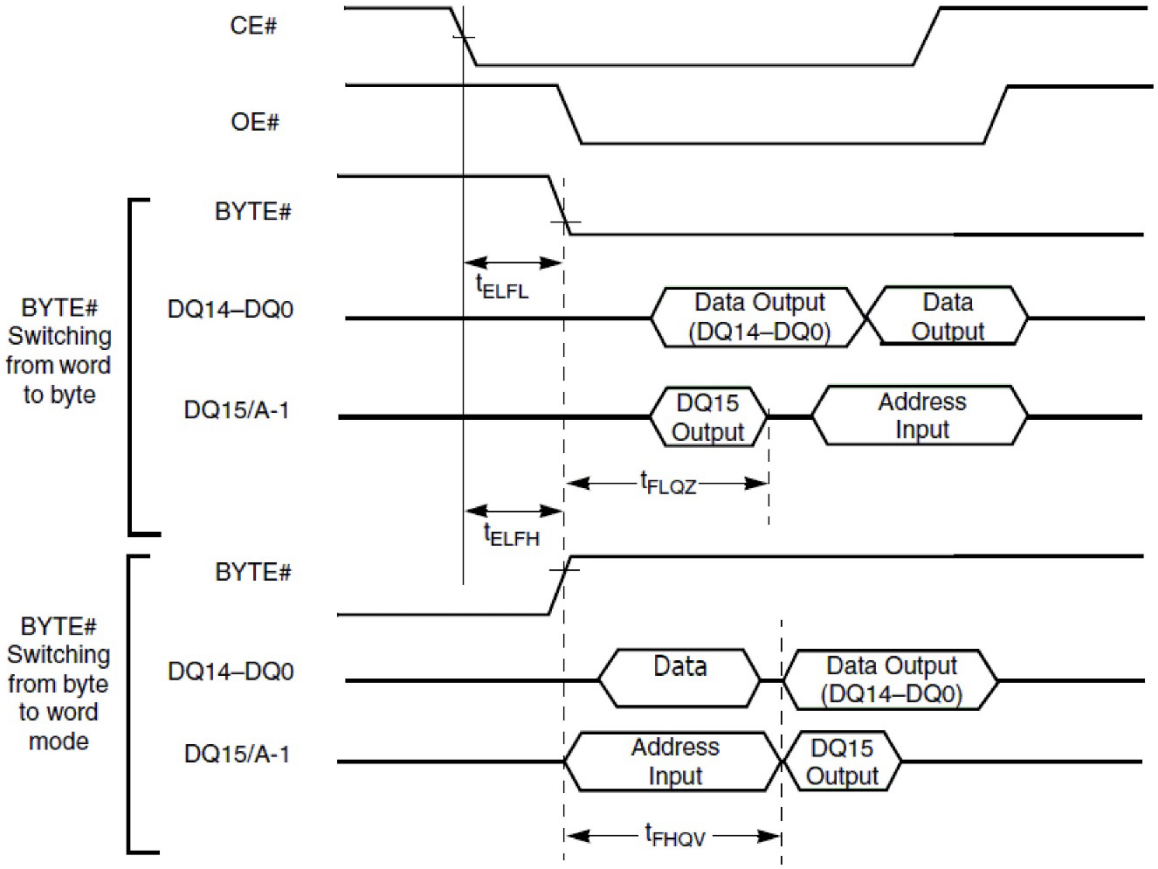


Figure 10: Byte# Timings for Write Operations

Erase and Program Operations

(V_{CC}=3.3V ± 0.3V; -40°C ≤ T_C ≤ +105°C)

Symbol	Parameter		MIN	MAX	Unit
t_{WC} [1]	Write cycle tine		60		ns
t_{AS} [1]	Address setup time		0		ns
t_{ASO} [1]	Address setup time to OE# low during toggle bit polling		15		ns
t_{AH} [1]	Address hold time		35		ns
t_{AHT} [1]	Address hold time from CE# or OE# high during toggle bit polling		0		ns
t_{DS} [1]	Data setup time		35		ns
t_{DH} [1]	Data hold time		0		ns
t_{OEPH} [1]	Output enable high during toggle bit polling		20		ns
t_{CS} [1]	CE# setup time		0		ns
t_{CH} [1]	CE# hold time		0		ns
t_{WP} [1]	Write pulse width		25		ns
t_{WPH} [1]	Write pulse width high		25		ns
tSR/W [1]	Latency between read and write operations		0		ns
t_{WHWH1} [1]	Programming operation	Byte	6		µs
		Word	6		µs
t_{WHWH2} [1, 2]	Sector erase operation		0.5		sec
t_{VCS} [3]	V_{CC} setup time		50		µs
t_{RB} [1]	Write recovery time from RY/BY#		0		ns
t_{BUSY}	Program/Erase valid to RY/BY# delay			90	ns
t_{ESL} [3]	Erase suspend latency			35	µs

Notes:

1. Guaranteed by functional test only.
2. See Erase and Programming Performance on page 39 for more information.
3. Supplied as a design limit, neither tested nor guaranteed.

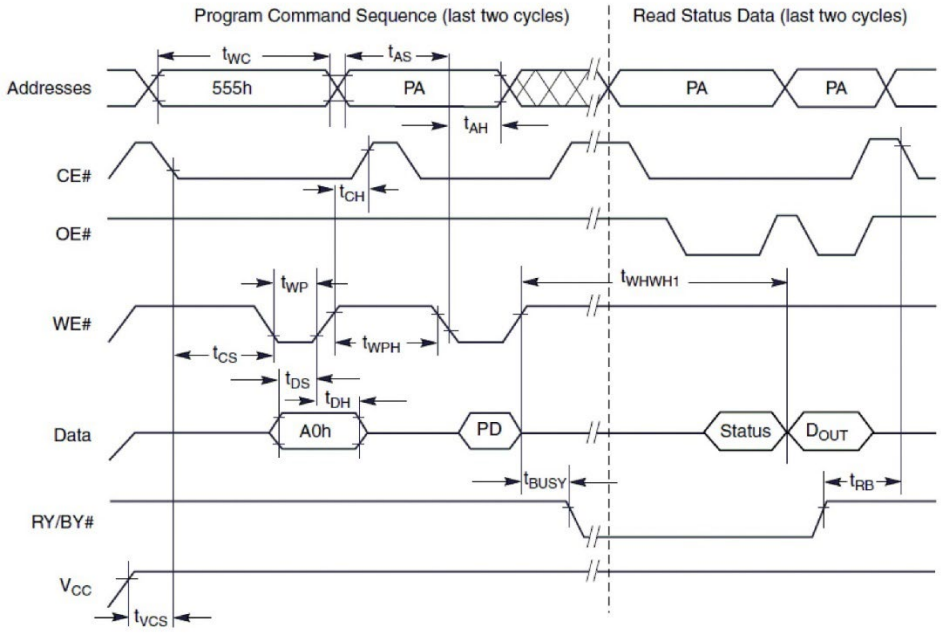


Figure 11: Program Operation Timings

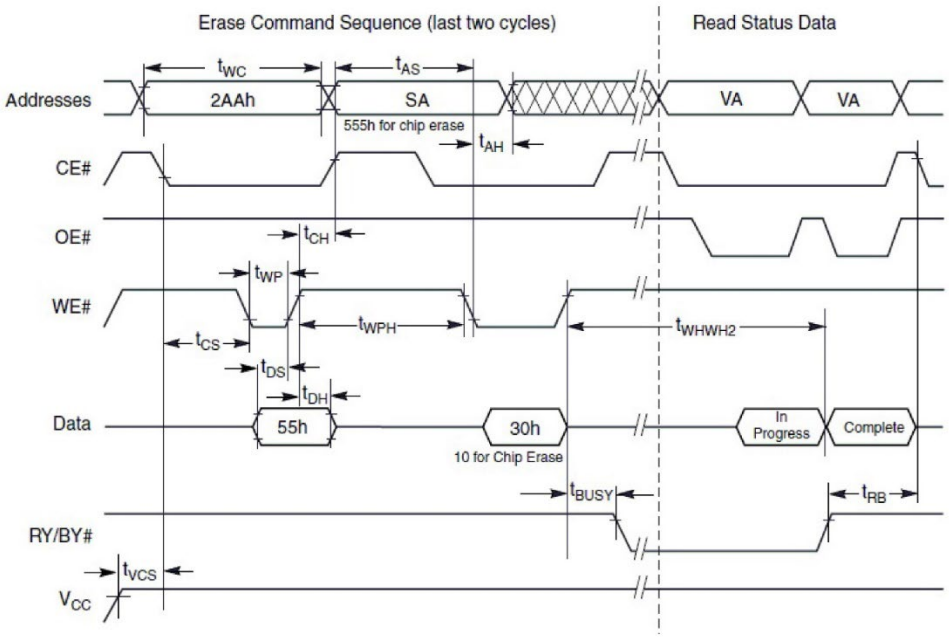


Figure 12: Chip/Sector Erase Operation Timings

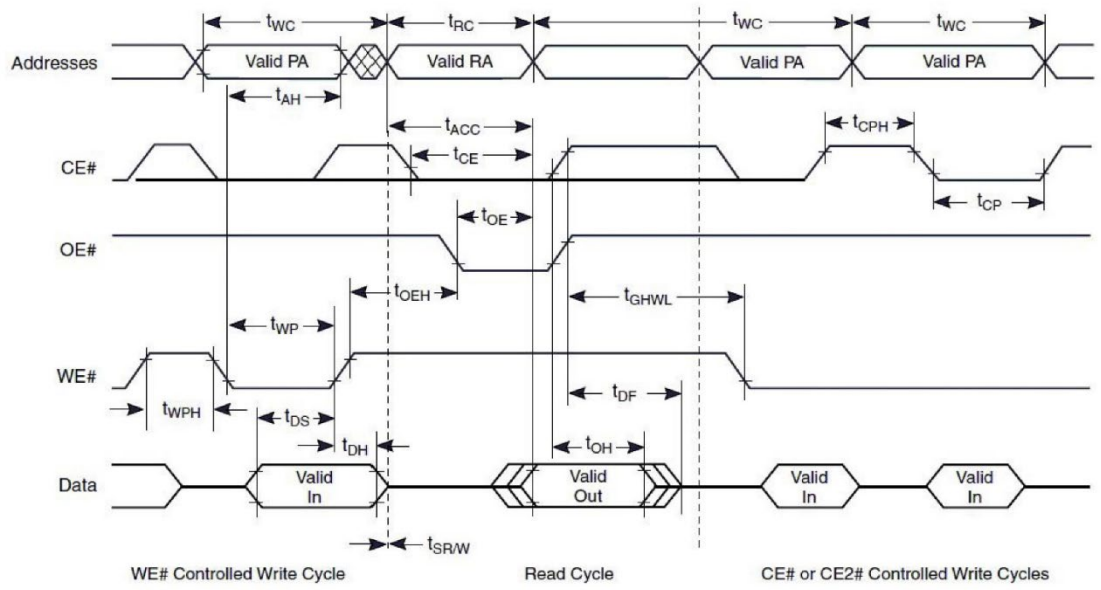


Figure 13: Back-to-Back Read/Write Timings

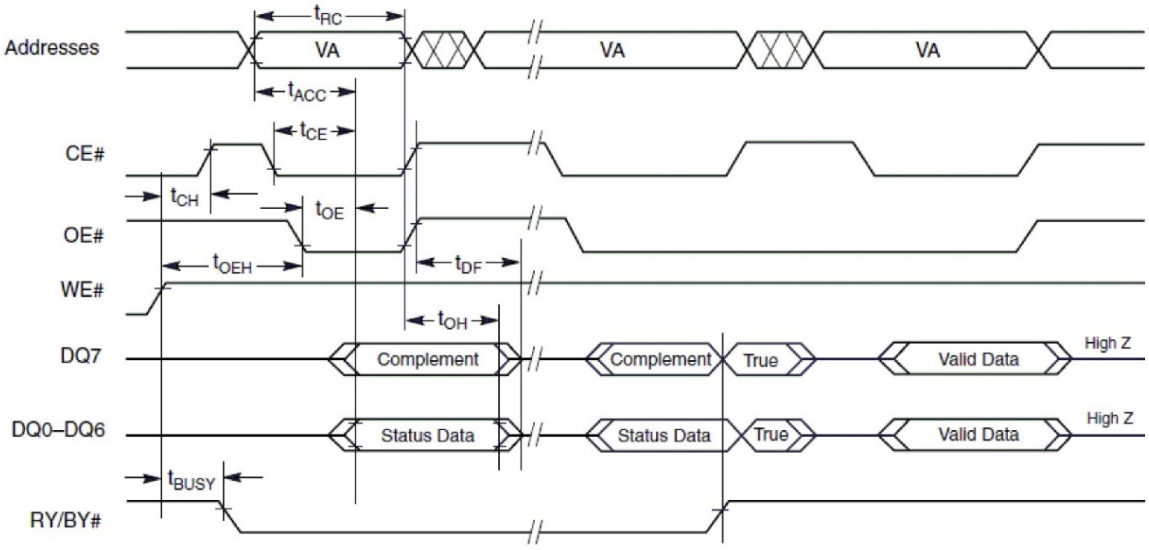


Figure 14: Data # Polling Timings (During Embedded Algorithms)

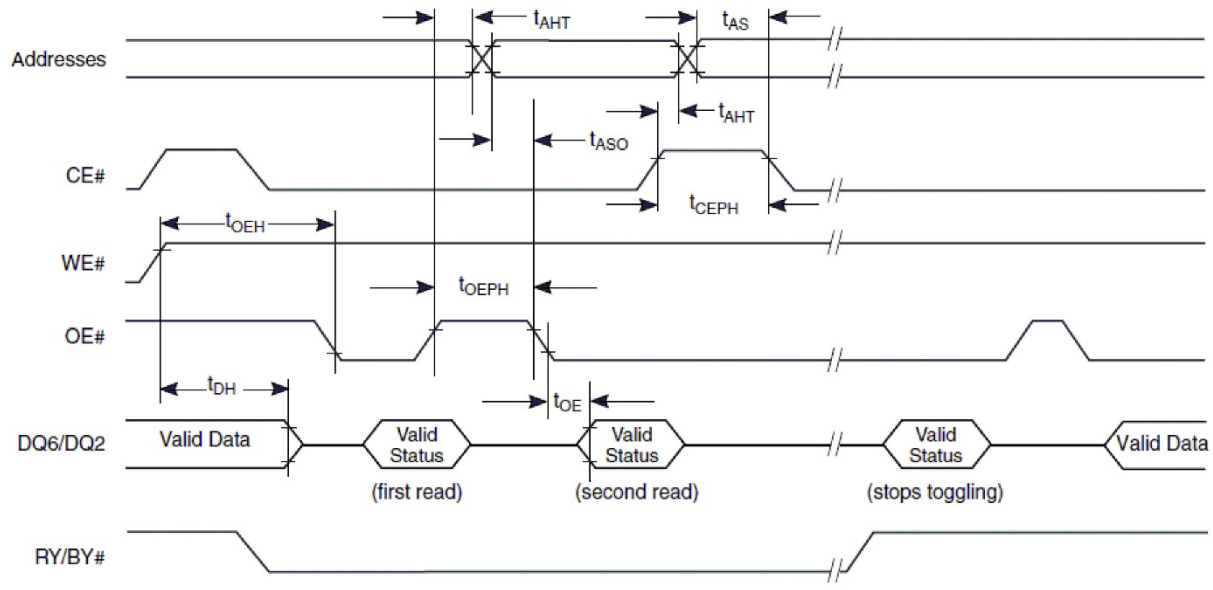


Figure 15: Figure 15. Toggle Bit Timings (During Embedded Algorithms)

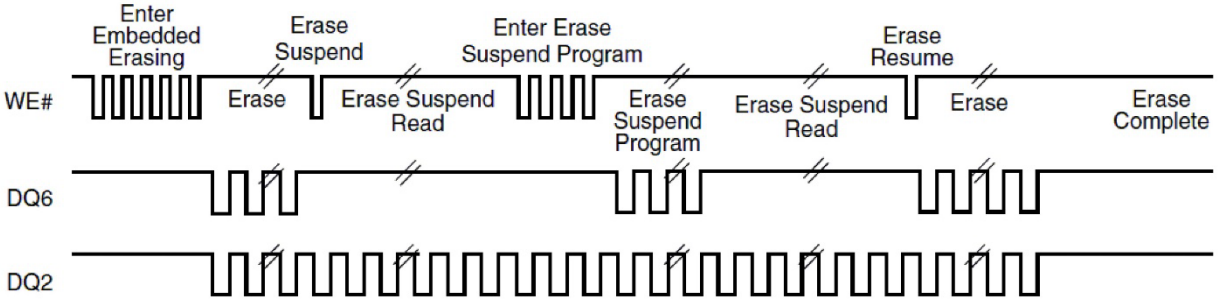


Figure 16: Figure 16. DQ2 vs DQ6

Alternate CE# Controlled Erase and Program Operations

(V_{CC}=3.3V ± 0.3V; -40°C ≤ T_C ≤ +105°C)

Symbol	Parameter		MIN	MAX	Unit
t_{WC} 1	Write cycle		60		ns
t_{AS} 1	Address setup time		0		ns
t_{AH} 1	Address hold time		35		ns

Symbol	Parameter		MIN	MAX	Unit
t_{DS} [1]	Data setup time		35		ns
t_{DH} [1]	Data hold time		0		ns
t_{GHEL} [1]	Read recovery time below write (OE# high to WE# low)		0		ns
t_{WS} [1]	WE# setup time		0		ns
t_{WH} [1]	WE# hold time		0		ns
t_{CP} [1]	CE# pulse width		25		ns
t_{CPH} [1]	CE# pulse width high		25		ns
t_{WHWH1} [1, 2]	Programming operation	Byte	6		µs
		Word	6		µs
t_{WHWH2} [1, 2]	Sector erase operation		0.5		sec

Notes:

1. Guaranteed by functional test only.
2. See Erase and Programming Performance on page 39 for more information.

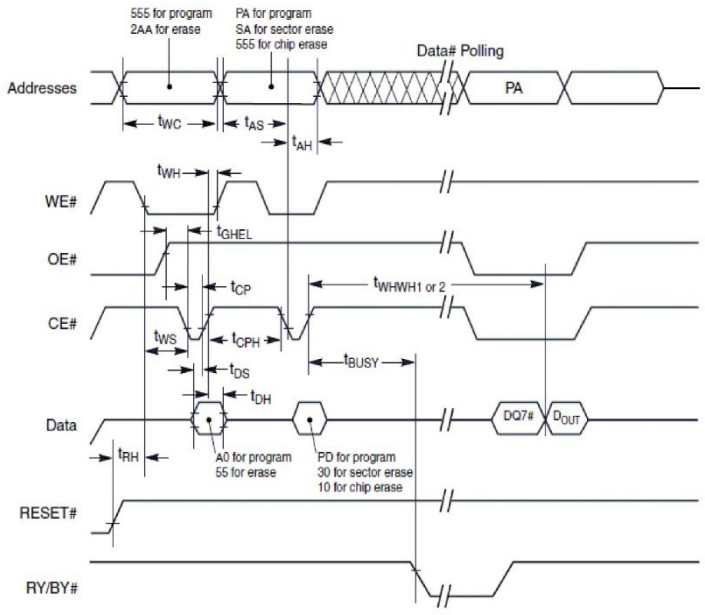


Figure 17: Alternate CE# Controlled Write (Erase/Program)

Erase and Programming Performance

(V_{CC}=3.3V ± 0.3V; -40℃ ≤ T_C ≤ +105℃)

Parameter	MAX	Unit
Sector erase time	5	sec
Chip erase time	120	sec
Byte program time [1]	150	µs
Word program time [1]	150	µs

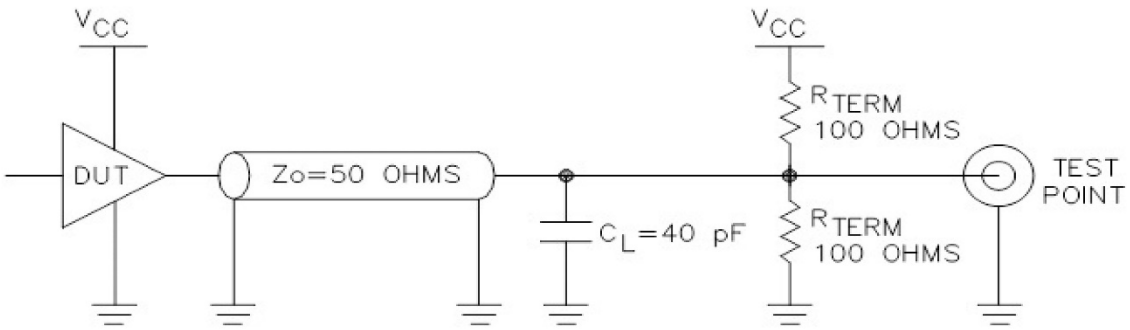
Note:

1. Guaranteed by functional test only.

Pin Capacitance

Parameter	Description	Test Setup	MAX	Unit
C_{IN}	Input capacitance (applies to A21-A0, DQ15-DQ0)	V_{IN} = 0	15	pF
C_{OUT}	Output capacitance (applies to DQ15-DQ0, RY/BY#)	V_{OUT}= 0	15	pF
C_{IN2}	Control pin capacitance (applies to CE#, WE#, RESET#, BYTE#)	V_{IN} = 0	15	pF
C_{IN3}	Control pin capacitance (applies to WP#))	V_{IN} = 0	25	pF

AC Test Load Circuit



Package Drawing

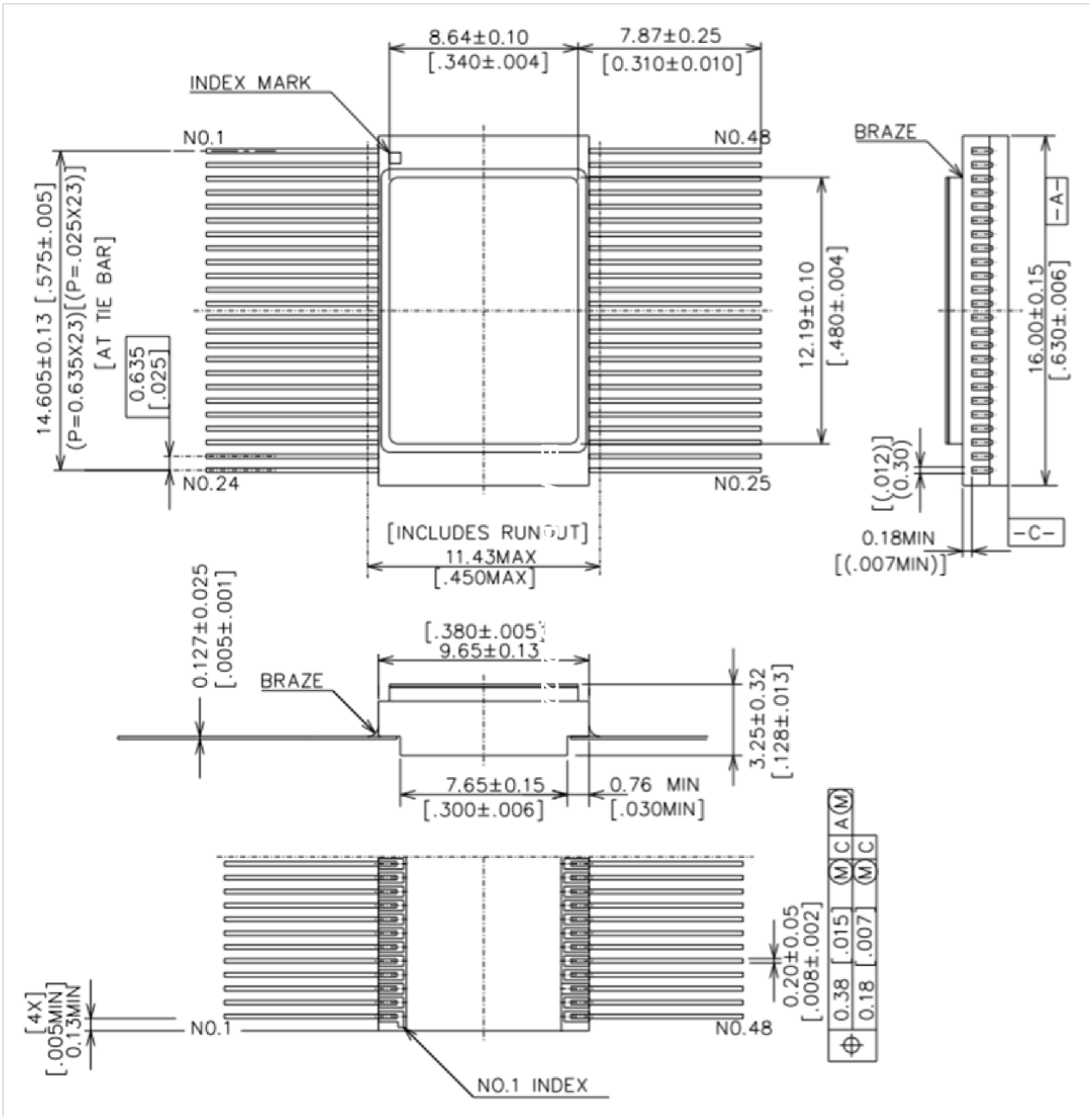


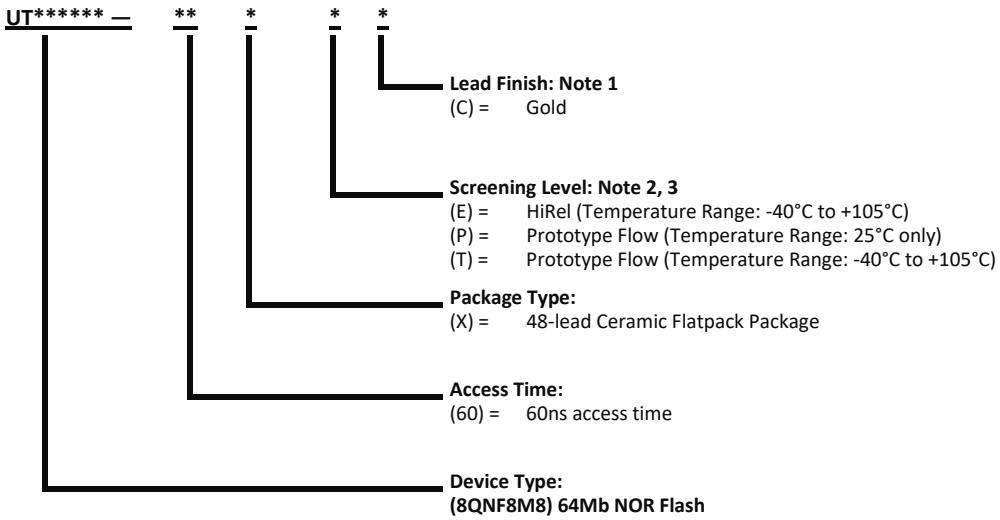
Figure 18: 48-pin Ceramic Flatpack Package

Notes:

1. Plating per MIL-PRF-38535
2. Seal ring and index mark are electrically connected to VSS.

Ordering Information

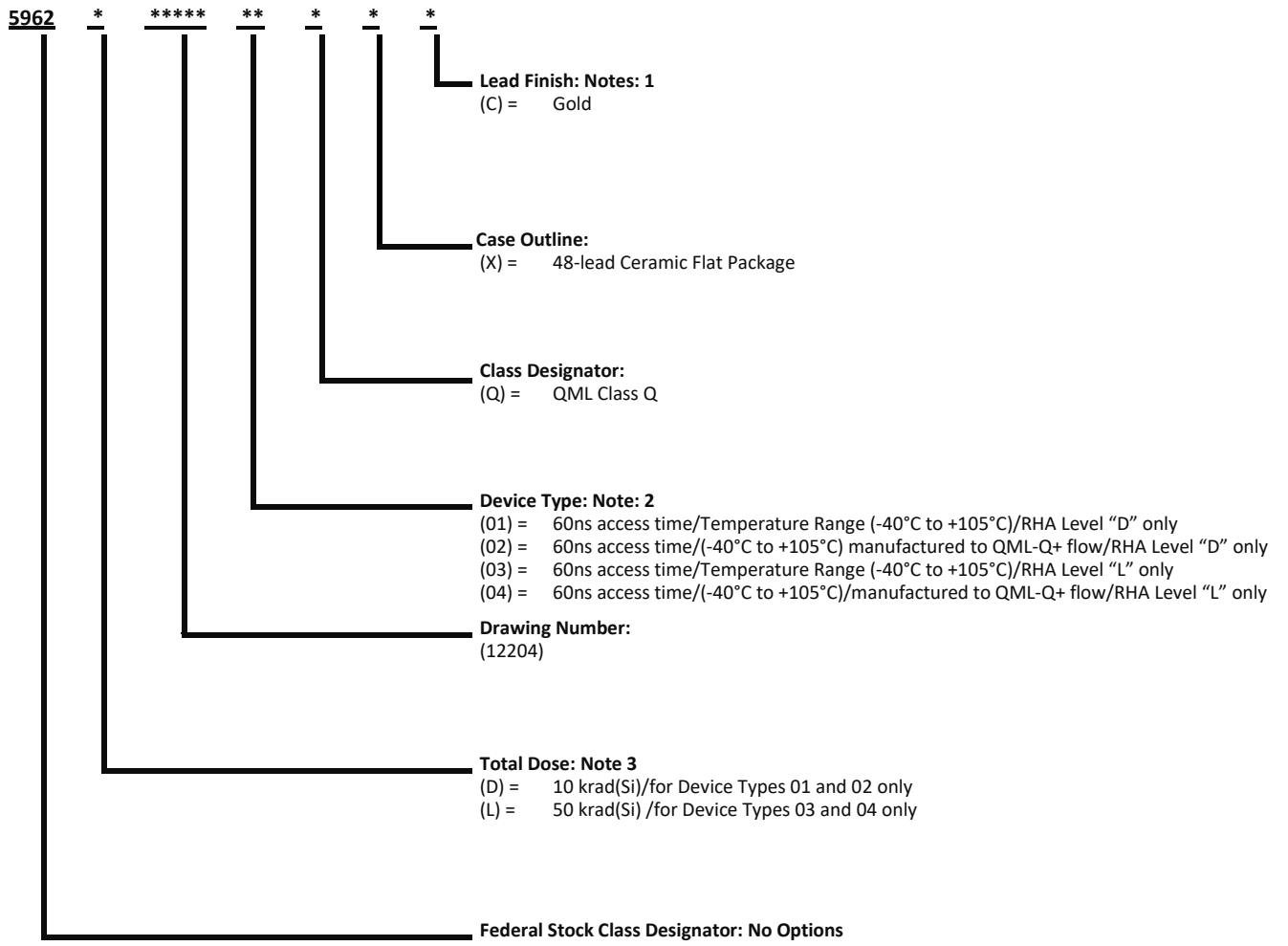
Frontgrade Part Numbering Ordering Information



Notes: * Radiographic inspection voids device warranty. Reference Frontgrade application note, X-ray Inspection Considerations

1. Lead finish is "C" (Gold) only.
2. Prototype flow per Frontgrade Colorado Springs Manufacturing Flows Document. Radiation neither tested nor guaranteed.
3. HiRel flow per Frontgrade Colorado Springs Manufacturing Flows Document. Radiation neither tested nor guaranteed.

SMD Part Number Ordering Information



Notes: * Radiographic inspection voids device warranty. Reference Frontgrade application note, X-ray Inspection Considerations 1)

4. Lead finish is "C" (Gold) only.
5. Frontgrade Q+ flow, as defined in Section 4.2.1d of SMD, provides QML-Q product through the SMD that is manufactured with Frontgrade standard QML-V flow.
6. Irradiated per MIL-STD-883 Method 1019 Condition C at 50-300 krad(Si) using an in-situ 900 rad(Si) device unpowered and 100 rad(Si) device statistically biased duty cycle repeated 50 times to achieve a TID level of 50 krad(Si). This irradiation insitu biasing method is predicated on an application which may allow the device to be unpowered during 90% of the mission life.

Revision History

Date	Revision #	Author	Change Description	Page #
5/1/2018		MJL	Initial revision history capture.	NA
4/25/2022		MJL	Added (See Table 13) to features page 1. Added ref to note 2 on data retention spec, and added note 2 to Table 13 page 27. Added Radiographic inspection voids warranty to page 40. Added reference to X-ray application note to both page 40 and 41. Added this revision table page 42	1, 27, 40, 41, 42

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.