FRONTGRADE

ADV DATASHEET

UT8MRQRHxG

1Gbit, 2Gbit, 4Gbit, 8Gbit Dual-Quad SPI MRAM

8/5/2024

Version#: 0.1.3

Features

- Interface
  - — Dual Quad SPI – support 8-bit wide transfer
    - Dual QPI (4-4-4) – up to 100MHz SDR
    - Dual QPI (4-4-4) – up to 50MHz DDR
- Technology
  - — 22nm pMTJ STT-MRAM
    - Data Endurance: 10^{16} write cycles
    - Data Retention: 20 years @ 85°C
- Density
  - — 1Gb, 2Gb, 4Gb, 8Gb
- Operating Voltage Range
  - — VCC: 2.50V – 3.60V
  - — VCCIO: 1.8V, 2.5V, 3.0V, 3.3V
- Packages
  - — 224-ball FBGA (20mm x 20mm)
    - Available in either lead free (SAC305) or leaded (63Sn 37Pb) balls
- Data Protection
  - — Hardware Based
    - Dedicated Hardware Signals (HBP0, HBP1, HBP2) in conjunction with Top/Bottom Select Signal (HTBSEL)
- Software Based
  - — Address Range Selectable through Configuration bits (Top/Bottom, Block Protect [2:0])
- Available in Frontgrade's Manufacturing Flow based on PEMS-INST-001 Class 2

Operational Environment

- Temperature Range: -40°C to +125°C*
- Total Dose: 100 krads (Si)
- SEL Immune: ≤ 60 MeV-cm^2/mg at 3V & 105°C
  - — ≤ 75 MeV-cm^2/mg at 2.7V & 105°C
- SEU Immune: ≤LET 57 MeV-cm^2/mg

Applications

- Reconfigurable computing image storage
- Ideal for applications needing low power, infinite endurance requiring the ability to store and retrieve data without incurring large latencies.

*All references to temperature herein are case temperature unless otherwise stated

Table of Contents

General Description

UT8MRQRHxG is a Spin-transfer torque Magneto-resistive random-access memory (STT-MRAM). It is offered in density ranging from 1Gbit to 8Gbit. MRAM technology is analogous to Flash technology with SRAM compatible read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile with 10^{16} write cycles endurance and greater than 20-year retention @85°C.

Table 1: Technology Comparison

	SRAM	Flash	EEPROM	MRAM
Non-Volatility	–	√	√	√
Write Performance	√	–	–	√
Read Performance	√	–	–	√
Endurance	√	–	–	√
Power	–	–	–	√

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, infinite endurance and scalable non-volatile memory technology.

UT8MRQRHxG has a Serial Peripheral Interface (SPI). SPI is a synchronous interface which uses separate lines for data and clock to help keep the host and slave in perfect synchronization. The clock tells the receiver exactly when to sample the bits on the data line. This can be either the rising (low to high) or falling (high to low) or both edges of the clock signal; please consult the instruction sequences in this datasheet for more details. When the receiver detects that correct edge, it can latch in the data.

UT8MRQRHxG connects two Quad SPI devices with dual-CS#, providing an eight bit I/O data path. Each device can be configured and operate independently with its own register sets, managing by a sperate CS#.

UT8MRQRHxG is available in a224-ball FBGA package. The package has separate balls for CS1#, CLK1#, and INT1 (Dual-Quad SPI device 1) and CS2#, CLK2#, and INT2 (Dual-Quad SPI device 2). This package is compatible with similar low-power volatile and non-volatile products.

Table 2: Multi-Die Package Density

Density	512Mb Die	1Gb Die
1Gb	x2	-
2Gb	-	x2
4Gb	-	x4
8Gb	-	x8

UT8MRQRHxG is offered with industrial extended (-40°C to 125°C) operating temperature ranges: this is measured as the junction temperature.

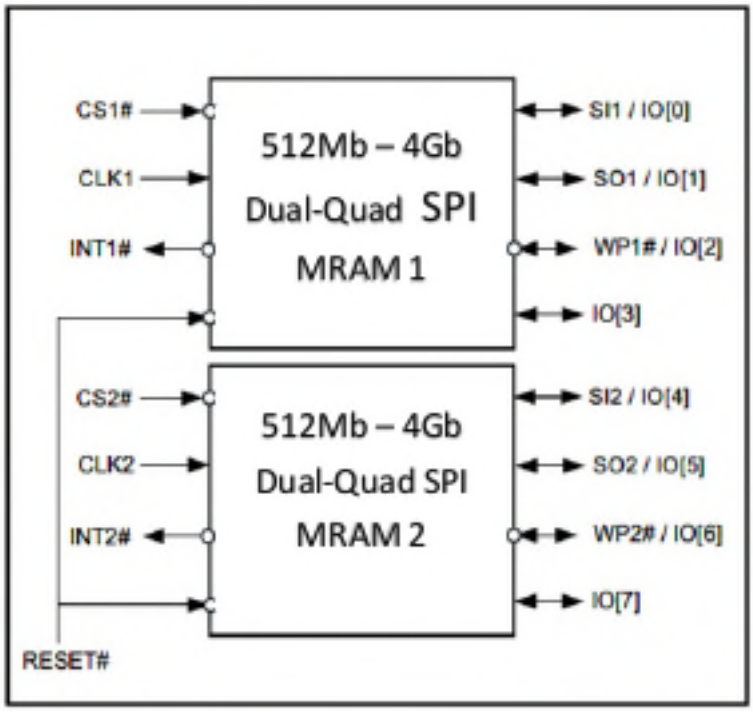


Figure 1: Simple Block Diagram

Signal Description, Assignments and Pinouts

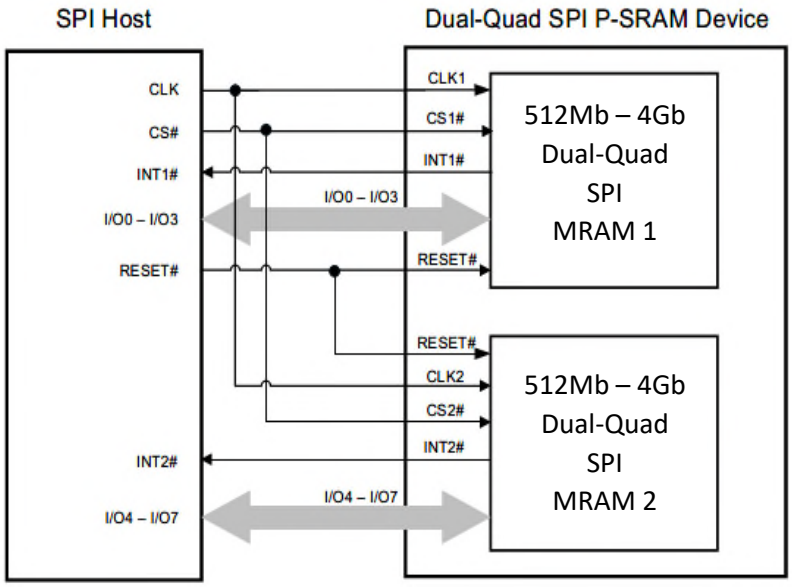


Figure 2: Single CS# System Block Diagram

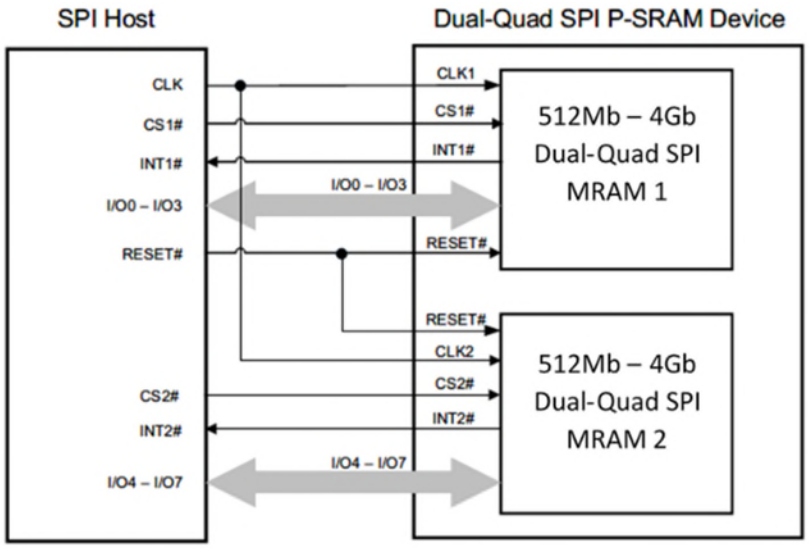


Figure 3: Dual-CS# System Block Diagram

Table 3: Signal Description for 224-Ball FPGA Package

Signal	Ball Assignment	Type	Description
CS1#	L9	Input	**Chip Select 1**: When CS1# is driven High, the Quad SPI device 1 will enter standby mode. All other input pins are ignored and the output pin is tri-stated. Driving CS1# Low enables device 1, placing it in the active mode. After power-up, a falling edge on CS1# is required prior to the start of any instructions.
CLK1	K9	Input	**Clock 1:** Provides the timing for device 1 serial interface. Depending on the mode selected, either single (rising or falling) edge or both edges of the clock are utilized for information transfer. In Single Data Rate mode (SDR) command, address and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock. In Double Data Rate mode (DDR) command is latched on the rising edge of the clock. Address and Data inputs are latched on both edges of the clock. Similarly, Data is output on both edges of the clock. The following two SPI clock modes are supported. • SPI Mode 0 (CPOL = 0, CPHA = 0) – SDR and DDR • SPI Mode 3 (CPOL = 1, CPHA = 1) – SDR only
INT1#	J12	Output	**Interrupt 1:** Output generated by device 1 when an unrecoverable ECC error is detected during read operation (output goes low on error).
SI1	M10	Input	**Serial Data Input (SPI):** The unidirectional I/O transfers data into device 1 on the rising edge of the clock in Single SPI mode.
IO[0]		Bidirectional	**Bidirectional Data 0 (QPI):** The bidirectional I/O transfers data into and out of device 1 in Quad SPI mode.
SO1	M9	Output	**Serial Data Output (SPI):** The unidirectional I/O transfers data out of device 1 on the falling edge of the clock in Single SPI mode.
IO[1}		Bidirectional	**Bidirectional Data 1 (QPI):** The bidirectional I/O that transfers data into and out of device 1 in Quad SPI mode.
WP1#	L11	Input	**Write Protect 1 (SPI):** Write protects the status register of device 1 in conjunction with the enable/disable bit of the status register. This is important since other write protection features are controlled 1through the Status Register. When the enable/disable bit of the status register is set to 1 and the WP# signal is driven Low, the status register becomes read-only and the WRITE STATUS REGISTER operation will not execute. This signal does not have internal pull-ups, it cannot be left floating and must be driven. WP# is valid only in Single SPI mode. This pin can be tied to Vcc if not used.
IO[2]		Bidirectional	**Bidirectional Data 2 (QPI):** The bidirectional I/O transfers data into and out of device 1 in Quad SPI mode.
IO[3]	M11	Bidirectional	**Bidirectional Data 3 (QPI):** The bidirectional I/O transfers data into and out of device 1 in Quad SPI mode. This pin can be tied to Vcc if not used.
CS2#	J10	Input	**Chip Select 2:** When CS2# is driven High, the Quad SPI device 2 will enter standby mode. All other input pins are ignored and the output pin is tri-stated. Driving CS2# Low enables device 2, placing it in the active mode. After power-up, a falling edge on CS2# is required prior to the start of any instructions.
CLK2	K8	Input	**Clock 2:** Provides the timing for device 2 serial interface. Depending on the mode selected, either single (rising or falling) edge or both edges of the clock are utilized for information transfer. In Single Data Rate mode (SDR) command, address and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock.

Signal	Ball Assignment	Type	Description
			In Double Data Rate mode (DDR) command is latched on the rising edge of the clock. Address and Data inputs are latched on both edges of the clock. Similarly, Data is output on both edges of the clock. The following two SPI clock modes are supported. • SPI Mode 0 (CPOL = 0, CPHA = 0) – SDR and DDR • SPI Mode 3 (CPOL = 1, CPHA = 1) – SDR only
INT2#	K10	Output	**Interrupt 2:** Output generated by device 2 when an unrecoverable ECC error is detected during read operation (output goes low on error).
SI2	M12	Input	**Serial Data Input (SPI):** The unidirectional I/O transfers data into device 2 on the rising edge of the clock in Single SPI mode.
IO[4]		Bidirectional	**Bidirectional Data 4 (QPI):** The bidirectional I/O transfers data into and out of device 2 in Quad SPI mode.
SO2	N10	Input	**Serial Data Output (SPI):** The unidirectional I/O transfers data out of device 2 on the falling edge of the clock in Single SPI mode.
IO[5]		Bidirectional	**Bidirectional Data 5 (QPI):** The bidirectional I/O transfers data into and out of device 2 in Quad SPI mode.
WP2#	N9	Input	**Write Protect 2 (SPI):** Write protects the status register of device 2 in conjunction with the enable/disable bit of the status register. This is important since other write protection features are controlled 1through the Status Register. When the enable/disable bit of the status register is set to 1 and the WP# signal is driven Low, the status register becomes read-only and the WRITE STATUS REGISTER operation will not execute. This signal does not have internal pull-ups, it cannot be left floating and must be driven. WP# is valid only in Single SPI mode. This pin can be tied to Vcc if not used.
IO[6]		Bidirectional	**Bidirectional Data 6 (QPI):** The bidirectional I/O transfers data into and out of device 2 in Quad SPI mode.
IO[7]	N8	Bidirectional	**Bidirectional Data 7 (QPI):** The bidirectional I/O transfers data into and out of device 2 in Quad SPI mode.
RESET#	J11	Input	**RESET:** This is a RESET# signal. When this signal is driven high, the device is in the normal operating mode. When this signal is driven low, the device is in reset mode and the output is High-Z.
HBP[0:2]	G12, G13, H14	Input	**HPB0, HBP1, HBP2:** these Hardware Block Protect signals, when driven High or Low, define the size of the memory array to be hardware protected against all Write memory array instructions: These balls have a Pull down to Vss. If left disconnected, they will be seen by device as “Low”.

Signal	Ball Assignment	Type	Description
HTBSEL	J14	Input	**HTBSEL:** this signal when driven High or Low, is used in conjunction with the Hardware Block Protect Pins (HBP0, HBP1, and HBP2) determines if the write-protected memory area defined by the state of the HBP pins, starts from the top or the bottom of the memory array: This ball has a Pull down to Vss. If left disconnected, it will be seen by device as “Low”.
VDD	K12	Supply	Reference Voltage Supply
VCCIO	G6, P6, G7, J7, P7, M8, H9, H11, N11, J13, M13, G14, P14	Supply	I/O power supply.
VSSIO	M7, H8, L8, P10, H12, N12, P12, H13, N13	Supply	I/O ground supply.
VCC	K6, M6, K7, G9, P9, G11, K11, P11, K13, K14, M14	Supply	Core power supply.
VSS	A3, B3, W3, Y3, A4, Y4, F5, G5, P5, R5, F6, H6, J6, L6, N6, R6, L7, N7, G8, P8, G10, H10, L12, L13, P13, F14, L14 N14, R14, F15, G15, P15, R15, A16, Y16, A17, B17, W17, Y17	Supply	Core ground supply.
DNU	H7, J8, J9, L10	-	Do Not Use: DNUs must be left unconnected, floating.

Signal	Ball Assignment	Type	Description
Dummy	A1, A2, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A18, A19, B1, B2, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B18, B19 C1,C2,C18,C19, D1,D2,D18,D19, E1,E2,E18,E19, F1,F2,F18,F19, G1,G2,G18,G19, H1,H2,H18,H19, J1,J2,J18,J19, K1,K2,K18,K19, L1,L2,L18,L19, M1,M2,M18,M19, N1,N2,N18,N19, P1,P2,P18,P19, R1,R2,R18,R19, T1,T2,T18,T19, U1,U2,U18,U19, V1,V2,V18,V19, W1,W2,W4,W5, W6,W7,W8,W9, W10,W11,W12, W13,W14,W15, W16,W18,W19, Y1,Y2,Y5,Y6,Y7,Y8, Y9,Y10,Y11,Y12,Y13,Y14,Y15,Y18,Y19	Mechanical	Dummy balls are electrically not connected. *

Package Options

224-ball FBGA (Balls Down, Top View)

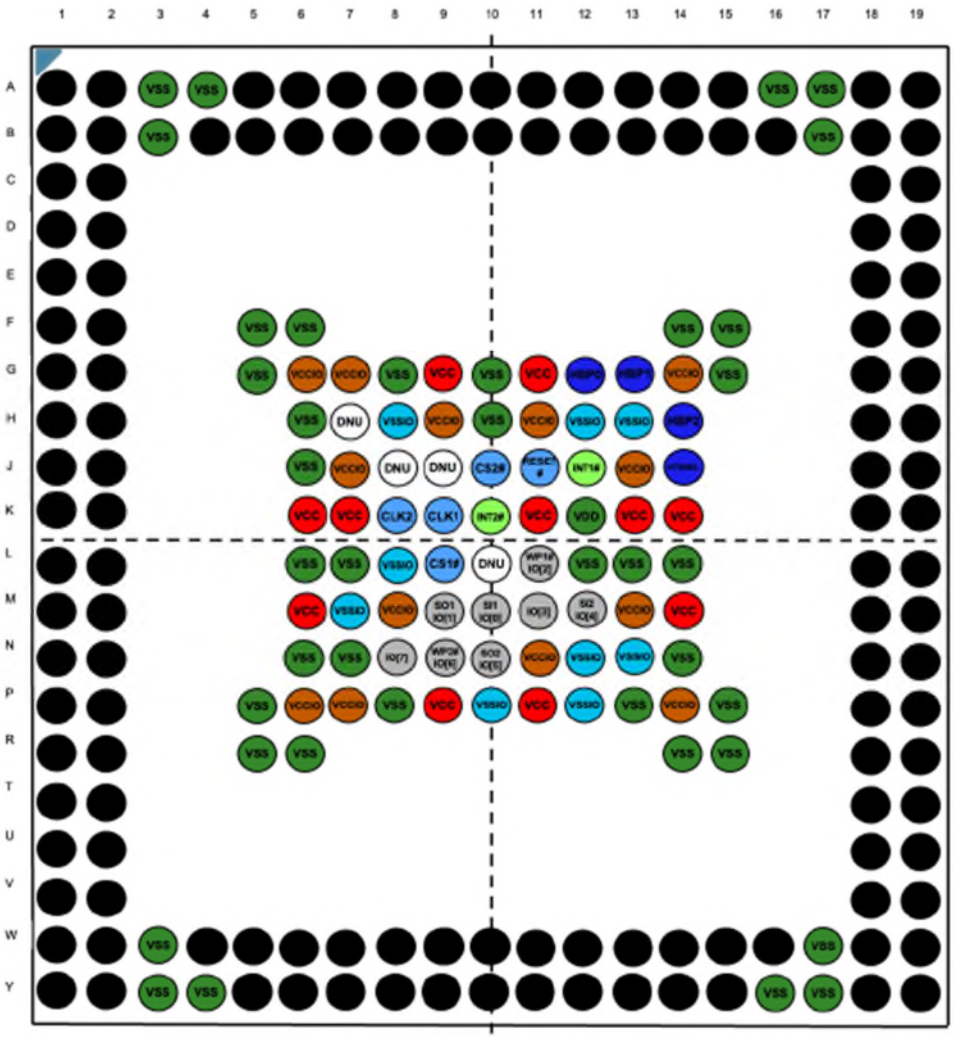


Figure 4: 224-ball FBGA

Architecture

UT8MRQRHxG is a high performance serial STT-MRAM device. It features a SPI-compatible bus interface running up to 50MHz (QPI) DDR mode or 100MHz (QPI) SDR mode, eXecute-In-Place (XIP) functionality, and hardware/software-based data protection mechanisms.

When CS# is Low, the device is selected and in active power mode. When CS# is High, the device is deselected but can remain in active power mode until ongoing internal operations are completed. Then the device goes into standby power mode and device current consumption drops to I_{SB}.

UT8MRQRHxG contains an 8-bit instruction register. All functionality is controlled through the values loaded into this instruction register. In Single SPI mode, the device is accessed via the SI / IO[0] pin of a Dual-Quad SPI 1 and the SI / IO[4] pin of a Dual-Quad SPI 2. In Quad mode, the IO[0:3] of a Dual-Quad SPI 1 and the IO[4:7] of a Dual-Quad SPI 2 are used respectively to access the device (consult Figure 2 & Figure 3). Furthermore, Single Data Rate (SDR) and Double Data Rate (DDR) instructions utilize CLK edges differently to transfer information; SDR uses a single CLK edge whereas DDR uses both edges of CLK. Table 4 & Table 5 summarizes all the different interface modes supported and their respective I/O usage. Table 6 shows the clock edge used for each instruction component

Nomenclature adoption: A typical SPI instruction consists of command, address and data components. The bus width to transmit these three components varies based on the SPI interface mode selected. To accurately represent the number of I/Os used to transmit these three components, a nomenclature (command-address-data) is adopted and used throughout this document. Integers placed in the (command-address-data) fields represent the number of I/Os used to transmit the particular component. As an example, 1-1-1 means command, address and data are transmitted on a single I/O (SI / IO[0]] or SO / IO[1]) of a Dual-Quad SPI 1 and (SI / IO[4]] or SO / IO[5]) of a Dual-Quad SPI 2. On the other hand, 4-4-4 represents command, address and data being sent on eight I/Os: (IO[3:0]) of a Dual-Quad SPI 1 and (IO[7:4]) of a Dual-Quad SPI 2 (consult Figure 2 & Figure 3).

All AC timings and waveforms and DC specification are defined in the datasheet using single CS# (Chip Select) and CLK (Serial Clock) signals.

Table 4: Interface Modes of Operations – Device 1

Instruction Component	Single SPI (1-1-1)	Quad Output SPI (1-1-4)	Quad I/O SPI (1-4-4)	QPI (4-4-4)
Command	SI / IO[0]	SI / IO[0]	SI / IO[0]	IO[3:0]
Address	SI / IO[0]	IO[0]	IO[3:0]	IO[3:0]
Data Input	SI / IO[0]	IO[3:0]	IO[3:0]	IO[3:0]
Data Output	SO / IO[1]	IO[3:0]	IO[3:0]	IO[3:0]

Table 5: Interface Modes of Operations – Device 2

Instruction Component	Single SPI (1-1-1)	Quad Output SPI (1-1-4)	Quad I/O SPI (1-4-4)	QPI (4-4-4)
Command	SI / IO[4]	SI / IO[4]	SI / IO[4]	IO[7:4]
Address	SI / IO[4]	IO[4]	IO[7:4]	IO[7:4]
Data Input	SI / IO[4]	IO[7:4]	IO[7:4]	IO[7:4]
Data Output	SO / IO[5]	IO[7:4]	IO[7:4]	IO[7:4]

Table 6: Clock Edge Used for instructions in SDR and DDR modes

Instruction Type	Command	Address	Data Input	Data Output
(1-1-1) SDR	R	R	R	F [1]
(1-1-1) DDR	R	R F	R F	F R [1]
(1-4-4) SDR	R	R	R	F [1]
(1-4-4) DDR	R	R F	R F	F R [1]
(4-4-4) SDR	R	R	R	F [1]
(4-4-4) DDR	R	R F	R F	F R [1]

Notes:

R: Rising Clock Edge

F: Falling Clock Edge

1. Data output from UT8MRQRHxG always begins on the falling edge of the clock – SDR & DDR

UT8MRQRHxG supports eXecute-In-Place (XIP) which allows completing a series of read and write instructions without having to individually load the read or write command for each instruction. Thus, XIP mode saves command overhead and reduces random read & write access time. A special XIP byte must be entered after the address bits to enable/disable (Axh/Fxh) XIP.

UT8MRQRHxG offers both hardware and software-based data protection schemes. Hardware protection is through WP# pin. Software protection is controlled by configuration bits in the Status register. Both schemes inhibit writing to the registers and memory array.

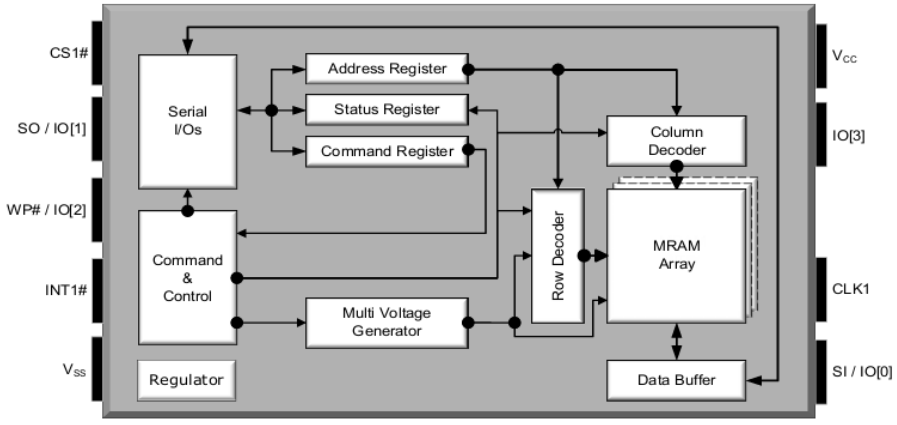


Figure 5: Functional Block Diagram – Dual QSPI Device 1

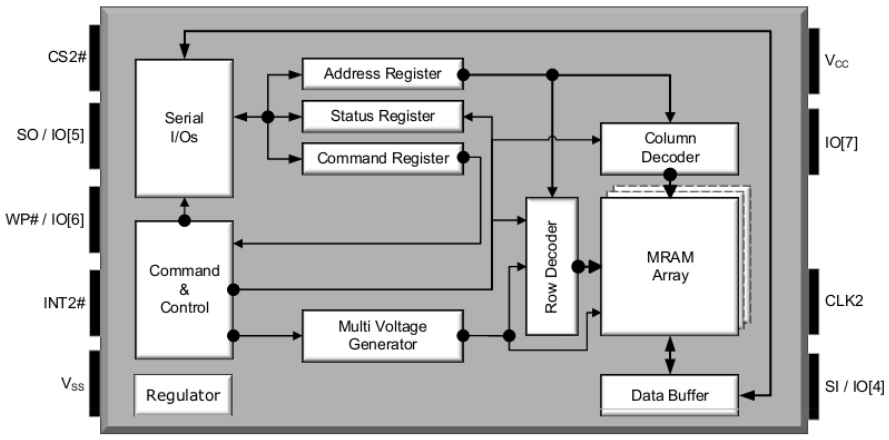


Figure 6: Functional Block Diagram – Dual QSPI Device 2

Table 7: Modes of Operation – Device 1

Mode	Current	CS#	CLK	SI / IO[3:0]	SO / IO[3:0]
Standby	ISB	H	Gated	Gated / Hi-Z	Hi-Z / Hi-Z
Active - Read	IREAD	L	Toggle	Command, Address	Data Output
Active - Write	IWRITE	L	Toggle	Command, Address, Data Input	Hi-Z

Notes:

H: High (Logic '1')

L: Low (Logic '0')

Hi-Z: High Impedance

Table 8: Modes of Operation – Device 2

Mode	Current	CS#	CLK	SI / IO[7:4]	SO / IO[7:4]
Standby	ISB	H	Gated	Gated / Hi-Z	Hi-Z / Hi-Z
Active - Read	IREAD	L	Toggle	Command, Address	Data Output
Active - Write	IWRITE	L	Toggle	Command, Address, Data Input	Hi-Z

Notes:

H: High (Logic '1')

L: Low (Logic '0')

Hi-Z: High Impedance

Device Initialization

When powering up, the following procedure is required to initialize the device correctly:

- VCC and VCCIO can ramp up together (RVR), if not possible then VCC first followed by VCCIO. The maximum difference between the two voltages should not exceed 0.7V before reaching the final value of VCCIO.
- VDD should be kept low until VCC and VCCIO have reached their minimum voltage values.
- The device must not be selected at power-up (a 10KΩ pull-up Resistor to VCCIO on CS# is recommended). Then a further delay of tPU (Figure 7) until VCC reaches VCC(minimum).
- During Power-up, recovering from power loss or brownout, a delay of tPU is required before normal operation commences (Figure 8).

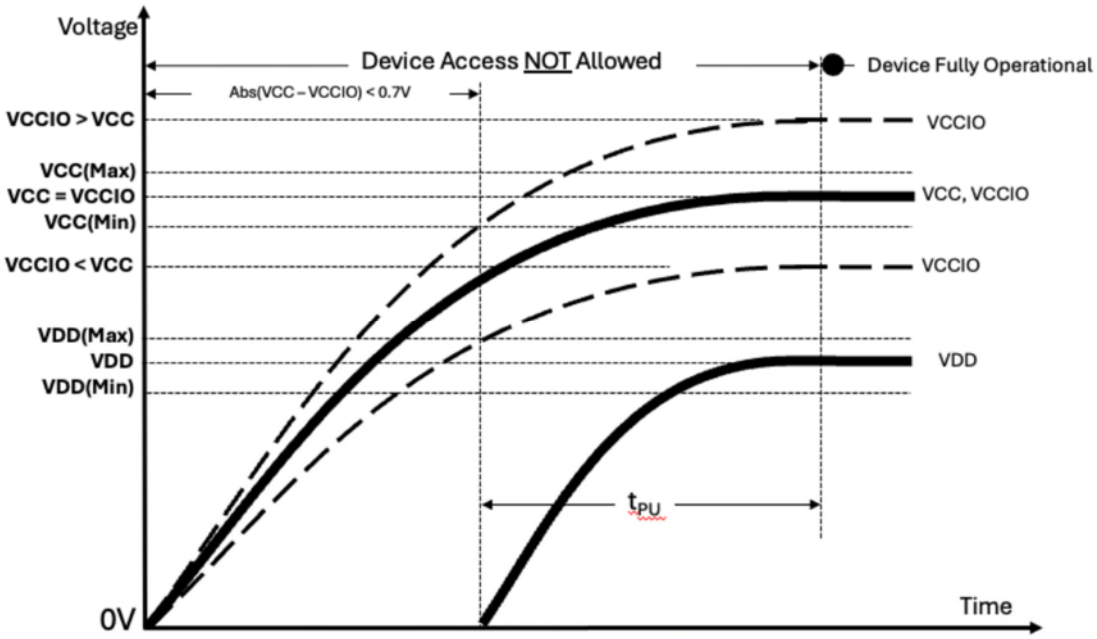


Figure 7: Power-Up Behavior

The following procedure is required to power down the device correctly:

- It is recommended to power down all supplies together. If not possible then the following sequence must be followed 1-VCC, 2 – VCCIO, 3-VDD.
- Timing for Ramp down rate should follow ramp sown time (RVF).
- CS# cannot be active during power-down (a 10KΩ pull-up resistor to VCCIO is recommended).
- It is recommended that no instructions are sent to the device when VCC is below VCC (min).
- During power loss or brownout, if VCC goes below VCC CUT-OFF or VDD goes below VDD CUT-OFF, all supply voltages VCC, VCCIO and VDD must be dropped below their respective (RESET) values VCC_RST, and VDD_RST for a period of tPD. Figure-8 timing needs to be observed for the subsequent power-up.

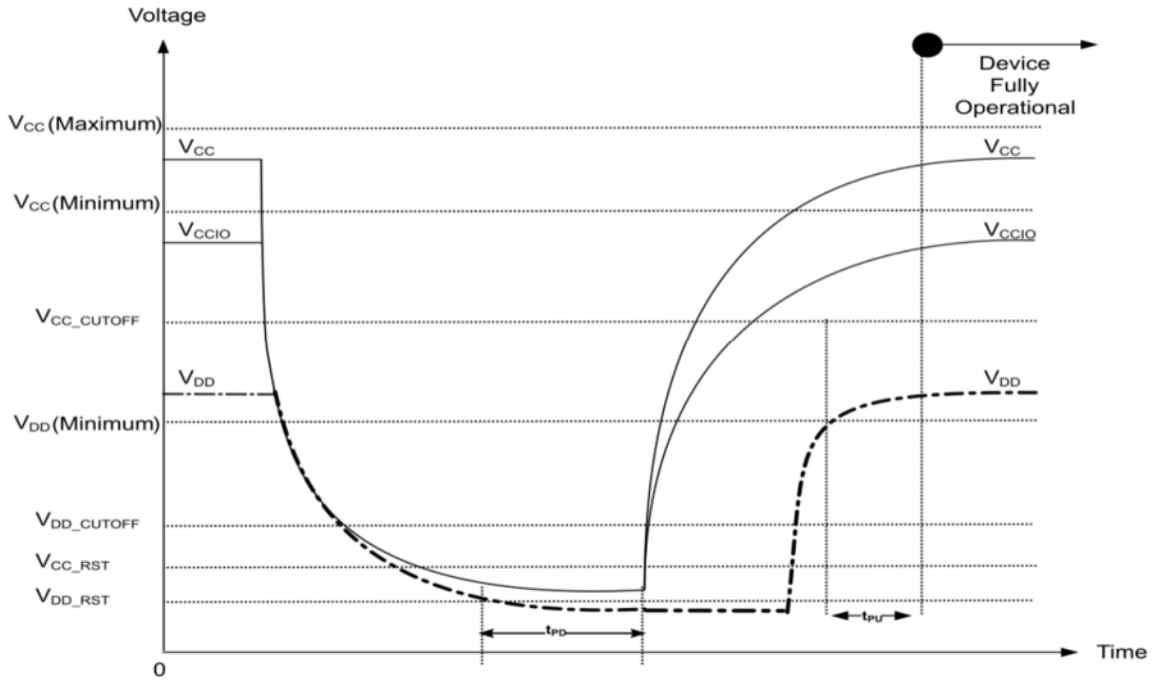


Figure 8: Power-Down Behavior

Table 9: Power Up/Down Timing and Voltages

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
VCC Range		All operating voltages and temperatures	2.5	-	3.6	V
VDD Range			0.85	0.90	0.95	V
VCC Ramp Up Time	RVR		30	-	-	µs/V
VCC Ramp Down Time	RVF		20	-	-	µs/V
VCC Power Up to First Instruction	tPU		250	-	-	µs
VCC (low) time	tPD		1			ms
VCC Cutoff – Must Initialize Device	VCC_CUTOFF		1.6	-	-	V
VCC (Reset)	VCC_RST		0		0.3	V
VDD Cutoff – Must Initialize Device	VDD_CUTOFF		0.6	-	-	V
VDD (Reset)	VDD_RST		0		0.2	V

Memory Map

Table 10: Memory Map

Device Density	Address Range	32-bit Address [31:0]	
512Mb	0000000h – 3FFFFFFh	[31:26] - Logic '0'	[25:0] - Addressable
1Gb	0000000h – 7FFFFFFh	[31:27] - Logic '0'	[26:0] - Addressable
2Gb	0000000h – FFFFFFFh	[31:28] - Logic '0'	[27:0] - Addressable
4Gb	000000h – 1FFFFFFFh	[31:29] - Logic '0'	[28:0] - Addressable

Address Range

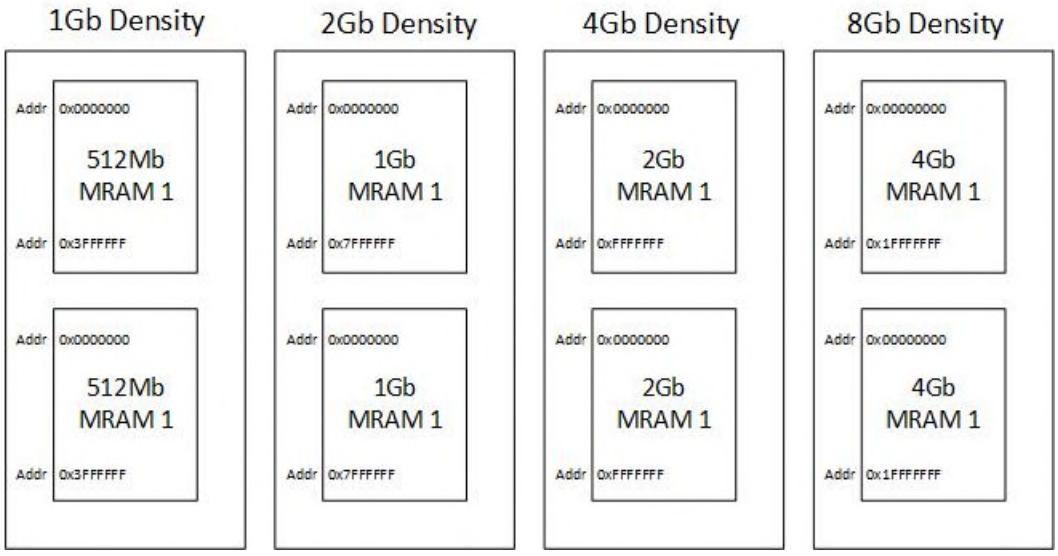


Figure 9: Address Range

Read Any Register Addresses

Table 11: Register Addresses

Register Name	Address
Status Register	0x000000
Interrupt Status Register	0x000001
Configuration Register 1	0x000002
Configuration Register 2	0x000003
Interrupt Configuration Register	0x000004
ECC Test – Data Input Register	0x000005
ECC Test – Error Injection Register	0x000006
ECC Test – Data Output Register	0x000007
ECC Test – Error Count Register	0x000008
Extended Address Register	0x000009
Device Identification Register	0x000030

Hardware Block Protection

The Hardware Block Protect signals (HBP0, HBP1, and HBP2), when driven High or Low, define the size of the memory array to be hardware protected against all Write memory array instructions. When one or more HBP signals are driven High, the relevant memory area, as defined in Table 13 and Table 14 below, becomes protected against all Write memory array instructions. When all three signals, HBP0, HBP1, and HBP2 are driven Low, the memory array is in normal operation without being write-protected.

The Hardware Top/Bottom Select signal (HTBSEL), when driven High or Low, is used in conjunction with the Hardware Block Protect signals (HBP0, HBP1, and HBP2) to determine if the write-protected memory area defined by the state of the HBP signals, starts from the top or the bottom of the memory array:

- When the HTBSEL signal is driven Low, the memory area, protected by the HBP signals, starts from the top of the memory array.
- When the HTBSEL signal is driven High, the memory area, protected by the HBP signals, starts from the bottom of the memory array.

These pins have an internal pull down to Vss. If the pins are left unconnected, the device will have no hardware protection and all regions of the device can be written to (unless the Software Block Protection is activated through the Status Register).

Table 12: Hardware Top Block Protection Address Range Selection (HTBSEL Signal = L)

HBP [2]	HBP [1]	HBP [0]	Protected Portion	512Mb	1Gb	2Gb	4Gb
L	L	L	None	None	None	None	None
L	L	H	Upper 1/64	3F00000h – 3FFFFFFh	7E00000h – 7FFFFFFh	FC00000h – FFFFFFFh	1F800000h – 1FFFFFFFh
L	H	L	Upper 1/32	3E00000h – 3FFFFFFh	7C00000h – 7FFFFFFh	F800000h – FFFFFFFh	1F000000h – 1FFFFFFFh
L	H	H	Upper 1/16	3C00000h – 3FFFFFFh	7800000h – 7FFFFFFh	F000000h – FFFFFFFh	1E000000h – 1FFFFFFFh
H	L	L	Upper 1/8	3800000h – 3FFFFFFh	7000000h – 7FFFFFFh	E000000h – FFFFFFFh	1C000000h – 1FFFFFFFh
H	L	H	Upper 1/4	3000000h – 3FFFFFFh	6000000h – 7FFFFFFh	C000000h – FFFFFFFh	18000000h – 1FFFFFFFh
H	H	L	Upper 1/2	2000000h – 3FFFFFFh	4000000h – 7FFFFFFh	8000000h – FFFFFFFh	10000000h – 1FFFFFFFh
H	H	H	All	0000000h – 3FFFFFFh	000000h – 7FFFFFFh	000000h – FFFFFFFh	0000000h – 1FFFFFFFh

Table 13: Hardware Bottom Block Protection Address Range Selection (HTBSEL Signal = H)

HBP [2]	HBP [1]	HBP [0]	Protected Portion	512Mb	1Gb	2Gb	4Gb
L	L	L	None	None	None	None	None
L	L	H	Lower 1/64	000000h – 0FFFFFh	000000h – 01FFFFFh	000000h – 03FFFFFh	000000h – 07FFFFFh
L	H	L	Lower 1/32	000000h – 01FFFFFh	000000h – 03FFFFFh	000000h – 07FFFFFh	000000h – 0FFFFFFh
L	H	H	Lower 1/16	000000h – 03FFFFFh	000000h – 07FFFFFh	000000h – 0FFFFFFh	000000h – 1FFFFFFh
H	L	L	Lower 1/8	000000h – 07FFFFFh	000000h – 0FFFFFFh	000000h – 1FFFFFFh	000000h – 3FFFFFFh
H	L	H	Lower 1/4	000000h – 0FFFFFFh	000000h – 1FFFFFFh	000000h – 3FFFFFFh	000000h – 7FFFFFFh
H	H	L	Lower 1/2	000000h – 1FFFFFFh	000000h – 3FFFFFFh	000000h – 7FFFFFFh	000000h – FFFFFFFh
H	H	H	All	000000h – 3FFFFFFh	000000h – 7FFFFFFh	000000h – FFFFFFFh	0000000h – 1FFFFFFFh

Notes:
High (H): Logic ‘1’
Low (L): Logic ‘0’

Register Map

Status Register / Device Protection Register (Read/Write)

Status register is a legacy SPI register and contains options for enabling/disabling data protection.

The WREN bit must be set to "1" to enable write operations. This bit can only be set by executing the Write Enable (WREN) instruction opcode.

The device supports Back-to-Back write operations: WREN is prerequisite to only the first Memory Array Write instruction. The WREN bit doesn't clear to "0" following subsequent memory write opcodes. WREN disable instruction must be executed to reset WREN.

Table 14 : Status Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Selection Options
SR[7]	WP#EN	Hardware Based WP# Protection Enable/Disable	R/W	0	1: Protection Enabled – write protects when WP# is Low 0: Protection Disabled – unprotected
SR[6]	RSVD	Reserved	R	0	Reserved for future use
SR[5]	TBPSEL	Software Top/Bottom Memory Array Protection Selection	R/W	0	1: Bottom Protection Enabled (Lower Address Range) 0: Top Protection Enabled (Higher Address Range)
SR[4]	BPSEL[2]	Block Protect Selection Bit 2	R/W	0	Block Protection Bits (Table 16, Table 17)
SR[3]	BPSEL[1]	Block Protect Selection Bit 1	R/W	0	
SR[2]	BPSEL[0]	Block Protect Selection Bit 0	R/W	0	
SR[1]	WREN	Write Operation Protection Enable/Disable	R	0	1: Write Operation Protection Disabled 0: Write Operation Protection Enabled
SR[0]	RSVD	Reserved	R	0	Reserved for future use

Software Block Protection

These 4 bits are OR'ed with the Hardware Protection Bits and can be used to dynamically protect regions of memory.

Table 15: Software Top Block Protection Address Range Selection (TBPSEL=0)

BPSEL [2]	BPSEL [1]	BPSEL [0]	Protected Portion	512Mb	1Gb	2Gb	4Gb
0	0	0	None	None	None	None	None
0	0	1	Upper 1/64	3F00000h – 3FFFFFFh	7E00000h – 7FFFFFFh	FC00000h – FFFFFFFh	1F800000h – 1FFFFFFFh
0	1	0	Upper 1/32	3E00000h – 3FFFFFFh	7C00000h – 7FFFFFFh	F800000h – FFFFFFFh	1F000000h – 1FFFFFFFh
0	1	1	Upper 1/16	3C00000h – 3FFFFFFh	7800000h – 7FFFFFFh	F000000h – FFFFFFFh	1E000000h – 1FFFFFFFh
1	0	0	Upper 1/8	3800000h – 3FFFFFFh	7000000h – 7FFFFFFh	E000000h – FFFFFFFh	1C000000h – 1FFFFFFFh
1	0	1	Upper 1/4	3000000h – 3FFFFFFh	6000000h – 7FFFFFFh	C000000h – FFFFFFFh	18000000h – 1FFFFFFFh
1	1	0	Upper 1/2	2000000h – 3FFFFFFh	4000000h – 7FFFFFFh	8000000h – FFFFFFFh	10000000h – 1FFFFFFFh
1	1	1	All	0000000h – 3FFFFFFh	000000h – 7FFFFFFh	000000h – FFFFFFFh	0000000h – 1FFFFFFFh

Table 16: Software Bottom Block Protection Address Range Selection (TBPSEL=1)

BPSEL [2]	BPSEL [1]	BPSEL [0]	Protected Portion	512Mb	1Gb	2Gb	4Gb
0	0	0	None	None	None	None	None
0	0	1	Lower 1/64	000000h – 0FFFFFh	000000h – 01FFFFFh	000000h – 03FFFFFh	000000h – 07FFFFFh
0	1	0	Lower 1/32	000000h – 01FFFFFh	000000h – 03FFFFFh	000000h – 07FFFFFh	000000h – 0FFFFFFh
0	1	1	Lower 1/16	000000h – 03FFFFFh	000000h – 07FFFFFh	000000h – 0FFFFFFh	000000h – 1FFFFFFh
1	0	0	Lower 1/8	000000h – 07FFFFFh	000000h – 0FFFFFFh	000000h – 1FFFFFFh	000000h – 3FFFFFFh
1	0	1	Lower 1/4	000000h – 0FFFFFFh	000000h – 1FFFFFFh	000000h – 3FFFFFFh	000000h – 7FFFFFFh
1	1	0	Lower 1/2	000000h – 1FFFFFFh	000000h – 3FFFFFFh	000000h – 7FFFFFFh	000000h – FFFFFFFh
1	1	1	All	000000h – 3FFFFFFh	000000h – 7FFFFFFh	000000h – FFFFFFFh	0000000h – 1FFFFFFFh

Table 17: Software Write Protection Modes

WREN (Status Register)	WP#EN (Status Register)	WP# (Pin)	Status & Configuration	Memory [1] Array Protected	Memory [1] Array Unprotected
0	X	X	Protected	Protected	Protected
1	0	X	Unprotected	Protected	Unprotected
1	1	Low	Protected	Protected	Unprotected
1	1	High	Unprotected	Protected	Unprotected

Notes:
High: Logic '1'
Low: Logic '0'
X: Don't Care – Can be Logic '0' or '1'
Protected: Write protected
Unprotected: Writable
1. Memory address range protection based on Block Protection Bits

Extended Address Register (Read/Write)

For the 3-byte addressing mode, the extended address register provides a fourth address byte A[31:24] to enable the host to access memory area beyond 128Mb. The extended address register bits [4:0] operate as memory address bit A[24:28] to select one of thirty two 128Mb segments of the memory array.

The value of the extended address register does not change when a 3-byte read operation crosses the selected 128Mb boundary.

Table 18: Extended Address Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Selection Options
[7:5]	A[31:29]	Reserved	R/W	00000000	000
[4:0]	A[28:24]	Enables specified 128Mb memory segment Up to 4Gb			11111: 32rd Highest 128Mb segment (1F000000h – 1FFFFFFFh) 11110: 31th 128Mb segment (1E000000h – 1EFFFFFFh) 11101: 30th 128Mb segment (1D000000h – 1DFFFFFFh) 11100: 29th 128Mb segment (1C000000h – 1CFFFFFFh) 10111: 28th 128Mb segment (1B000000h – 1BFFFFFFh) 11010: 27th 128Mb segment (1A000000h – 1AFFFFFFh) 11001: 26th 128Mb segment (19000000h – 19FFFFFFh) 11000: 25th 128Mb segment (18000000h – 18FFFFFFh) 10111: 24th 128Mb segment (17000000h – 17FFFFFFh) 10110: 23th 128Mb segment (16000000h – 16FFFFFFh) 10101: 22th 128Mb segment (15000000h – 15FFFFFFh) 10100: 21th 128Mb segment (14000000h – 14FFFFFFh) 10011: 20th 128Mb segment (13000000h – 13FFFFFFh) 10010: 19th 128Mb segment (12000000h – 12FFFFFFh) 10001: 18th 128Mb segment (11000000h – 11FFFFFFh) 10000: 17th 128Mb segment (10000000h – 10FFFFFFFh) 01111: 16th 128Mb segment (0F000000h – 0FFFFFFFh) 01110: 15th 128Mb segment (0E000000h – 0EFFFFFFh) 01101: 14th 128Mb segment (0D000000h – 0DFFFFFFh) 01100: 13th 128Mb segment (0C000000h – 0CFFFFFFh) 01011: 12th 128Mb segment (0B000000h – 0BFFFFFFh) 01010: 11th 128 Mb segment (0A000000h – 0AFFFFFFh) 01001: 10th 128Mb segment (09000000h – 09FFFFFFh) 01000: 9th 128Mb segment (08000000h – 08FFFFFFh) 00111: 8th 128Mb segment (07000000h – 07FFFFFFh) 00110: 7th 128Mb segment (06000000h – 06FFFFFFh) 00101: 6th 128Mb segment (05000000h – 05FFFFFFh) 00100: 5th 128Mb segment (04000000h - 04FFFFFFh) 00011: 4th 128Mb segment (030000000h – 03FFFFFFh) 00010: 3rd 128Mb segment (02000000h – 02FFFFFFh) 00001: 2nd 128Mb segment (01000000h – 01FFFFFFh) 00000: Lowest 128Mb segment (00000000h – 00FFFFFFh)

Flag Status Register (Read Only)

Flag status register contains device's access status and addressing information.

Table 19: Flag Status Register – Read Only

Bits	Name	Description	Read / Write	Default State	Selection Options
FSR1[7]	ST	Device Access Status	R	1	1: Ready 0: Busy
FSR1[6:1]	RSVD	Reserved	R	0	Reserved for future use
FSR1[0	RSVD	Reserved	R	0	Reserved for future use

Device Identification Register (Read Only)

Unique Identification register contains a number unique to every device.

Table 20 : Device ID Register – Read Only

Bits	Manufacturer ID	Device Configuration				
ID[31:0]	ID[31:24]	Interface	Voltage	Temp	Density	Freq
		ID[23:20]	ID[19:16]	ID[15:12]	ID[11:8]	ID[7:0]

Manufacturer ID	Interface	Voltage	Temperature	Density	Frequency
31-24	23-20	19-16	15-12	11-8	7-0
1110 0110	0010-HP Dual-Quad SPI	0001 - 3V	0010 - -40°C to 125°C	0110 - Reserved	00000001 - 100MHz
				1000 - 1Gb	
				1001 – 2Gb	
				1010 – 4Gb	
				1100 – 8Gb	

Configuration Register 1 (Read/Write)

Configuration Register 1 (CR1) controls the output drive strength selection, locking/unlocking data protection options set in the Status register. Once locked, the protection options cannot be changed in the Status register. In addition, CR1 controls the Write Enable protection (WREN – Status Register) reset functionality during memory array writing[1]. This functionality makes SPI MRAM compatible to other SPI devices.

Table 21: Configuration Register 1 (CR1) – Read and Write

Bits	Name	Description	Read / Write	Default	Selection Options
CR1[7]	ODSEL[2]	Output Driver Strength Selector	R/W	1	**VCCIO=** **1.8V** **2.5V** 000: 1mA 2.5mA 001: 3mA 5mA 010: 5mA 10mA 011: 7mA 14mA 100: 1mA 2.5mA 101: 3mA 5mA 110: 5mA 10mA 111: 7mA 14mA
CR1[6]	ODSEL[1]			1	
CR1[5]	ODSEL[0]			1	
CR1[4]	RSVD	Reserved	R	0	Reserved for future use
CR1[3]	RSVD	Reserved	R	0	Reserved for future use
CR1[2]	MAPLK	Status Register Lock Enable/Disable (TBSEL, BPSEL[2:0]	R/W	0	1: Lock TBSEL and BPSEL[2:0] 0: Unlock TBSEL and BPSEL[2:0]
CR1[1]	WRENS[1]	WREN Reset Selector (Memory Array Write Functionality)	R/W	0	**00:** Normal: WREN is prerequisite to all Memory Array Write instruction. (WREN is reset after CS# goes High) **01:** SRAM: WREN is not a prerequisite to Memory Array Write instruction (WREN is ignored) **10:** Back-to-Back: WREN is prerequisite to only the first Memory Array Write instruction. WREN disable instruction must be executed to reset WREN. (WREN does not reset once CS# goes High) **11:** Illegal - Reserved for future use
CR![0]	WRENS[0]			0	

Notes:

1. Write Enable protection (WREN – Status Register) for Registers is maintained irrespective of the Configuration Register 1 settings. In other words, all register write instructions require WREN to be set and WREN resets once CS# goes High for the write instruction.

Configuration Register 2 (Read/Write)

Configuration Register 2 (CR2) controls the memory array access latency.

Table 22: Configuration Register 2 (CR2) – Read and Write

Bits	Name	Description	Read / Write	Default State	Selection Options
CR2[7]	RSVD	Reserved	R	0	Reserved for future use
CR2[6]	RSVD	Reserved	R	0	Reserved for future use
CR2[5]	RSVD	Reserved	R	0	Reserved for future use
CR2[4]	RSVD	Reserved	R	0	Reserved for future use
CR2[3]	MLATS[3]	Memory Array Read/Read Any Register Latency Selection [1]	R/W	1	0000: 0 Cycles 0001: 1 Cycles 0010: 2 Cycles 0011: 3 Cycles 0100: 4 Cycles 0101: 5 Cycles 0110: 6 Cycles 0111: 7 Cycles 1000: 8 Cycles – Default 1001: 9 Cycles 1010: 10 Cycles 1011: 11 Cycles 1100: 12 Cycles 1101: 13 Cycles 1110: 14 Cycles 1111: 15 Cycles
CR2[2]	MLATS[2]			0	
CR2[1]	MLATS[1]			0	
CR2[0]	MLATS[0]			0	

Notes:

1. Latency is frequency dependent. Please consult Table 29, 30 and 31

Interrupt Configuration Register (Read/Write)

The Interrupt Configuration Register controls different events that trigger INT# pin transitioning from High to Low state. INT# pin can be configured in the INT# configuration register to transition to the active Low state when either ECC error is detected and not corrected or transitioning from the busy to the ready state.

This register also enables access to 1 of 4 die sitting on the internal bus. The ECC engine can be tested be enabling the Test Enable bit and selecting 1 of 4 die.

Table 23: Interrupt Configuration Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Selection Options
INTCR[7]	INTRF	Shows status of ECC error detection	R	0	Selection Options: 1: Unrecoverable ECC error detected 0: No unrecoverable ECC error detected
INTCR[6]	INTR	Clear Interrupt Status	W	0	Selection Options: 1 = Resets Interrupt caused by unrecoverable ECC 0 = No Action
INTCR[5]	ECC_CR	Reset the ECC Error Count Register	W	0	Selection Options: 1 = Resets ECC count register to 0 0 = No Action
INTCR[4]	----	Reserved	-	-	-
INTCR[3:2]	ECCDS	Die Selection	W	0	Die Select Options: 11 = Die 4 selected 10 = Die 3 selected 01 = Die 2 selected 00 = Die 1 selected
INTCR[1]	ECCTE	ECC Test Enable	W	0	ECC Test Engine Test mode: 1 = Enable 0 = Disable
INTCR[0]	ECCDS	ECC Error Detection Selection	W	0	Selection Options: 1 = ECC detection will transition a High to Low state on the INT# pin 0 = ECC detection will not transition the INT# pin

Error Correction Code (ECC) Test – Data Input Register

The contents of this register are entered into the ECC engine data buffer i.e. used as data input to test the ECC engine.

Table 24: ECC Test Data Input Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Select Options
[31:0]	ECC_Data_In	Data Input	R/W	32’b0	Any value from 0x00000000 to 0xFFFFFFFF

Error Correction Code (ECC) Test – Error Injection

The contents of this register are used as an error mask to inject error to test the ECC engine.

Table 25: ECC Test Error Injection Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Select Options
[31:0]	ECC_Error_Injection	Error Mask	R/W	32'b0	1 in any position injects an error into ECC engine. For example, 0x00000003 will inject a two-bit error in two LSB bits i.e. the Data in the ECC engine buffer is Exclusive or'd with the error mask.

Error Correction Code (ECC) Test – Data Output Register

The contents of this register are the output of the ECC engine when testing the ECC engine.

Table 26: ECC Test Data Output Register – Read Only

Bits	Name	Description	Read / Write	Default State	Select Options
[31:0]	ECC_Data_Out	Output of ECC engine	R	32'b0	None – read only.

Error Correction Code (ECC) – Error Count Register

This register must only be used during TEST MODE for testing the ECC engine. The Error Count Register is incremented when uncorrectable ECC errors are induced during the test mode. During normal operation of the device, the content of this register is not reflective of corrected or uncorrected errors. An interrupt is generated on device pin INT# and the interrupt flag is set when an unrecoverable error is detected in test mode.

Table 27: ECC Count Register – Read Only

Bits	Name	Description	Read / Write	Default State	Select Options
[31:0]	Error_Count	Number of induced uncorrectable Errors detected during TEST mode	R	32'b0	None – read only

Table 28: Memory Array Read Latency Cycles vs. Maximum Clock Frequency (with XIP)

Read Type	Latency	Max Frequency
(1-1-1) SDR	12-15	100MHz
(1-1-1) DDR	8-15	50MHz
(1-4-4) SDR	12-15	100MHz
(1-4-4) DDR	8-15	50MHz
(4-4-4) SDR	12-15	100MHz
(4-4-4) DDR	8-15	50MHz

Table 29: Memory Read Latency Cycles vs. Maximum Clock Frequency (without XIP)

Read Type	Latency	Max Frequency
(1-1-1) SDR	0	50MHz

Table 30 : Read Any Register Command Latency Cycles vs. Maximum Clock Frequency

Read Type	Latency Cycles	Max Frequency
(1-1-1) SDR	8-15	100MHz
(1-4-4) SDR	8-15	100MHz
(4-4-4) SDR	8-15	100MHz

Instruction Set

Table 31: Instruction Set

#	Instruction Name	Command (Opcode)	(1-0-0)	(1-0-1)	(1-1-1)	(1-1-4)	(1-4-4)	(4-0-0)	(4-4-4)	XIP Byte	SDR	DDR	Latency Cycles	Address Byte	Data Bytes	Max. Frequency	Prerequisite	Note
1	No Operati	NOOP 00h	•					•			•			0		100 MHz		
2	Write Enable	WREN 06h	•					•			•			0		100 MHz		
3	Write Disable	WRDI 04h	•					•			•			0		100 MHz		
4	Enable QPI	QPIE 38h	•								•			0		100 MHz		
5	Enable SPI	SPIE FFh	•					•			•			0		100 MHz		
6	Read Status	RDSR 05h		•							•			0	1	50 MHz		
7	Read Flag	RDSFR 70h			•				•		•			0	1	50 MHz		
8	Read Device	RDID 9Fh		•							•			0	4	50 MHz		
9	Read Any	RDAR 65h			•				•		•		•	4	1	100 MHz		
10	Write Status	WRSR 01h		•							•			0	1	100 MHz	WREN	
11	Write Any	WRAR 71h			•				•		•			4	1	100 MHz	WREN	

#	Instruction Name	Command (Opcode)	(1-0-0)	(1-0-1)	(1-1-1)	(1-1-4)	(1-4-4)	(4-0-0)	(4-4-4)	XIP Byte	SDR	DDR	Latency Cycles	Address Byte	Data Bytes	Max. Frequency	Prerequisite	Note
12	Read Memor	READ 03h			•						•			4	1 to ∞	50 MHz		1,2
13	Read Memor	READ 13h			•						•			4	1 to ∞	50 MHz		1,2,5
14	Fast Read	RDFT 0Bh			•				•		•		•	3	1 to ∞	100 MHz		1,2,3,5
15	Fast Read	RDFT 0Ch			•				•		•		•	4	1 to ∞	100 MHz		1,2,3,5
16	Fast Read	DRFR 0Dh			•				•	•		•	•	4	1 to ∞	50 MHz		1,2,3
17	Read Quad	RDQO 6Bh				•					•		•	3	1 to ∞	100 MHz		1,2,3,5
18	Read Quad	RDQO 6Ch				•					•		•	4	1 to ∞	100 MHz		1,2,3,5
19	Read Quad	RDQI EBh					•			•	•		•	4	1 to ∞	100 MHz		1,2,3
20	Read Quad	DRQI EDh					•			•		•	•	4	1 to ∞	50 MHz		1,2,3
21	Write Memor	WRTE 02h			•				•		•			4	1 to ∞	100 MHz	WREN	1,4
22	Fast Write	4WRFT DAh			•				•	•	•			4	1 to ∞	100 MHz	WREN	1,2,4
23	Fast Write	4DRFW DEh			•				•	•		•		4	1 to ∞	50 MHz	WREN	1,2,4
24	Write Quad	4WQIO D2h					•			•	•			4	1 to ∞	100 MHz	WREN	1,2,4

#	Instruction Name	Command (Opcode)	(1-0-0)	(1-0-1)	(1-1-1)	(1-1-4)	(1-4-4)	(4-0-0)	(4-4-4)	XIP Byte	SDR	DDR	Latency Cycles	Address Byte	Data Bytes	Max. Frequency	Prerequisite	Note
25	Write Quad	4DWQO					•			•		•		4	1 to ∞	35	WREN	1,2,4

Notes:

1. A typical SPI instruction consists of command, address and data components. The bus width to transmit these three components varies based on the SPI interface mode selected. To accurately represent the number of I/Os used to transmit these three components, a nomenclature (command-address-data) is adopted and used throughout this document. Integers placed in the (command-address-data) fields represent the number of I/Os used to transmit the particular component. As an example, 1-1-1 means command, address and data are transmitted on a single I/O Dual-Quad SPI device 1 (SI / IO[0] or SO / IO[1]) and Dual-Quad SPI device 2 (SI / IO[04 or SO / IO[7]). On the other hand, 1-4-4 represents command being sent on a single I/O Dual-Quad SPI device 1 (SI / IO[0]) and Dual-Quad SPI device 2 (SI / IO[4]) - address/data being sent on four I/Os of Dual-Quad SPI device 1 (IO[3:0]) and Dual-Quad SPI device 2 (IO[7:4])
2. XIP allows completing a series of read and write instructions without having to individually load the read or write command for each instruction. A special mode byte must be entered after the address bits to enable/disable XIP – Axh / Fxh.
3. Fast Read instruction must include Latency cycles to meet higher frequency. They are configurable (Configuration Register 2 – CR2[3:0]) and frequency dependent.
4. WREN prerequisite for array writing is configurable (Configuration Register 1– CR1[1:0])
5. Support legacy device boot on Xilinx platforms

Instruction Description and Structures

All communication between a host and UT8MRQRHxG is in the form of instructions. Instructions define the operation that must be executed. Instructions consist of a command followed by an optional address modifier and data transfer to or from UT8MRQRHxG. All command, address and data information are transferred sequentially. Instructions are structured as follows:

- Each instruction begins with CS# going Low (logic '0') and ends with CS# returning High (Logic'1').
- CLK marks the transfer of each bit.
- Each instruction starts out with an 8-bit command. The command selects the type of operation UT8MRQRHxG must perform. The command is transferred on the rising edges of CLK.
- The command can be stand alone or followed by address to select a memory location or register. The address is 4-byte (32-bit).
  - SDR: The address is transferred on the rising edges of CLK.
  - DDR: The address is transferred on both edges of the CLK in DDR.
- The address bits are followed by data bits. For Write instructions:
  - SDR: Write data bits to UT8MRQRHxG are transferred on the rising edges of CLK.
  - DDR: Write data bits to UT8MRQRHxG are transferred on both edges of CLK.
- In normal operational mode, Write instructions must be preceded by the WREN instruction. WREN instruction sets the WREN bit in the Status register. WREN bit is reset at the end of every Write instruction. WREN bit can also be reset by executing the WRDI instruction. UT8MRQRHxG offers two other modes, namely SRAM and Back-to-Back Write where WREN does not get reset after a write instruction to the memory array. These modes are set in Configuration Register 1.
- Similar to write instructions, the address bits are followed by data bits for read instructions:
  - SDR: Read data bits from UT8MRQRHxG are transferred on the falling edges of CLK.
  - DDR: Read data bits from UT8MRQRHxG are transferred on both edges of CLK. The start of read data transfer is always on the falling edge of the CLK.
- UT8MRQRHxG is a high-performance serial memory and at higher frequencies, read instructions require latency cycles to compensate for the memory array access time. The number of latency cycles required depends on the operational frequency and is configurable – Configuration Register 2. The latency cycles are inserted after the address bits before the data comes out of UT8MRQRHxG.
- For Read and Write instructions, UT8MRQRHxG offers XIP mode. XIP allows similar instructions to be executed sequentially without incurring the command cycles overhead. XIP is enabled by entering byte Axh and disabled by entering byte Fxh. These respective bytes must be entered following the address bits.
- The entire memory array can be read from or written to using a single read or write instruction. After the staring address is entered, subsequent address is internally incremented as long as CS# is Low and CLK continues to cycle.
- All commands, address and data are shifted with the most significant bit first.

Figure 10 to Figure 18 show the description of SDR instruction types supported.

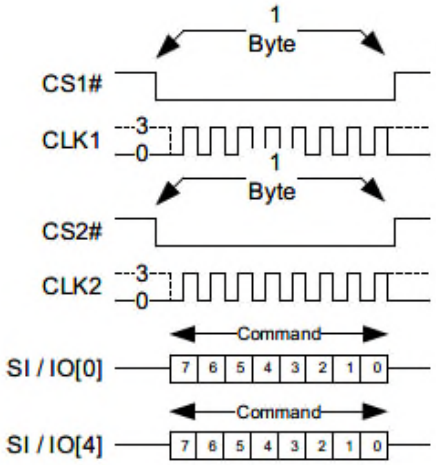


Figure 10: Description of (1-0-0) Instruction Type

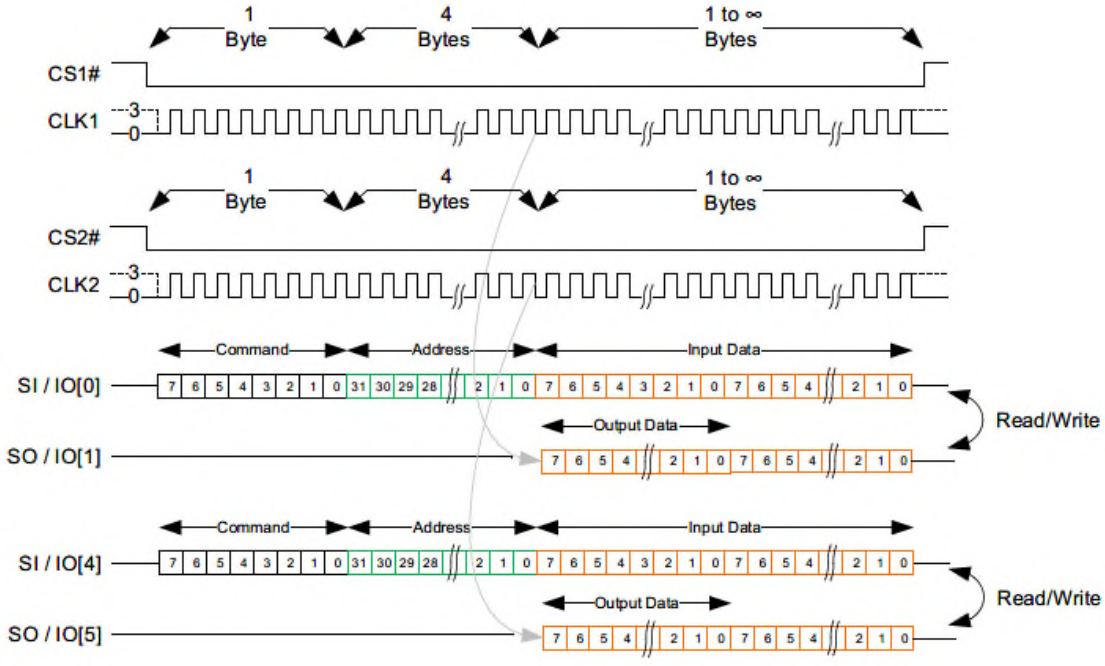


Figure 11: Description of (1-0-1) Instruction Type

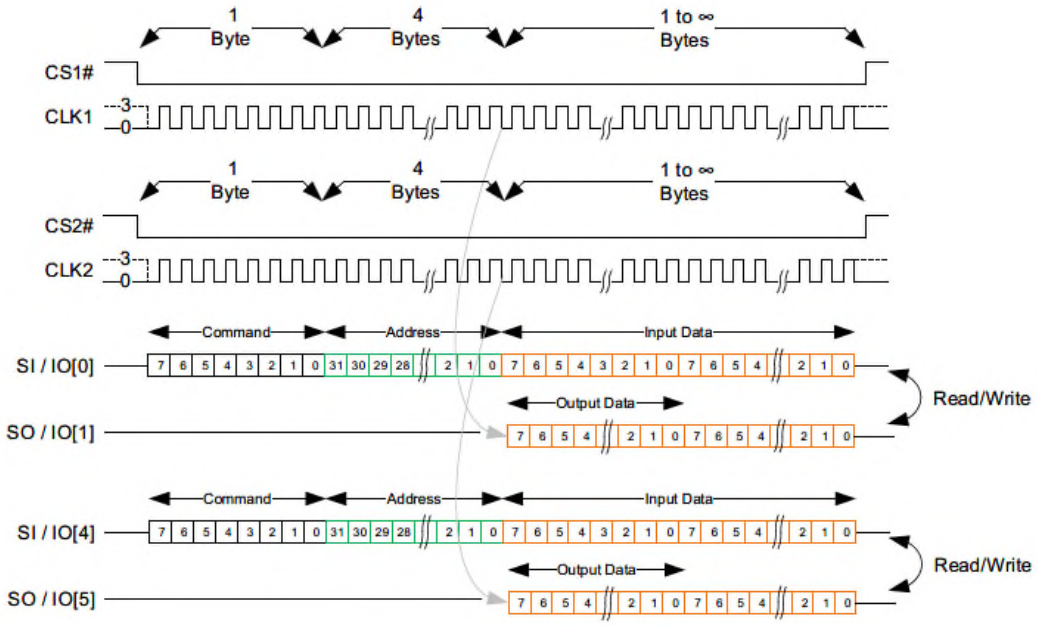


Figure 12: Description of (1-1-1) Instruction Type (Without XIP)

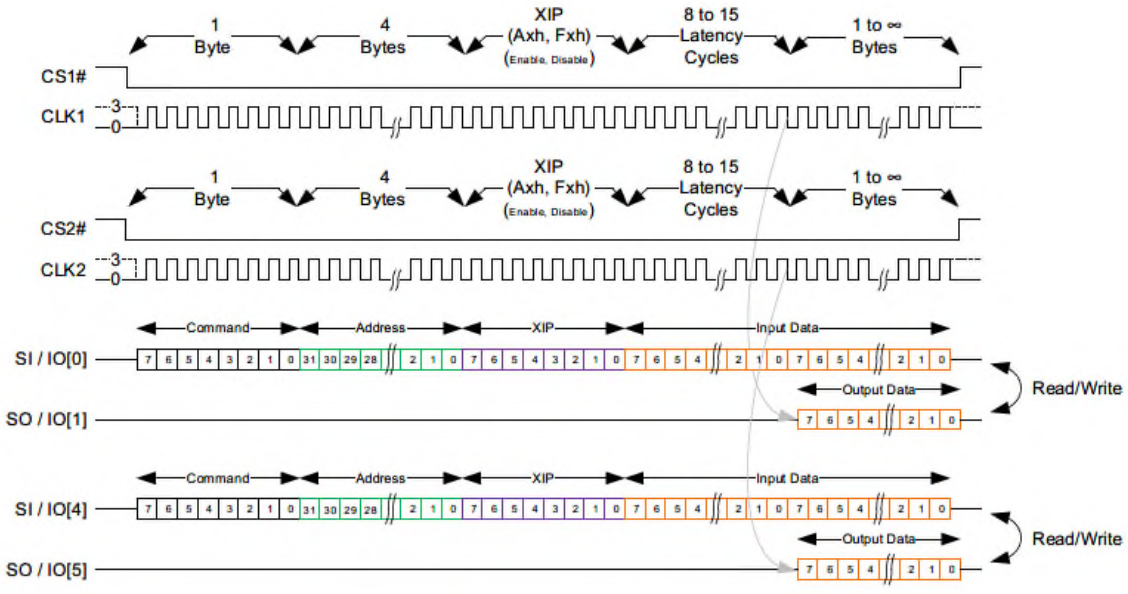


Figure 13: Description of (1-1-1) Instruction Type (With XIP)

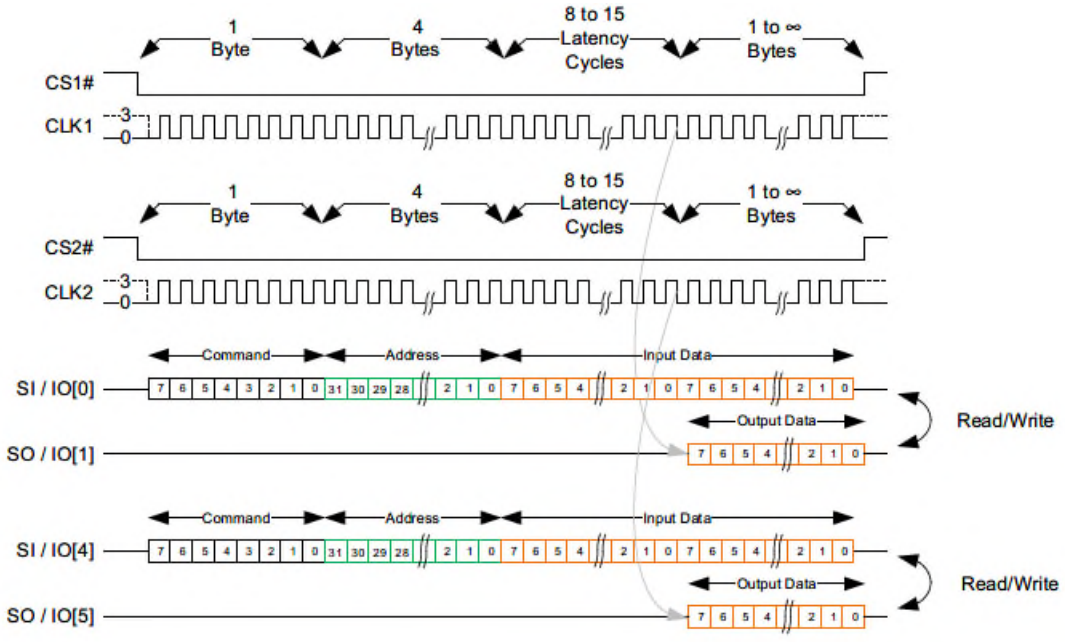


Figure 14: Description of (1-1-1) Instruction Type (Without XIP)

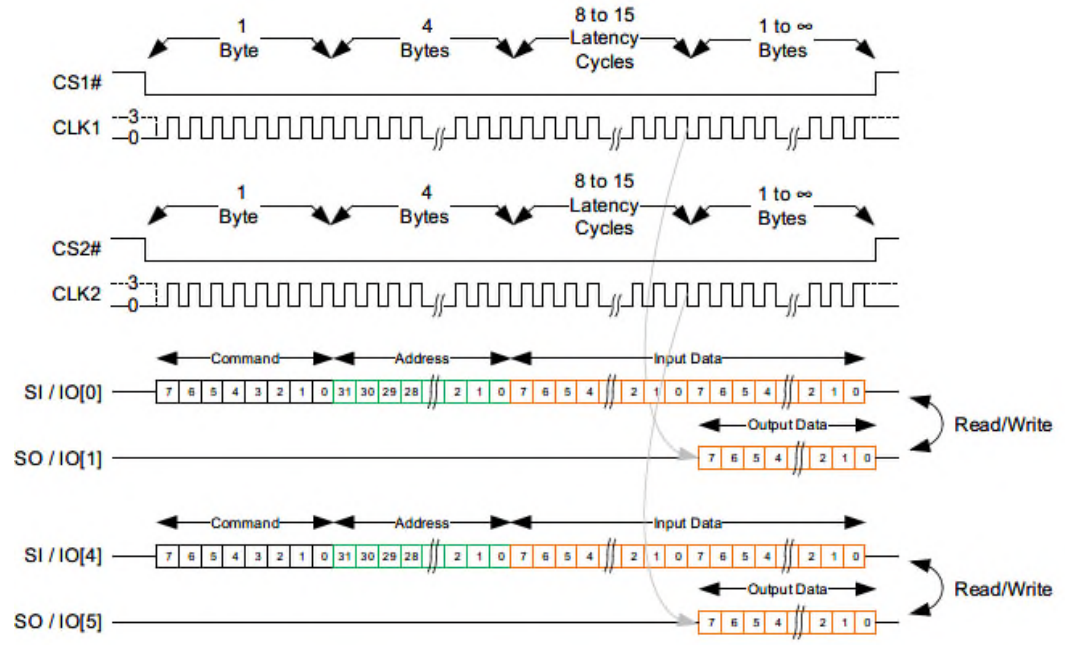


Figure 15: Description of (1-1-4) Instruction Type (Without XIP)

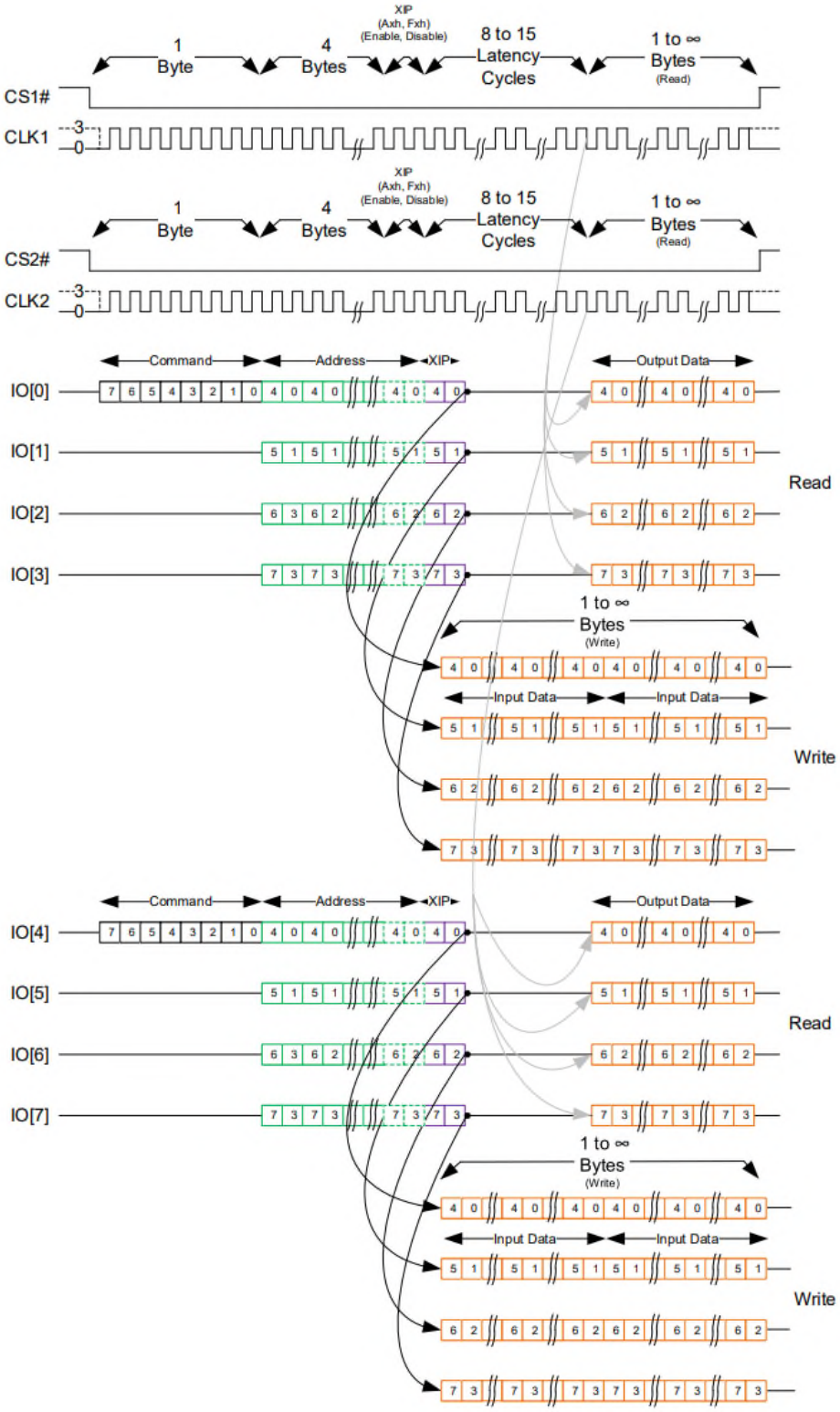


Figure 16: Description of (1-4-4) Instruction Type (With XIP)

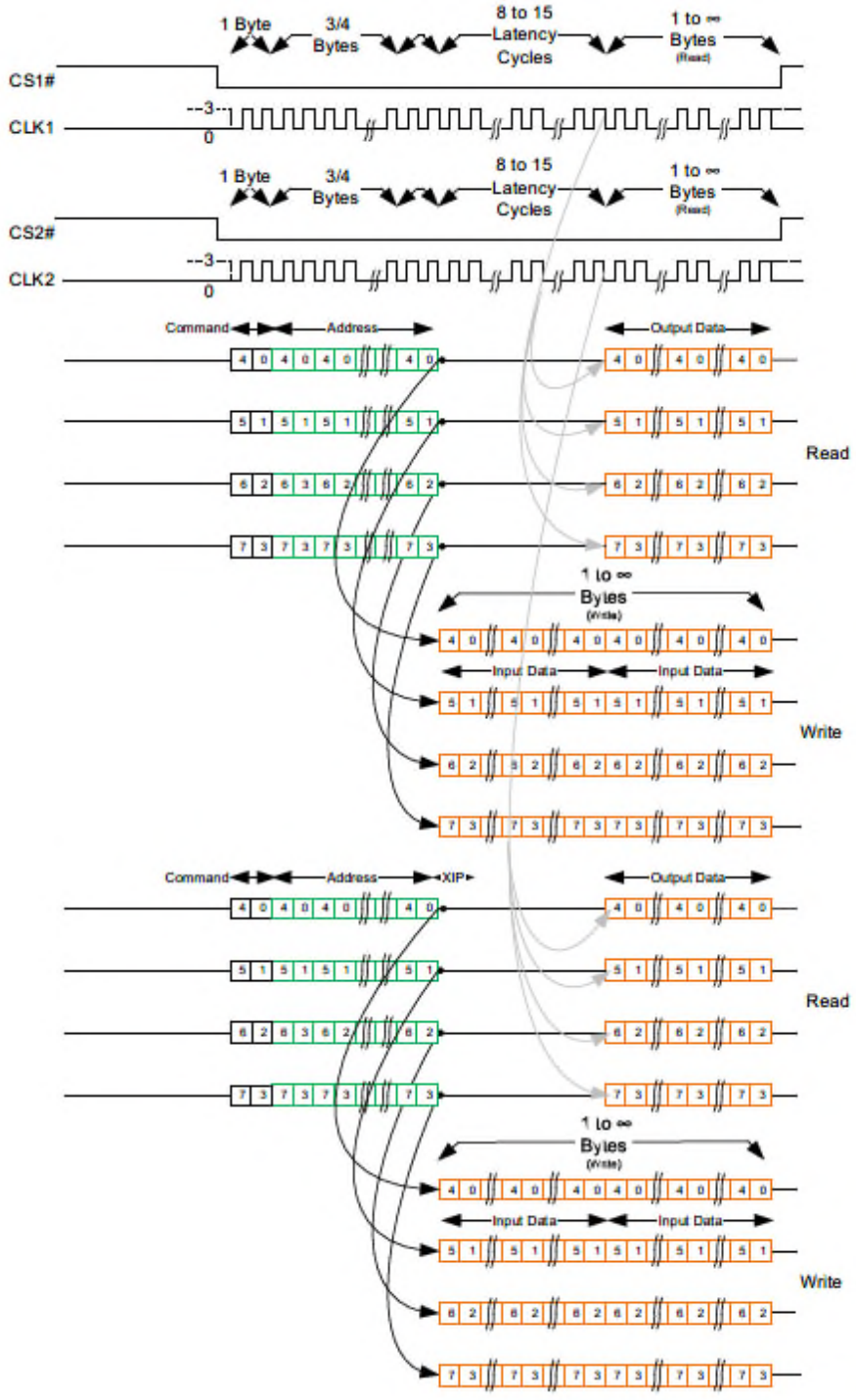


Figure 17: Description of (4-4-4) Instruction Type (Without XIP)

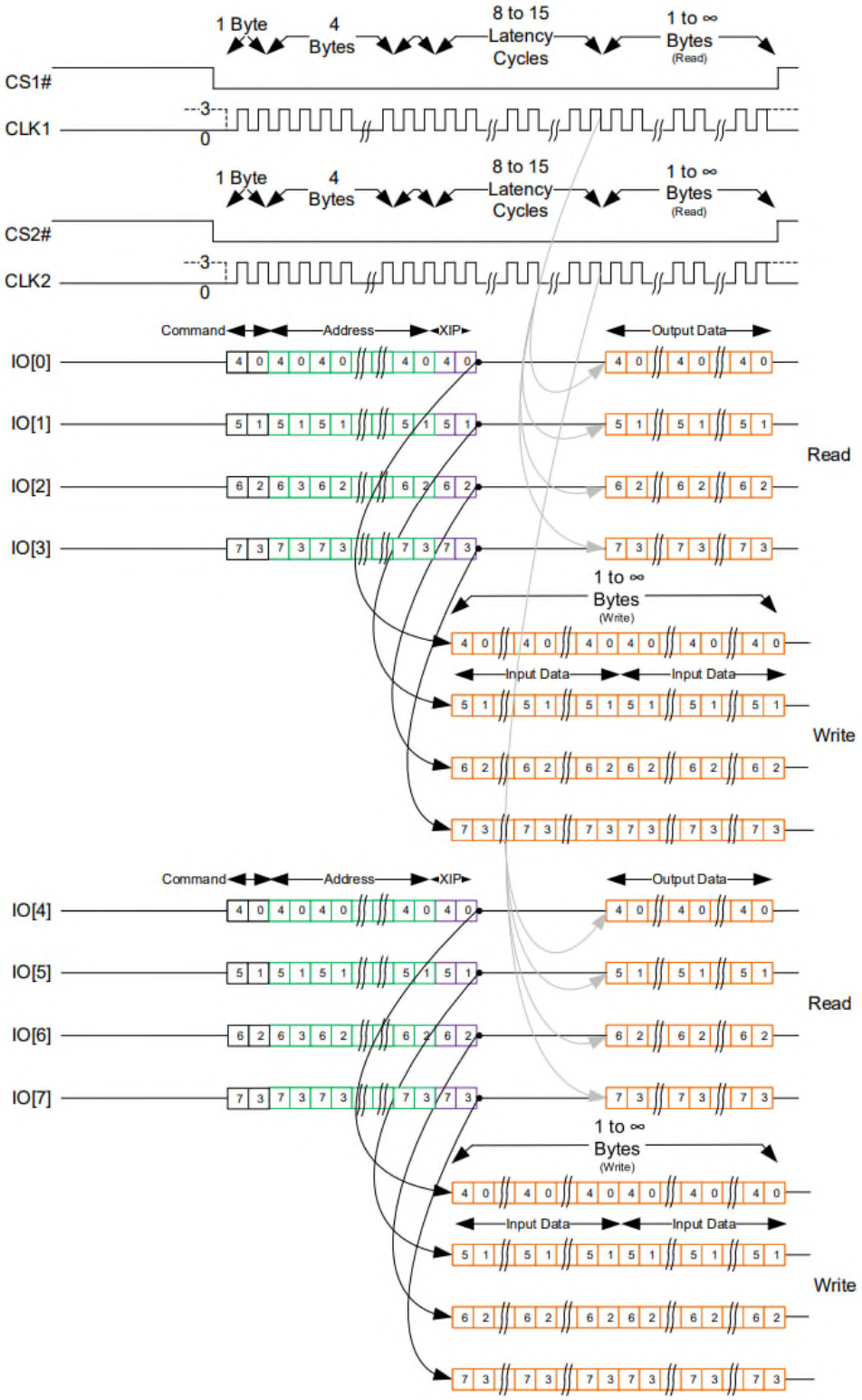


Figure 18: Description of (4-4-4) Instruction Type (With XIP)

Figure 19 to Figure 20 show the description of DDR instruction types supported

Figure 21: Description of (1-1-1) DDR Instruction Type (With XIP)

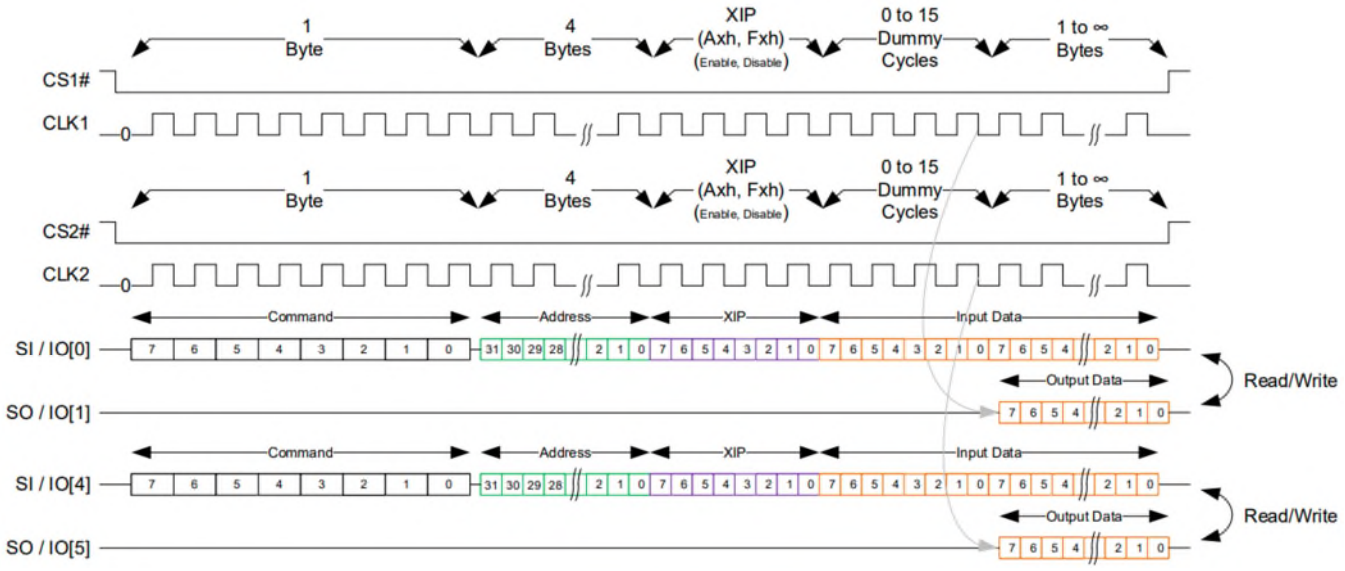


Figure 19: Description of (1-1-1) DDR Instruction Type (With XIP)

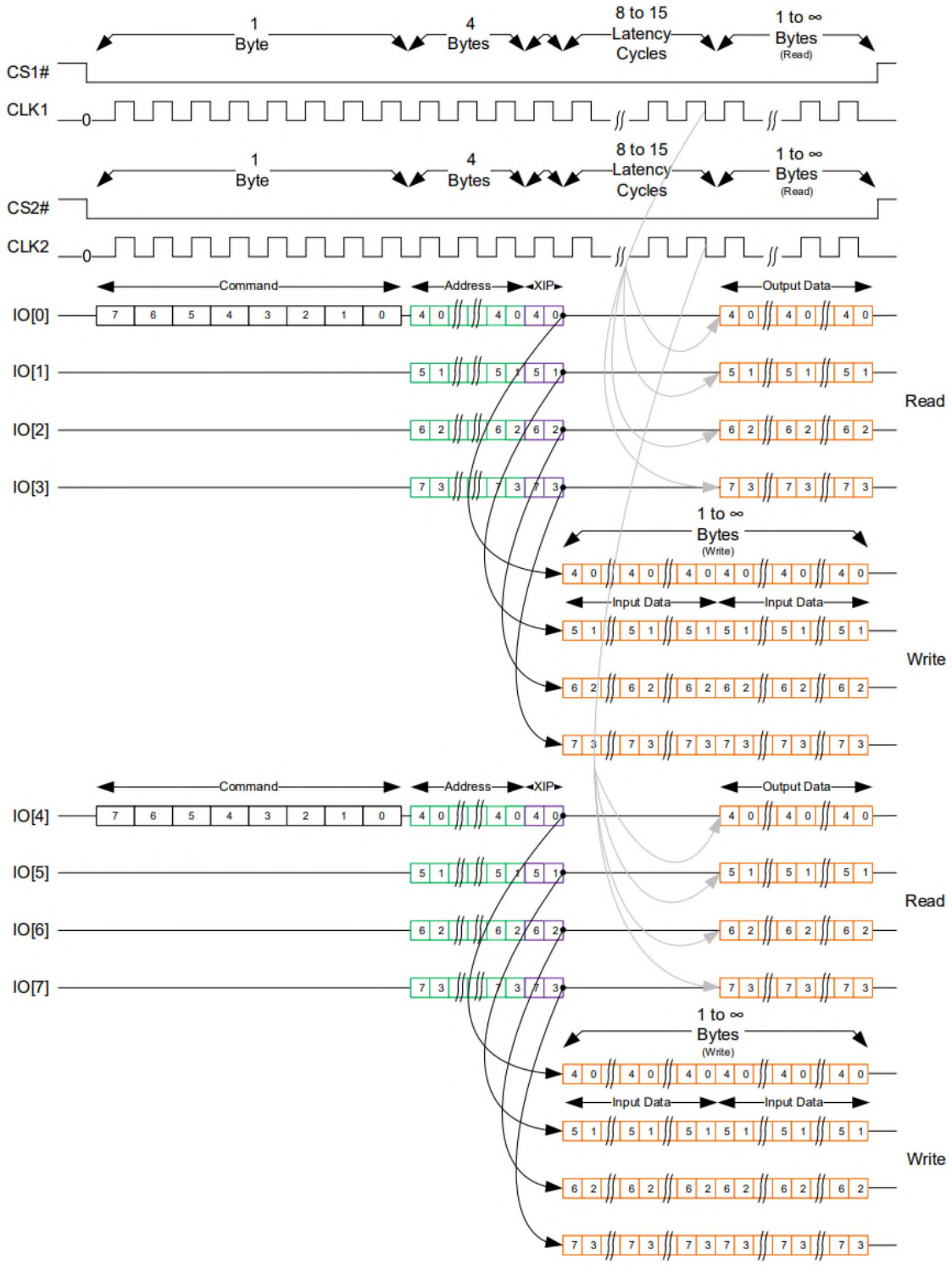


Figure 20: Description of (1-4-4) DDR Instruction Type (With XIP)

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only. Exposure to maximum rating for extended periods may adversely affect reliability.

Table 32: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Magnetic Field During Write	---	24000	A/m
Magnetic Field During Read	---	24000	A/m
Junction Temperature		150	°C
Storage Temperature	-55 to 150		°C
Supply Voltage VCC	-0.5	4.0	V
Supply Voltage VCCIO	-0.5	3.8	V
Voltage on any pin	-0.5	VCCIO + 0.2	V
ESD HBM (Human Body Model) ANSI/ESDA/JEDEC JS-001-2017	≥ |2000 V|		V
ESD CDM (Charged Device Model) ANSI/ESDA/JEDEC JS-002-2018	≥ |500 V|		V
Latch-Up (I-test) JESD78	≥ |100 mA|		mA
Latch-Up (Vsupply over-voltage test) JESD78	Passed		---

Electrical Specifications

Table 33: Recommended Operating Conditions

	Parameter / Condition	Minimum	Typical	Maximum	Units
Normal Operation	Operating Temperature:	-40.0	-	125.0	°C
	VCC Supply Voltage	2.5	3.0	3.6	V
	VCCIO Supply Voltage	1.71	1.8 – 3.0	3.6	V
Under Radiation	Operating Temperature:	-40.0	-	85.0	°C
	VCC Supply Voltage	2.5	2.7	3.0	V
	VCCIO Supply Voltage	1.71	1.8 – 3.0	3.6	V
VSS Supply Voltage		0.0	0.0	0.0	V
VSSIO Supply Voltage		0.0	0.0	0.0	V
VDD Supply Voltage		0.85	0.90	0.95	V

Table 34: Pin Capacitance

Parameter	Test Conditions	Symbol	Maximum	Units
Input Pin Capacitance	TEMP = 25°C; f = 1 MHz; VIN = 3.0V	CIN	5.0	pF
Output Pin Capacitance	TEMP = 25°C; f = 1 MHz; VIN = 3.0V	CINOUT	6.0	pF

Table 35: Endurance & Retention

Parameter	Symbol	Test Conditions	Minimum	Units
Write Endurance	END	-	10^{16}	cycles
Data Retention	RET	85°C	20	years

Table 36: Operational Environment

Parameter	Conditions	Limit	Units
Total Dose	VCC & VCCIO = Max; Temperature = Room (~25°C)	100	krads(Si)
SEL Onset LET	VCC = VCCIO = 3V; Temperature = 105°C VCC = VCCIO = 2.7V; Temperature = 105°C	>60 >75	MeV-cm^2/mg
SEU Onset LET	VCC = VCCIO = Min; Temperature = Room (~25°C)	>57	MeV-cm^2/mg
SEFI Onset LET	VCC = VCCIO = Min; Temperature = Room (~25°C)	>TBD	MeV-cm^2/mg

Table 37: Magnetic Immunity Characteristics

Parameter	Symbol	Maximum	Units
Magnetic Field During Write	Hmax_write	24000	A/m
Magnetic Field During Read	Hmax_read	24000	A/m

Table 38: DC Characteristics

Parameter	Symbol	Test Conditions	Density	3.0V Device (2.5V-3.6V)				
				Min	Typical [1]	85°C [2]	Max [3]	Units
Active Read Current	IREAD	VCC = 3.6V, CLK=100MHz	1Gb		90	180	300	mA
			2Gb		90	180	300	mA
			4GB		120	250	450	mA
			8Gb		200	400	750	mA
Active Write Current	IWRITE	VCC = 3.6V, CLK=100MHz	1Gb		90	180	300	mA
			2Gb		90	180	300	mA
			4GB		120	250	450	mA
			8Gb		180	400	750	mA
Standby Current	ISB1	VCC = 3.6V, CLK=VCCIO, CS#=VCCIO, SI=WP#=VCCIO	1Gb		70	135	260	mA
			2Gb		70	135	260	mA
			4GB		100	200	400	mA
			8Gb		200	350	700	mA
VDD Standby Current	ISB2	VDD = 0.9V VCCIO = 3.6	1-8Gb		2	3	5	mA
VDD Active Current	IVDD	VDD = 0.9V VCCIO = 3.6	1-8Gb		5	7	10	mA
Input Leakage Current	ILI	VIN=0 to VCCIO (max)					±1.0	µA
Output Leakage Current	ILO	VOUT=0 to VCCIO (max)					±1.0	µA
Input High Voltage (VCCIO=1.71-2.2)	VIH			0.65* VCCIO			VCCIO+0.2	V
Input High Voltage (VCCIO=2.2-2.7)				1.8				
Input High Voltage (VCCIO=2.7-3.6)				2.2				
Input Low Voltage (VCCIO=1.71-2.2)	VIL			-0.2			0.6	V
Input Low Voltage (VCCIO=2.2-2.7)							0.7	
Input Low Voltage (VCCIO=2.7-3.6)							0.8	
Output Low Voltage (VCCIO=1.71-2.2)	VOL	IOL = 2.0mA		-			0.4	V
Output Low Voltage (VCCIO=2.2-2.7)		IOL = 2.0mA					0.4	
Output Low Voltage (VCCIO=2.7-3.6)		IOL = 2.0mA					0.4	
Output High Voltage (VCCIO=1.71-2.2)	VOH	IOH = -0.1mA		1.4			-	V
Output High Voltage (VCCIO=2.2-2.7)		IOH = -0.1mA		1.7				
Output High Voltage (VCCIO=2.7-3.6)		IOH = -1.0mA		2.2				

Notes:

1. Typical values are measured at 25°C
2. 85°C (Junction Temperature) values are guaranteed by characterization; not tested in production
3. Max values are measured at 125°C (Case Temperature)

Table 39: AC Test Conditions

Parameter	Value
Input pulse levels	0.0V to VCCIO
Input rise and fall times	3.0ns
Input and output measurement timing levels	VCCIO/2
Output Load	CL = 30.0pF

CS# Operation & Timing

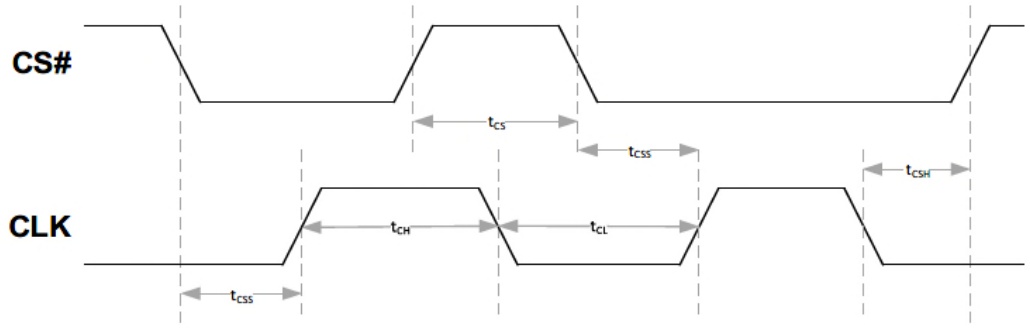


Figure 21: CS# Operation & Timing

Table 40: SDR CS# Operation

Parameter	Symbol	Minimum	Maximum	Units
Clock Frequency	fCLK	1	100 (SDR)	MHz
Clock Low Time	tCL	0.45 * 1/ fCLK	-	ns
Clock High Time	tCH	0.45 * 1/ fCLK	-	ns
Chip Deselect Time after Read Cycle	tCS1	20	-	ns
Chip Deselect Time after Write Cycle (SPI)	tCS3	600	-	ns
Chip Deselect Time after Write Cycle (QPI)	tCS5	600	-	ns
CS# Setup Time (w.r.t CLK)	tCSS	5	-	ns
CS# Hold Time (w.r.t CLK)	tCSH	4	-	ns

Notes:
Power supplies must be stable

Table 41: DDR CS# Operation

Parameter	Symbol	Minimum	Maximum	Units
Clock Frequency	fCLK	1.0	50 (DDR)	MHz
Clock Low Time	tCL	0.45 * 1/ fCLK	-	ns
Clock High Time	tCH	0.45 * 1/ fCLK	-	ns
CS# High Time (End of Read)	tCS1	20.0	-	ns
CS# High Time (End of Memory Array Write) SPI	tCS3	600.0	-	ns
CS# High Time (End of Memory Array Write) QPI	tCS5	600.0	-	ns
CS# Setup Time (w.r.t CLK)	tCSS	5.0	-	ns
CS# Hold Time (w.r.t CLK)	tCSH	4.0	-	ns

Notes:
Power supplies must be stable

Command, Address, XIP and Data Input Operation & Timing

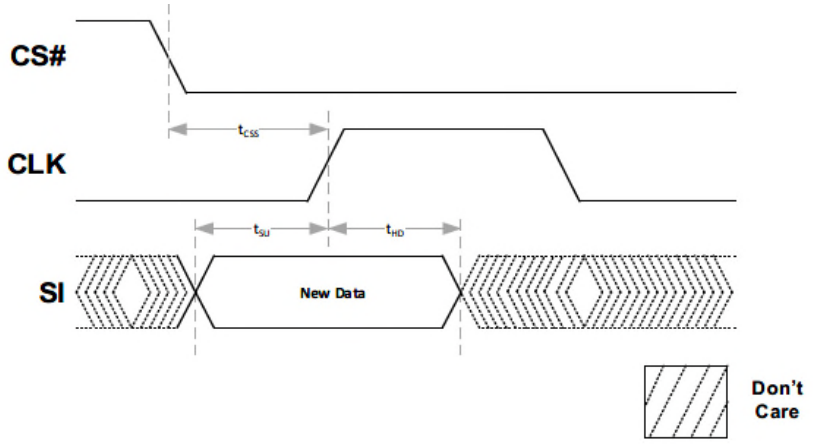


Figure 22: SDR Command, Address and Data Input Operation & Timing

Table 42: SDR Command, Address, XIP, and Data Input Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
Data Setup Time (w.r.t CLK)	tSU	2.0	-	ns
Data Hold Time (w.r.t CLK)	tHD	3.0	-	ns

Notes:
Power supplies must be stable

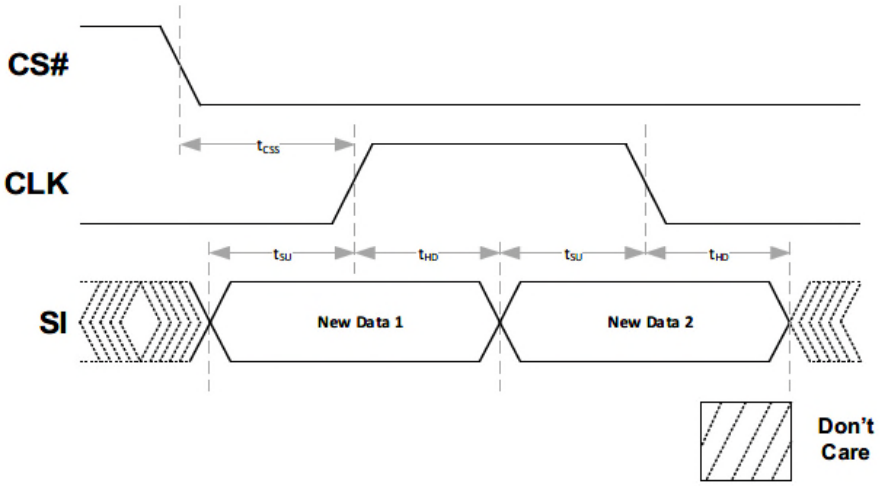


Figure 23: DDR Command, Address and Data Input Operation & Timing

Table 43: DDR Command, Address, XIP, and Data Input Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
Data Setup Time (w.r.t CLK)	tSU	4.0	-	ns
Data Hold Time (w.r.t CLK)	tHD	4.0	-	ns

Notes:
Power supplies must be stable

Data Output Operation & Timing

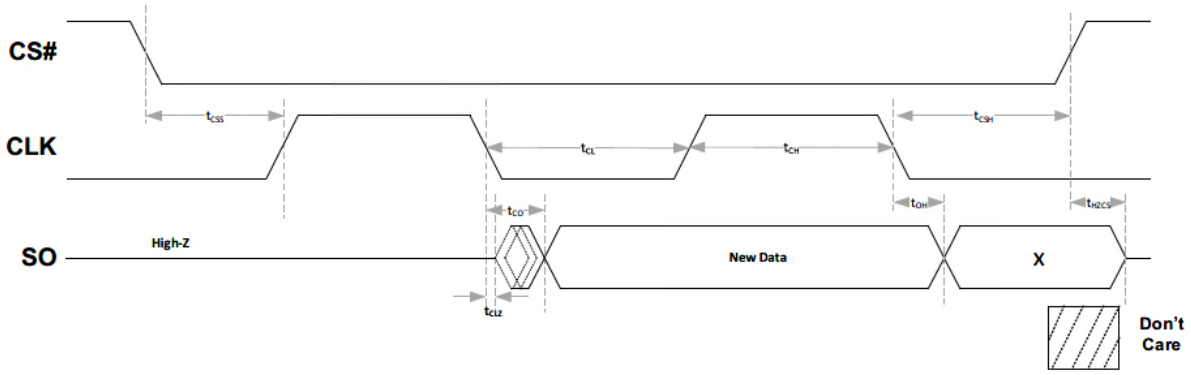


Figure 24: SDR Data Output Operation & Timing

Table 44: SDR Data Output Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
CLK Low to Output Low Z (Active)	tCLZ	0	-	ns
Output Valid (w.r.t CLK)	tCO	-	9.0	ns
Output Hold Time (w.r.t CLK)	tOH	1.0	-	ns
Output Disable Time (w.r.t CS#)	tHZCS	-	9.0	ns

Notes:

Power supplies must be stable

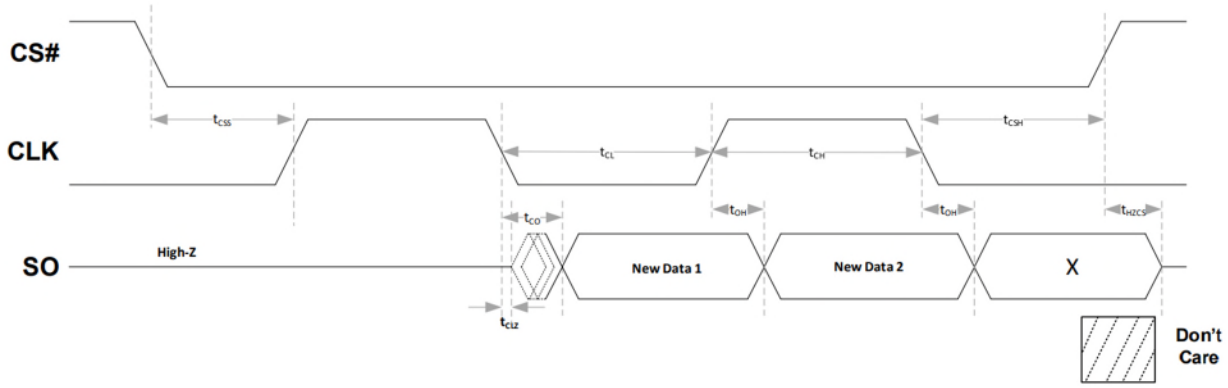


Figure 25: DDR Data Output Operation & Timing

Table 45: DDR Data Output Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
CLK Low to Output Low Z (Active)	tCLZ	0	-	ns
Output Valid (w.r.t CLK)	tCO	-	9.0	ns
Output Hold Time (w.r.t CLK)	tOH	1.0	-	ns
Output Disable Time (w.r.t CS#)	tHZCS	-	9.0	ns

Notes:

Power supplies must be stable

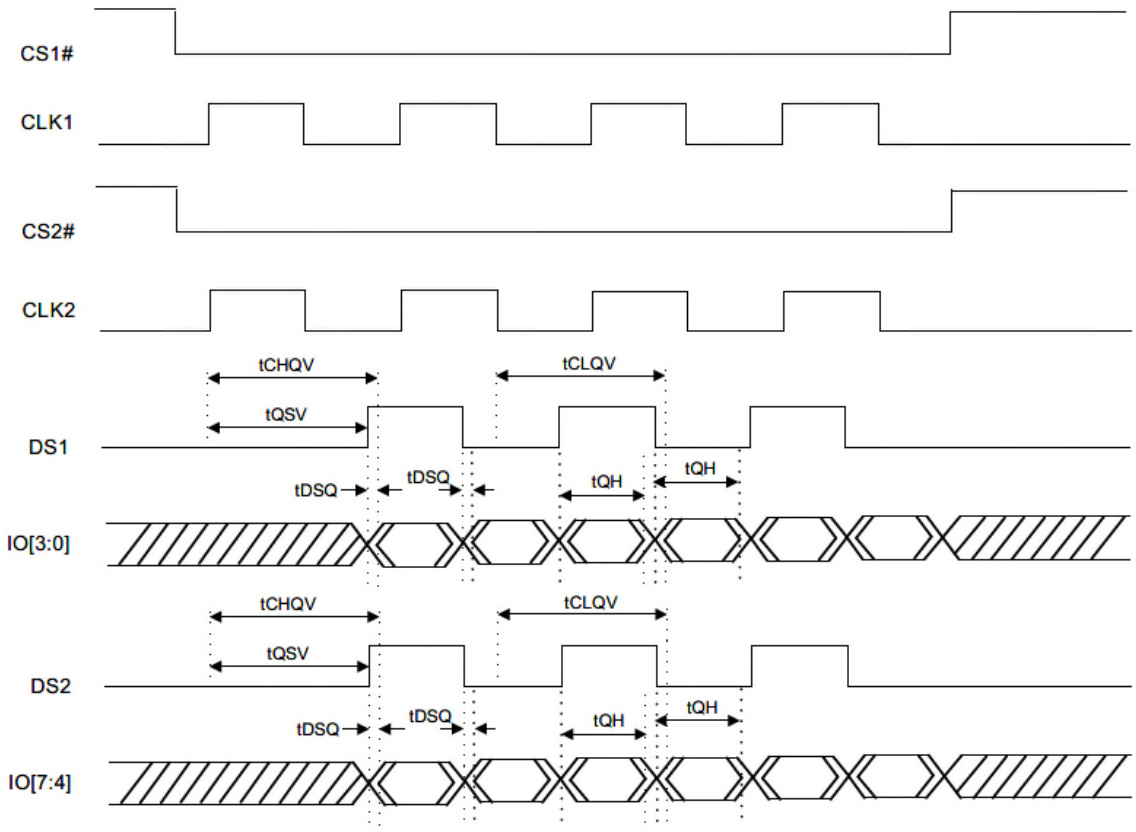


Figure 26: DDR Data Strobe (DS) Output Timing

Table 46: DDR Data Strobe (DS) OutputTiming

Parameter	Symbol	Minimum	Maximum	Units
Clock Transient to Output Valid (30pF Loading)	tCLQV/ tCHQV	-	5.0	ns
I/O Valid Skew Related to DS (30pF Loading)	tDSQ	-	1.0	ns
I/O Hold Time Related to DS	tQH	(tCL/ tCH) - tQHS	-	ns
I/O Hold Skew Factor (30pF Loading)	tQHS	-	1.0	ns
DS Clock Transient to DS Valid Time	tQSV	-	5.0	ns

Notes:
Power supplies must be stable

Table 47: WP# Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
WP# Setup Time (w.r.t CS#)	tWPSU	20	-	ns
WP# Hold Time (w.r.t CS#)	tWPHD	20	-	ns

Notes:
Power supplies must be stable

Thermal Resistance

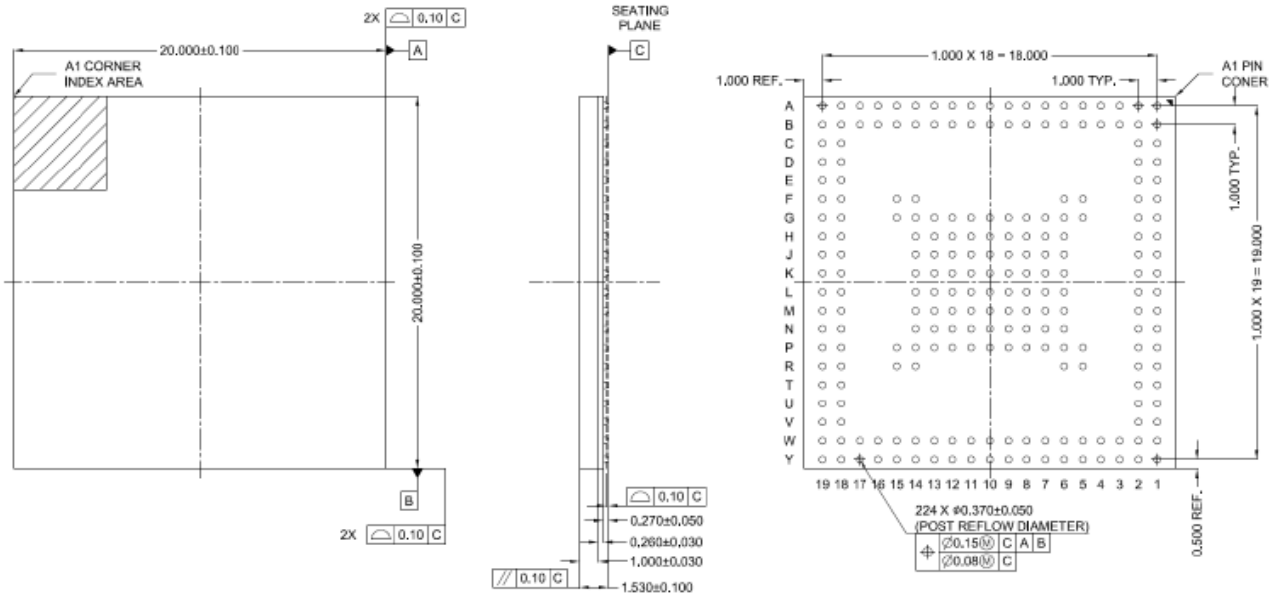
Table 49: Thermal Resistance Specifications

Parameter	Description	Units	224-Ball FBGA									
θ_{JC}	Thermal Resistance (junction to case)	°C/W	Top Die	2nd Die	3rd Die	4th Die	5th Die	6th Die	7th Die	Bottom Die	Controller	Reg
			2.03	2.05	2.00	1.88	1.67	1.38	1.00	0.54	1.25	10.9

Notes:
1. These parameters are guaranteed by characterization; not tested in production.
2. Case temperature, No Airflow, TC 85 °C
3. Worst case Junction temp specified for Top die (θJA) and Bottom die (θJC)

Package Drawings

224-Ball FBGA



TOP VIEW SIDE VIEW BOTTOM VIEW

NOTES

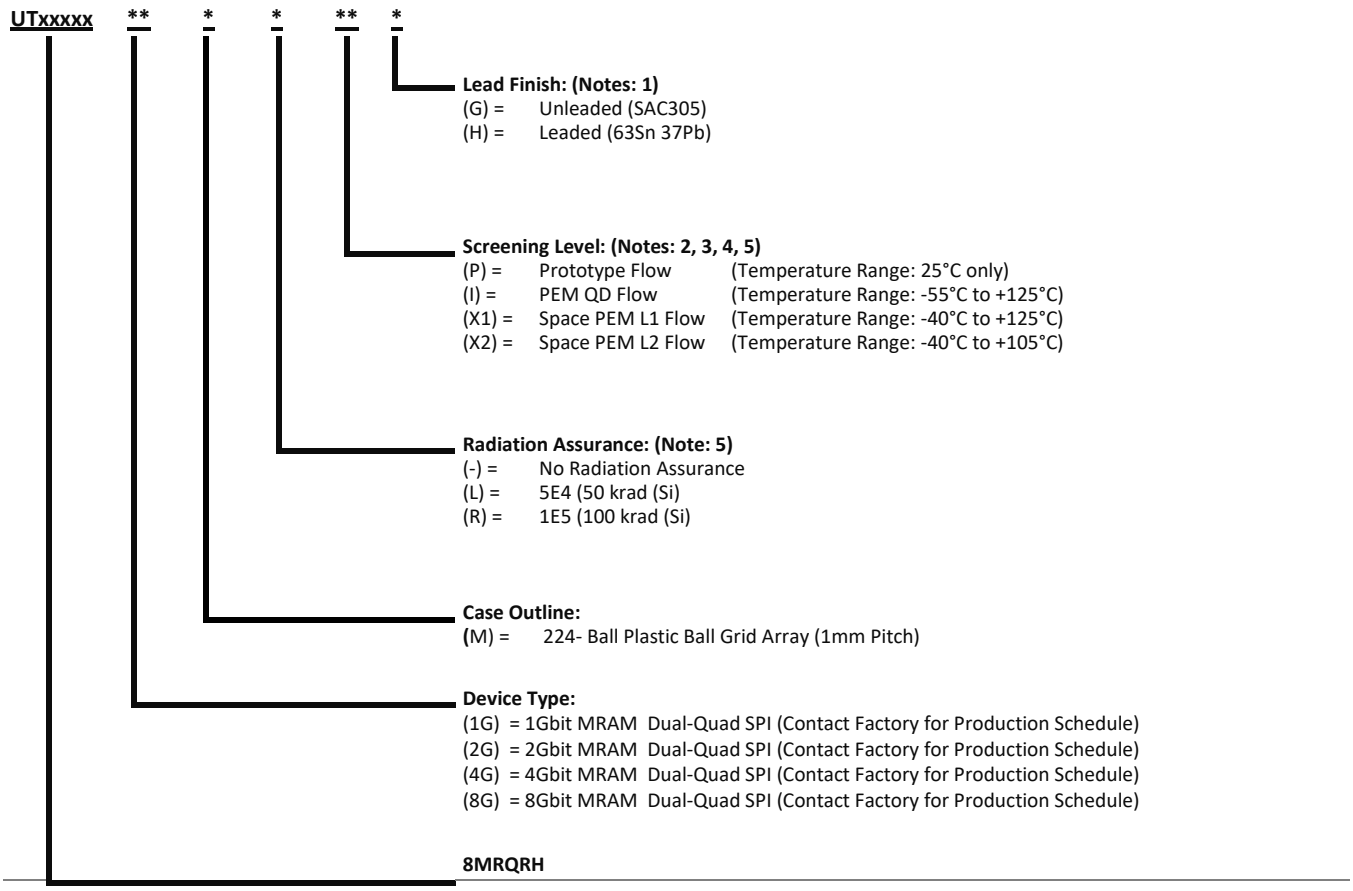
RAW SOLDER BALL SIZE IS 0.350

SRO SIZE IS 0.300

Figure 27: 224-ball FBGA

Ordering Information

Frontgrade Part Numbering Ordering Information



Notes:

1. Lead finish (G or H) must be specified.
2. Prototype Flow per Frontgrade Manufacturing Flows Document.
3. PEM QD Flow per Frontgrade Manufacturing Flows Document.
4. Space PEM L1 and L2 per Frontgrade Manufacturing Flows Document. Based on NASA PEM-INST-001 Level 1 and 2 criteria.
5. Radiation assurance levels may be selected for Space PEM L1 and L2 orders. For Prototype and PEM QD orders, No Radiation Assurance must be selected.

Revision History

Date	Revision #	Author	Change Description	Page #
01/17/2024	0.1.0	MJL	Initial RH version created from UT8MRQxG version 0.1.2	
5/2/2024	0.1.1	MJL	Initial RH version for Adv Rel	
6/7/2024	0.1.2	MJL	Revised per Manu pre released version G.2 5/1/2024. Power up/dn revised to include VDD. Table 20 updated from Unique to Device ID. Added read status flag register to instruction set.	various
8/7/2024	0.1.3	PBN	Revised per released version H.1 7/15/2024 VDD nominal and recommended operating range changed. Various DC electrical updates DDR and SDR frequency changed to 100 and 50 Mhz, respectively Removed JEDEC reset section	various

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.