FRONTGRADE

DATASHEET

UT54LVDS328

Octal 400 Mbps LVDS Repeater

9/1/2021

Version #: 2.2.2

Features

- 400.0 Mbps low jitter fully differential data path
- 200MHz clock channel
- 3.3V power supply
- 3.5mA LVDS TX output drivers
- Cold sparing all pins
- Fast propagation delay of 3.5ns max
- Receiver input threshold <100mV
- Operational environment; total dose irradiation testing to MIL- STD-883 Method 1019
- Total-dose: 1 Mrad(Si)
- SEL immune (LET ≤ 100 MeV-cm^2/mg)
- Packaging options:
  - 48-lead flatpack (1.4 grams)
  - Standard Microcircuit Drawing (SMD), 5962-20219
- QML Q and V
- Compatible with TIA/EIA-644

Operational Environment

- Temperature Range: -55°C to +125°C
- Total Dose: 1 Mrad(Si)
- SEL Immune: ≤ 100 MeV-cm^2/mg

Introduction

The UT54LVDS328 400 Mbps Octal Repeater utilizes Low Voltage Differential Signaling (LVDS) I/O logic standard for low power, high speed operation, and reduced EMI. Data paths are fully differential from input to output for low noise generation and low pulse width distortion. LVDS I/O enable high speed data transmission for point-to point interconnects. This device is designed for use as a high speed differential repeater.

The individual LVDS outputs can be put into Tri-State mode by use of the enable pins.

All pins have Cold Spare buffers. These buffers will be high impedance when V_{DD} is tied to V_{SS}.

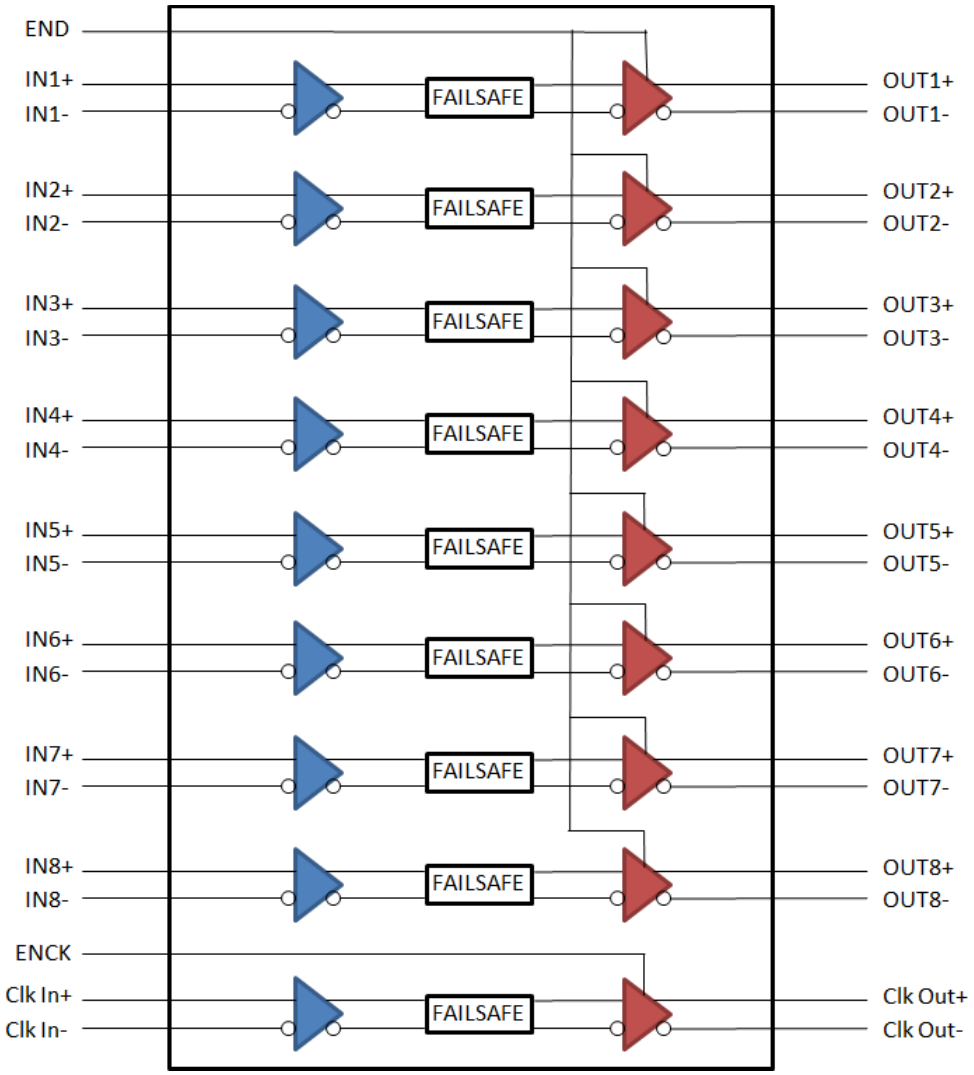


Figure 1. UT54LVDS328 Repeater Diagram

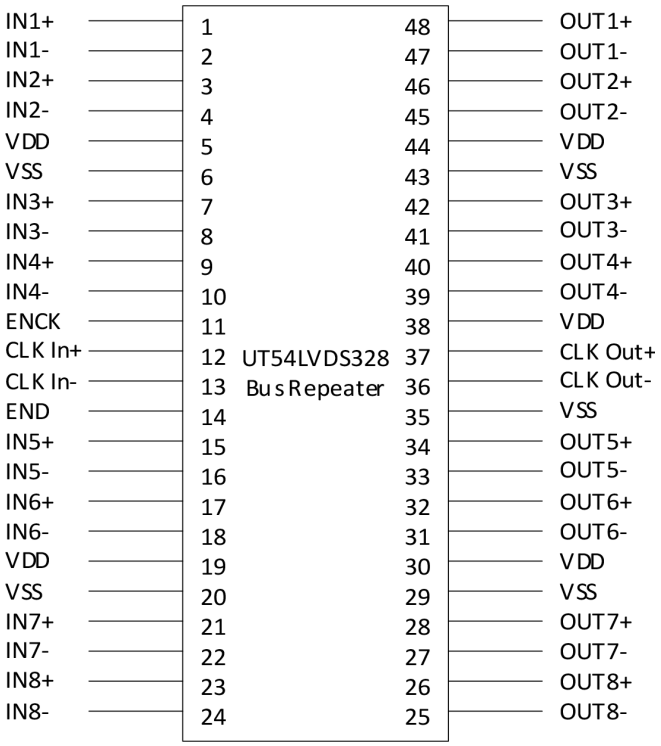


Figure 2. UT54LVDS328 Pinout

Pin Description

Name	# of Pins	Description
INn+	8	Non-inverting LVDS input
INn-	8	Inverting LVDS input
OUTn+	8	Non-inverting LVDS output
OUTn-	8	Inverting LVDS Output
END	1	A logic low on the enable puts the LVDS data output into Tri-State and reduces the supply current
ENCK	1	A logic low on the enable puts the LVDS clock output into Tri-State and reduces the supply current
V_{SS}	5	Ground
V_{DD}	5	Power supply
CLK IN+	1	Non-Inverting Clock LVDS Input
CLK IN-	1	Inverting clock LVDS Input
CLK OUT+	1	Non-Inverting Clock LVDS Output
CLK OUT-	1	Inverting Clock LVDS Output

Applications Information

The UT54LVDS328 provides the basic repeater function. The device operates as a 9 channel LVDS buffer. Repeating the signal restores the LVDS amplitude, allowing it to drive another media segment. This allows for isolation of segments or long distance applications.

The intended application of this device and LVDS signaling technique is for point-to-point baseband (single termination) data transmissions over controlled impedance media. The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics.)

Input Fail-Safe

The UT54LVDS328 also supports OPEN, shorted and terminated input fail-safe. Receiver output will be HIGH for all fail-safe conditions.

PCB layout and Power System Bypass

Circuit board layout and stack-up for the UT54LVDS328 should be designed to provide noise-free power to the device. Good layout practice also will separate high frequency or high level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power/ground sandwiches. This increases the intrinsic capacitance of the PCB power system which improves power supply filtering, especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range 0.01µF to 0.1µF. Tantalum capacitors may be in the range of 2.2µF to 10µF. Voltage rating for tantalum capacitors should be at least 5X the power supply voltage being used. It is recommended practice to use two vias at each power pin of the UT54LVDS328, as well as all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance and extends the effective frequency range of the bypass components.

The outer layers of the PCB may be flooded with additional ground plane. These planes will improve shielding and isolation, as well as increase the intrinsic capacitance of the power supply plane system. Naturally, to be effective, these planes must be tied to the ground supply plane at frequent intervals with vias. Frequent via placement also improves signal integrity in signal transmission lines by providing short paths for image currents which reduces signal distortion. The planes should be pulled back from all transmission lines and component mounting pads a distance equal to the width of the widest transmission line from the internal power or ground plane(s) whichever is greater. Doing so minimizes effects on transmission line impedances and reduces unwanted parasitic capacitances at component mounting pads.

Operational Environment

Symbol	Parameter	Limit	Units
TID	Total Ionizing Dose[1,2]	1.0E6	rad(Si)
SEL	Single Event Latchup[3]	≤100	MeV-cm^2/mg
Neutron Fluence	Neutron Fluence[4]	1.0E13	n/cm^2

Notes:

1. For devices procured with a total ionizing dose tolerance guarantee, post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to maximum TID level procured.
2. Per MIL-STD-883, method 1019.9, condition A.
3. SEL characterization is performed at V_{DD}=3.6 V at 125°C.
4. Guaranteed by design but not tested.

Absolute Maximum Ratings[1]

(Referenced to V_{SS})

Symbol	Parameter	Min	Max	Units
V_{DD}	DC supply voltage	-0.3	4.0	V
$V_{I/O}$	Voltage on any pin	-0.3	V_{DD} + 0.3	V
$I_{I/O}$	DC current on any I/O pin	-10	10	mA
ESD_{HBM}	HBM ESD Rating	1200		V
ESD_{CDM}	CDM ESD Rating	500		V
T_{STG}	Storage temperature	-65	150	°C
P_D	Maximum power dissipation permitted @ Tc=+125°C		1.667	W
T_J	Maximum junction temperature[2]		+150	°C
θ_{JC}	Thermal resistance, junction-to-case[3]		15	°C/W
I_I	DC input current		±10	mA

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Per MIL-STD-883, Method 1012.1, Section 3.4.1, PD=(T_J(max) - T_C(max) /Θ_{JC}
3. Test per MIL-STD-883, Method 1012.
4. For cold spare mode (V_{DD}=V_{SS}), $V_{I/O}$ may be -0.3V to the maximum recommended operating V_{DD} + 0.3V.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{DD}	Positive Supply voltage	3.0	3.6	V
T_{OP}	Temperature Range	-55	125	°C
T_C	Case temperature range	-55	125	°C
V_{IN}	DC input voltage, receiver inputs	0	2.4	V
	DC input voltage, logic inputs[1]	0	V_{DD}	V

Notes:

1. For END and ENCK signals only

DC Electrical Characteristics*[1]

(V_{DD}=3.3V ± 0.3V; -55°C < T_C < +125°C); Unless otherwise noted, T_C is per the temperature range ordered.

Symbol	Parameter	Condition	MIN	MAX	Unit
CMOS/TTL DC Specifications (EN)					
V_{IH}	High-level input voltage		2.0	V_{DD}	V
V_{IL}	Low-level input voltage		GND	0.8	V
I_{IH}	High-level input current	V_{IN}=3.6V; V_{DD}=3.6V	-10	+10	µA
I_{IL}	Low-level input current	V_{IN}=0V; V_{DD}=3.6V	-10	+10	µA
V_{CL}	Input clamp voltage	I_{CL}=-18mA		-1.5	V
I_{OS}	Cold Spare Leakage current	V_{IN}=3.6V; V_{DD}=V_{SS}	-20	+20	µA
LVDS Output DC Specifications (OUT+, OUT-)					
V_{OD}	Differential Output Voltage	R_L= 100Ω (see Figure 9)	250	450	mV
ΔV_{OD}	Change in V_{OD} between complimentary output states	R_L= 100Ω (see Figure 9)		35	mV
V_{OS}	Offset Voltage		1.055	1.550	V
ΔV_{OS}	Change in V_{OS} between complimentary output states	R_L= 100Ω V_{OS}= $\left(\frac{V_{OH}+V_{IN}}{2}\right)$		35	mV
I_{OZ}	Output Tri-State Current	Tri-State output, V_{DD} =3.6V V_{OUT}=V_{DD} or GND		±10	µA
I_{CSOUT}	Cold Sparing Leakage Current	V_{OUT}=3.6V, V_{DD}=V_{SS}	-20	+20	µA
I_{OS}2,3	Output Short Circuit Current	V_{OUT}+ OR V_{OUT}-=0 V		-25	mA
LVDS RECE DC Specifications (IN+, IN-)					
V_{TH}[3]	Differential Input High Threshold	V_{CM}=+1.2V		+100	mV
V_{TL}[3]	Differential Input Low Threshold	V_{CM}=+1.2V	-100		mV
V_{CMR}	Common Mode Voltage Range	V_{ID}=210mV	0.2	2.00	V
I_{IN}	Input Current	V_{IN}=+2.4V, V_{DD}=3.6V	-10	+10	µA
		V_{IN}=0V, V_{DD}=3.6V	-10	+10	µA
I_{CSIN}	Cold Spare Leakage Current	V_{IN}=3.6V, V_{DD}=V_{SS}	-20	+20	µA
Supply Current					
I_{CCL}	Total Supply Current	R_L=100Ω END, ENCK= V_{DD}, V_{DD}= 3.6V		90	mA
ICCZ	Tri-State Supply Current	END, ENCK=V_{SS}, V_{DD}= 3.6V		20	mA

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground.
2. Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time do not exceed maximum junction temperature specification.
3. Guaranteed by characterization.

AC Switching Characteristics*

(V_{DD} =+3.3V ± 0.3V; T_A=-55 °C to +125 °C); Unless otherwise noted, T_C is per the temperature range ordered.

Symbol	Parameter	Conditions	MIN	MAX	Unit
t_{PHZ}(1)	Disable Time (Active to Tri-State) High to Z (Figure 7)	R_L=100Ω, C_L=10pf		4.5	ns
t_{PLZ}(1)	Disable Time (Active to Tri-State) Low to Z (Figure 7)	R_L=100Ω, C_L=10pf		4.5	ns
t_{PZH}(1)	Enable Time (Tri-State to Active) Z to High (Figure 57)	R_L=100Ω, C_L=10pf		11.0	ns
t_{PZL}(1)	Enable Time (Tri-State to Active) Z to Low (Figure 7)	R_L=100Ω, C_L=10pf		11.0	ns
t_{LHT}(1)	Output Low-to-High Transition Time, 20% to 80% (Figure 4 and 5)	R_L=100Ω, C_L=10pf		1.3	ns
t_{HLT}(1)	Output High-to-Low Transition Time, 80% to 20% (Figure 4 and 5)	R_L=100Ω, C_L=10pf		1.3	ns
t_{PLHD}	Propagation Low to High Delay (Figure 4 and 6)	R_L=100Ω, C_L=10pf		3.5	ns
T_{PHLD}	Propagation High to Low Delay (Figure 4 and 6)	R_L=100Ω, C_L=10pf		3.5	ns
T_{SKEW}	Differential Skew T_{PHLD} - T_{PLHD} (Figure 4 and 6)			900	ps
T_{CCS}	Output Channel-to-Channel Skew (Figure 4 and 6)			500	ps

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Guaranteed by design.

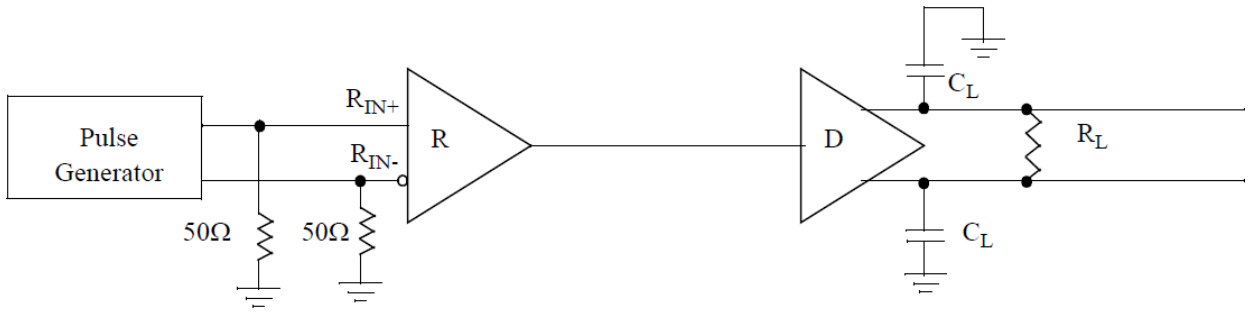


Figure 4. LVDS Output Load

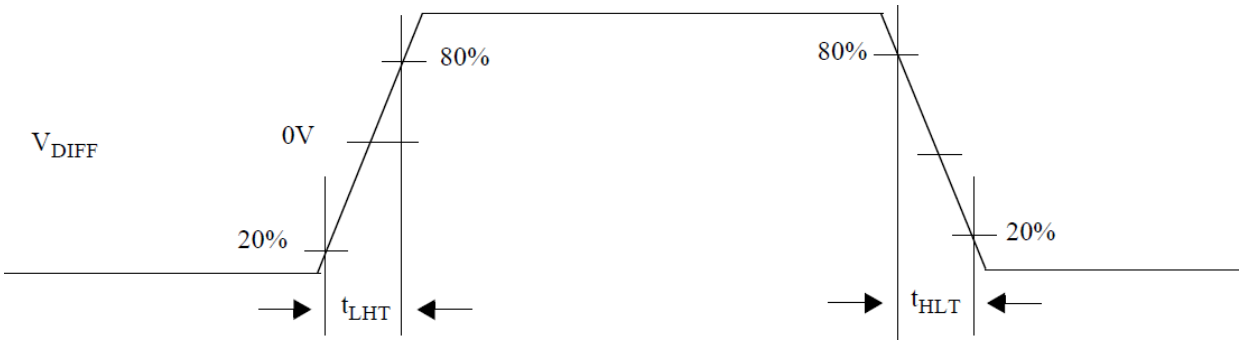


Figure 5. LVDS Output Transition Time

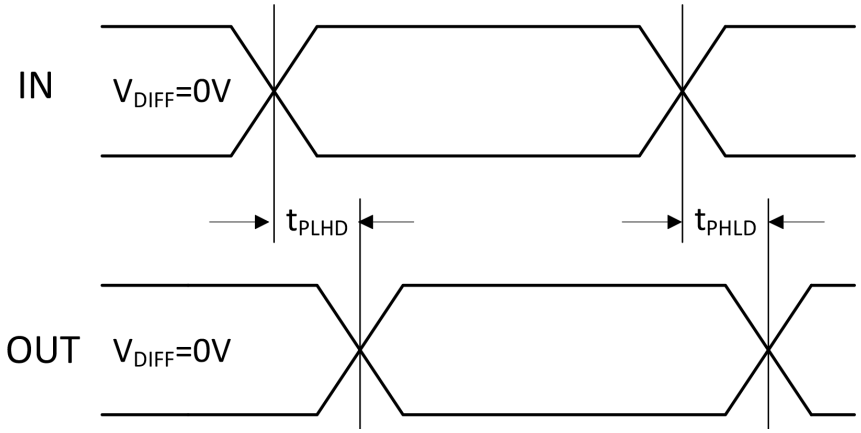


Figure 6. Propagation Delay Low-to-High and High-to-Low

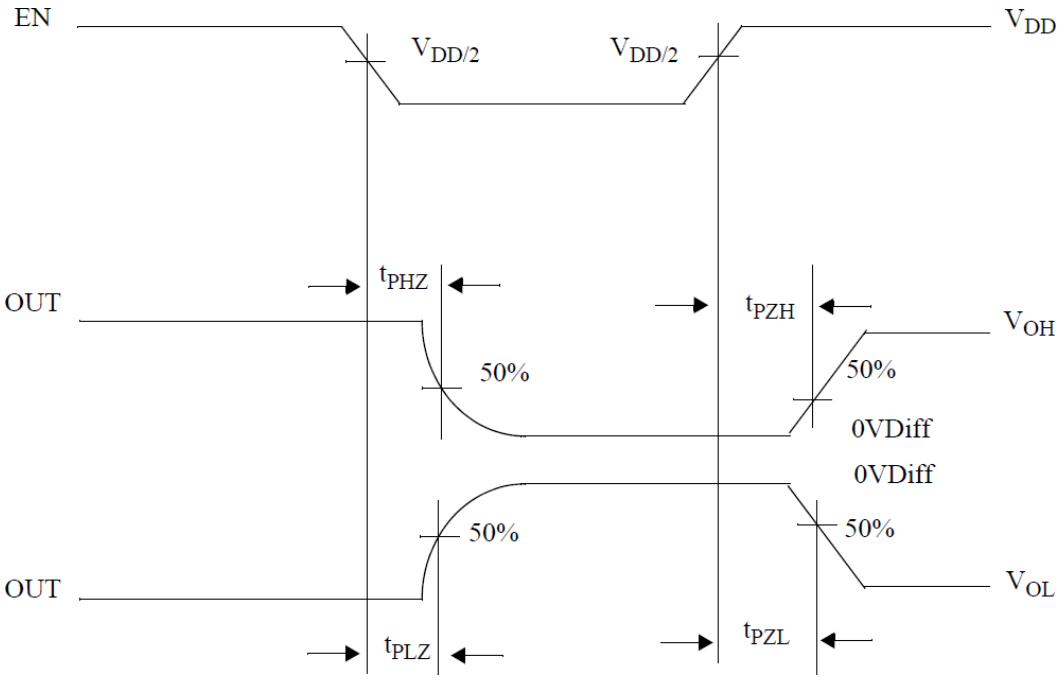


Figure 7. Output active to TRI-STATE and TRI-STATE to active

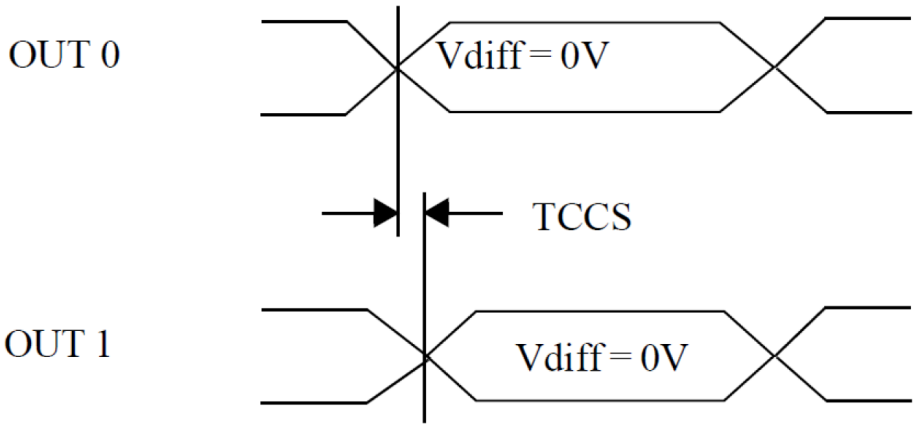


Figure 8. Output Channel-to-Channel Skew

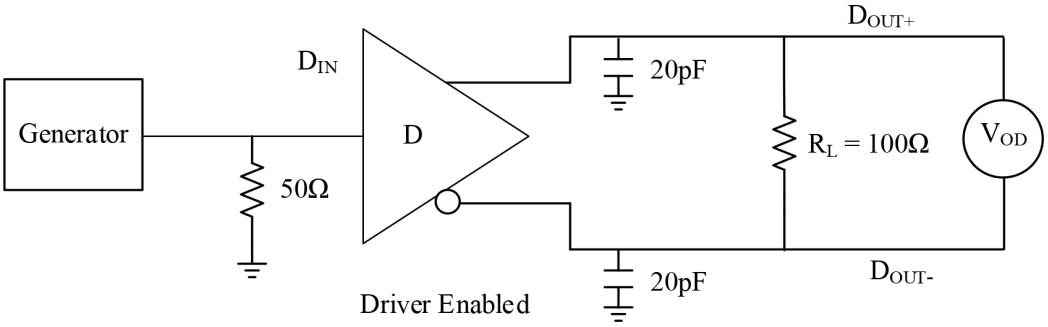


Figure 9. Driver V_{OD} and V_{OS} Test Circuit or Equivalent Circuit

Packaging

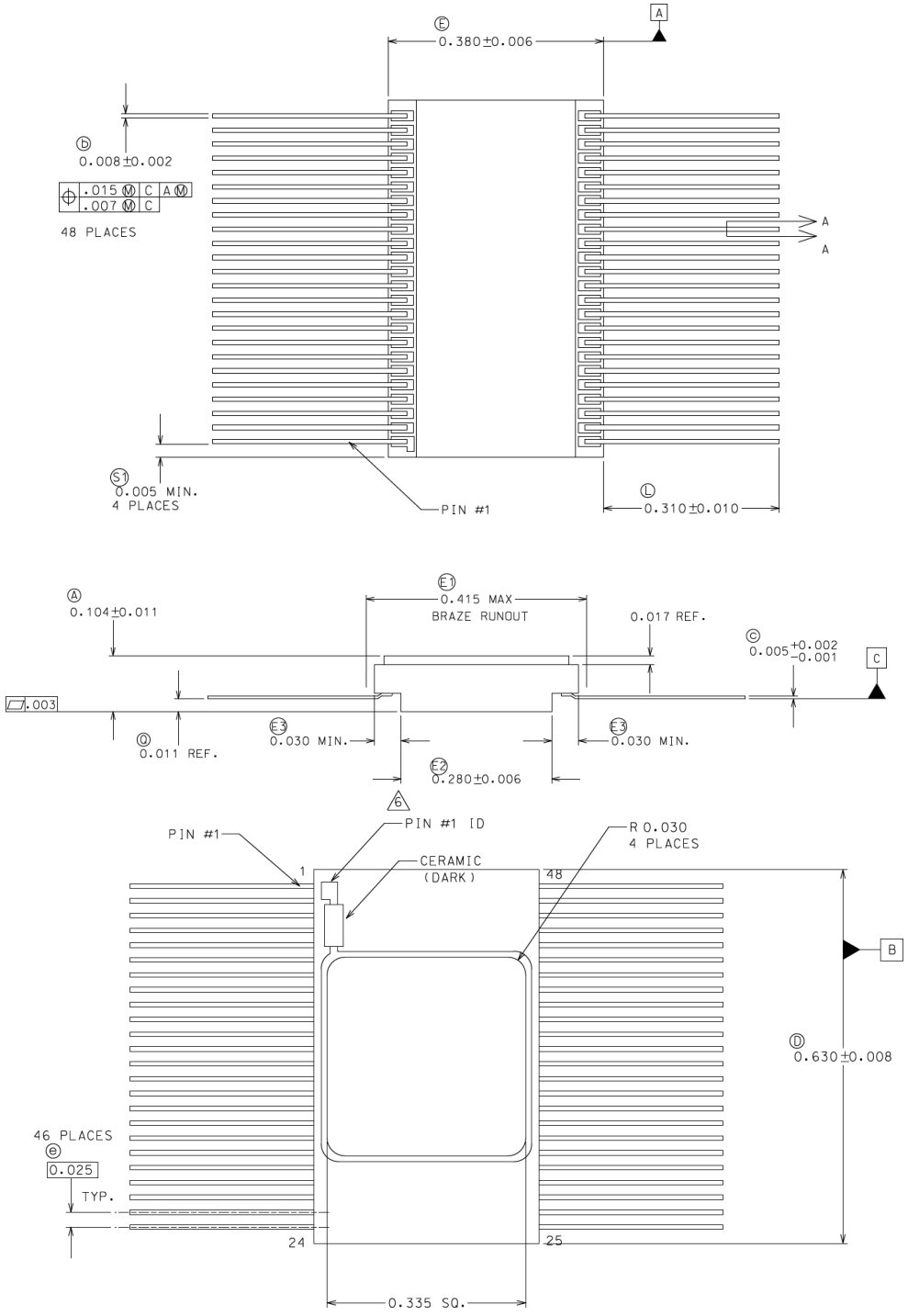


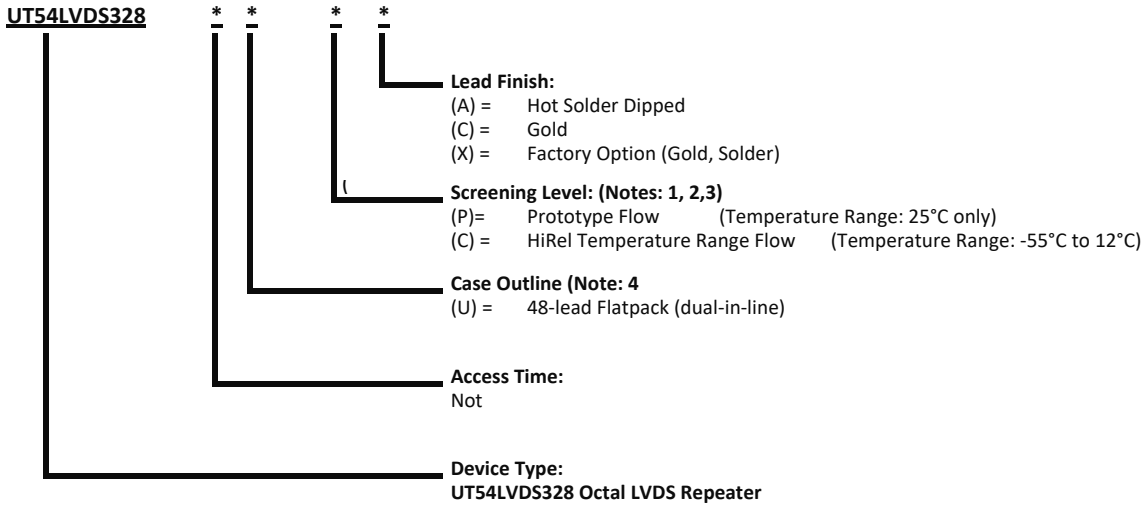
Figure 10. 48-pin Flatpack

Notes:

1. All exposed metallized areas are gold plated over electrically nickel per MIL-PRF-38535.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Dimension symbology is in accordance with MIL-PRF-38535.
5. Lead position and coplanarity are not measured.D
6. ID mark symbol is vendor option: no alphanumerics.

Ordering Information:

Frontgrade Part Numbering Ordering Information

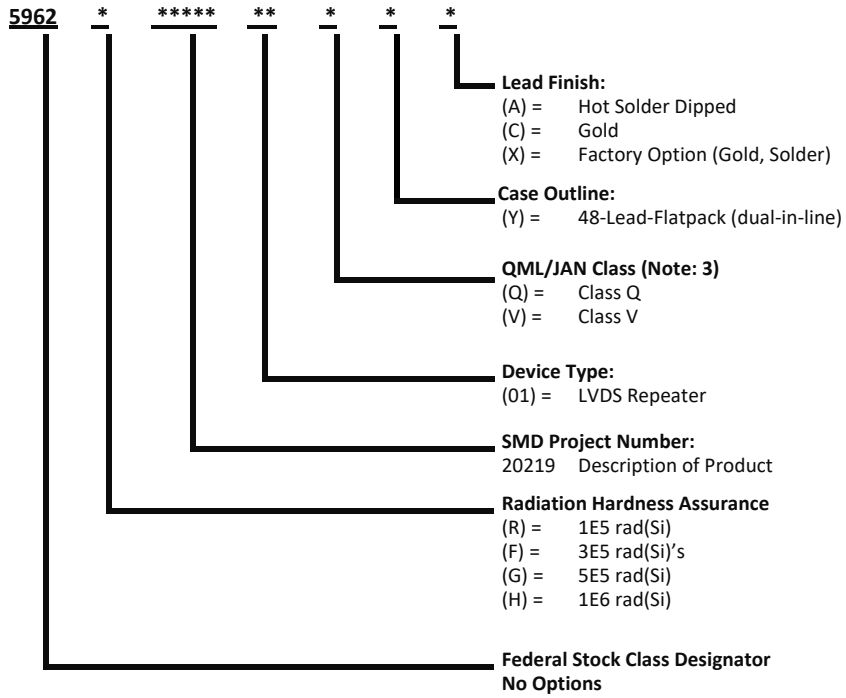


Notes:

1. Lead finish (A, C, or X) must be specified.
2. If and "X" is specified when ordering, then the part marking will match the lead finish and will be either “A” (solder) or “C” (gold).
3. Prototype Flow per Frontgrade Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY Radiation neither tested nor guaranteed.
4. HiRel Temperature Range Flow per Frontgrade Manufacturing Flows Document. Devices are tested at -55°C room temp, and 125°C. Radiation neither tested nor guaranteed.

Ordering Information

SMD Part Number Ordering Information



Notes:

1. Lead finish (A, C, or X) must be specified.
2. If "X" is specified when ordering, the factory will determine lead finish. Part marking will reflect the lead finish applied to the device shipped.
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.

Revision History

Date	Revision #	Author	Change Description	Page #
01/31/2020	0.1.0	BM	Initial Advanced Data Sheet	
04/14/2020	0.1.1	BM	Electrical parameter updates from Design Engineering	
05/14/2020	0.1.2	BM	Formatting and product description updates	
06/15/2020	0.1.3	BM	Corrections to Radiation Effects: FEATURES + Operational Environment, p.1	p. 1
07/31/2020	0.1.4	BM	Correction to Section 4, p. 4, Operational Environment: Neutron Fluence	P. 4
10/26/2020	1.0.1	BM	Table 5, p. 5, V_{OS} range update. Changed from Advanced to Preliminary	p. 5
11/24/2020	1.0.2	BM	Updated DS, FEATURES, p.1: TID=1Mrad(Si) only.	p. 1
01/05/2021	2.0.0	BM	Updated from “Preliminary Data Sheet” to [Released] “Data Sheet”	
03/08/2021	2.1.0	BM/JM	Corrected clerical errors	
06/28/2021	2.2.0	BM	Corrected all R_L=35Ω to R_L=100Ω, p. 6, 7, 9	p. 6, 7, 9
07/29/2021	2.2.1	BM	AMR Table, p.5: Added ESD ratings, edited AMR Table Notes	p. 5
09/08/2021	2.2.2	BM	ROC Table, p.5: Corrected V_{DD} operating voltage range	p. 5

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.