FRONTGRADE

DATASHEET

UT54LVDM228

Quad 2x2 400 Mbps Cross Point Switch

9/22/2021

Version #: 1.0.3

Features

- 400.0 Mbps low jitter fully differential data path
- 200MHz clock channel
- 3.3 V power supply
- 10mA LVDS output drivers
- Input receiver fail-safe
- Cold sparing all pins
- Configurable as quad 2:1 mux, 1:2 demux, repeater or1:2 signal splitter
- Fast propagation delay of 3.5ns max
- Receiver input threshold < ± 100 mV
  — Operational environment; total dose irradiation testing to MIL-STD-883 Method 1019
  — Total-dose: 300 krad(Si) and 1 Mrad(Si)
- Latchup immune (LET ≤100 MeV-cm^2/mg)
- Packaging options:
  — 64-lead flatpack (1.8 grams)
- Standard Microcircuit Drawing 5962-01537
  — QML Q and V compliant part
- Compatible with TIA/EIA-899

Introduction

The UT54LVDM228 is a quad 2x2 crosspoint switch utilizing Low Voltage Differential Signaling (LVDS) technology for low power, high speed operation. Data paths are fully differential from input to output for low noise generation and low pulse width distortion. The non-blocking design allows connection of any input to any output or outputs on each switch. LVDS I/O enable high speed data transmission for point-to point or multi-drop interconnects. This device can be used as a high speed differential crosspoint, 2:1 mux, 1:2 demux, repeater or 1:2 signal splitter.
The mux and demux functions are useful for switching between primary and backup circuits in fault tolerant systems. The 1:2 signal splitter and 2:1 mux functions are useful for distribution of a bus across several rack-mounted backplanes.

The individual LVDS outputs can be put into Tri-State by use of the enable pins.

All pins have Cold Spare buffers. These buffers will be high impedance when V_{DD} is tied to V_{SS}.

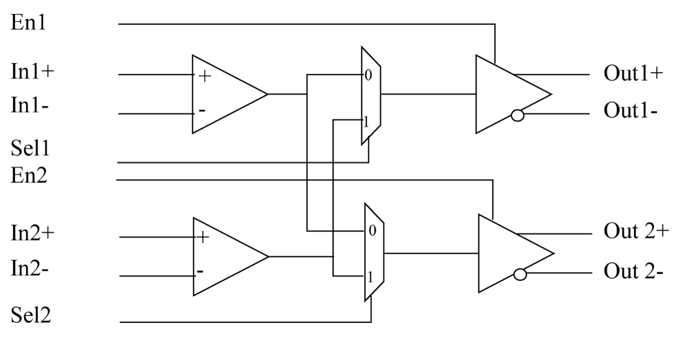

Figure 1a. UT54LVDM228 Crosspoint Switch Block Diagram (Partial - see Page 2 for complete diagram)

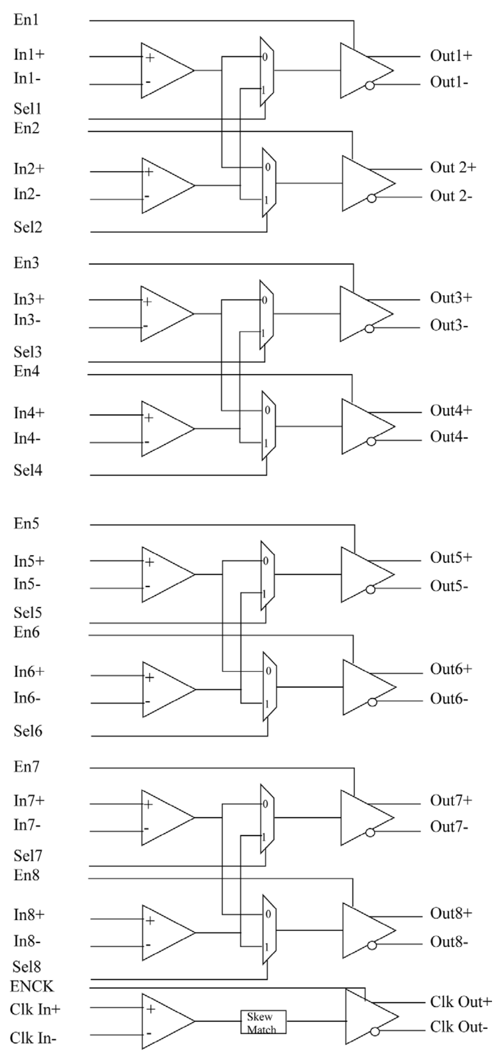

Figure 1b. UT54LVDM228 Crosspoint Switch Block Diagram

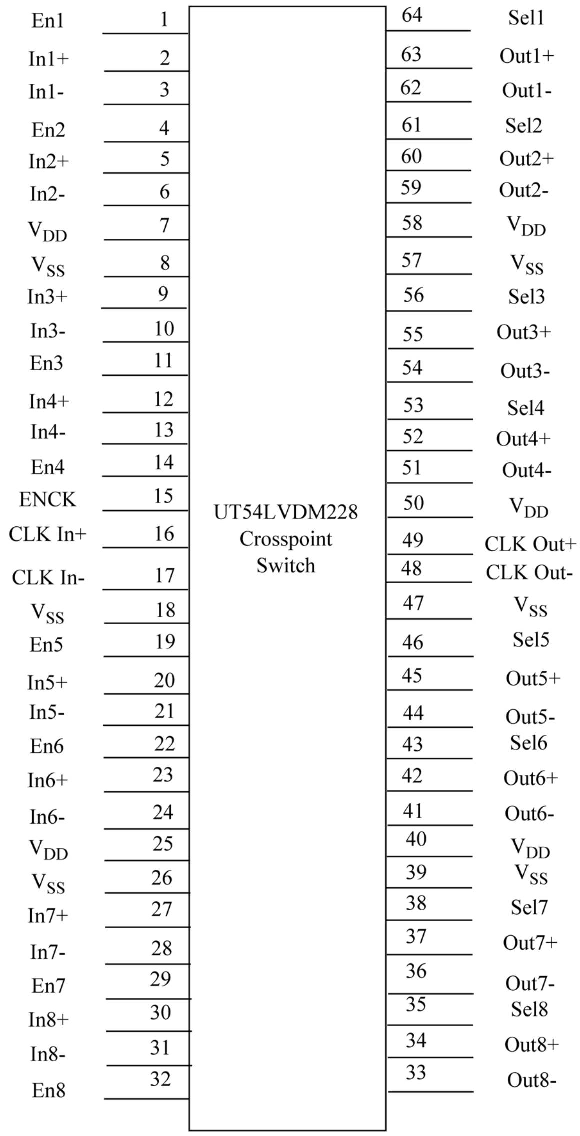

Figure 2. UT54LVDS228 Pinout

Truth Table

Sel1	Sel2	Out1	Out2	Mode
0	0	In1	In1	1:2 splitter
0	1	In1	In2	Repeater
1	0	In2	In1	Switch
1	1	In2	In2	1:2 splitter

Pin Description

Name	# of Pins	Description
In+	8	Non-inverting LVDS input
In-	8	Inverting LVDS input
Out+	8	Non-inverting LVDS output
Out-	8	Inverting LVDS Output
En	8	A logic low on the enable puts the LVDS output into Tri-State and reduces the supply current
ENCK	1	A logic low on the enable puts the LVDS output into Tri-State and reduces the supply current
Sel	8	2:1 mux input select
V_{SS}	6	Ground
V_{DD}	5	Power supply
CLK In+	1	Non-Inverting Clock LVDS Input
CLK In-	1	Inverting clock LVDS Input
CLK Out+	1	Non-Inverting Clock LVDS Output
CLK Out-	1	Inverting Clock LVDS Output

Applications Information

The UT54LVDM228 provides three modes of operation. In the 1:2 splitter mode, the two outputs are copies of the same single input. This is useful for distribution / fan-out applications. In the repeater mode, the device operates as a 9channel LVDS buffer. Repeating the signal restores the LVDS amplitude, allowing it to drive another media segment. This allows for isolation of segments or long distance applications or buffers standard LVDS to 10mA multi- op drivers. The switch mode provides a crosspoint function. This can be used in a system when primary and redundant paths are supported in a fault tolerant application.

The intended application of these devices and signaling technique is for both point-to-point baseband (single termination) and multipoint (double termination) data transmissions over controlled impedance media. The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics.

Input Fail-Safe:

The UT54LVDM228 also supports OPEN, shorted and terminated input fail-safe. Receiver output will be HIGH for all fail-safe conditions.

PCB layout and Power System Bypass:

Circuit board layout and stack-up for the UT54LVDM228 should be designed to provide noise-free power to the device. Good layout practice also will separate high frequency or high level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power/ground sandwiches. This increases the intrinsic capacitance of the PCB power system which improves power supply filtering, especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range 0.01µF to 0.1µF. Tantalum capacitors may be in the range of 2.2µF to 10µF. Voltage rating for tantalum capacitors should be at least 5X the power supply voltage being used. It is recommended practice to use two vias at each power pin of the UT54LVDM228, as well as all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance and extends the effective frequency range of the bypass components.

The outer layers of the PCB may be flooded with additional ground plane. These planes will improve shielding and isolation, as well as increase the intrinsic capacitance of the power supply plane system. Naturally, to be effective, these planes must be tied to the ground supply plane at frequent intervals with vias. Frequent via placement also improves signal integrity in signal transmission lines by providing short paths for image currents which reduces signal distortion. The planes should be pulled back from all transmission lines and component mounting pads a distance equal to the width of the widest transmission line from the internal power or ground plane(s) whichever is greater. Doing so minimizes effects on transmission line impedances and reduces unwanted parasitic capacitances at component mounting pads.

Compatibility with LVDS standard:

In backplane multidrop configurations, with closely spaced loads, the effective differential impedance of the line is reduced. If the mainline has been designed for 50Ω differential impedance, the loading effects may reduce this to the 35Ω range depending upon spacing and capacitance load. Terminating the line with a 35Ω load is a better match than with 50Ω and reflections are reduced.

Operational Environment

Parameter	Limit	Units
Total Ionizing Dose (TID)	1.0E6	rad(Si)
Single Event Latchup (SEL)	≤100	MeV-cm^2/mg
Neutron Fluence 1	1.0E13	n/cm^2

Notes:

1. Guaranteed but not tested.

Absolute Maximum Ratings 1

(Referenced to V_{SS})

Symbol	Parameter	Limits
V_{DD}	DC supply voltage	-0.3 to 4.0V
$VI_{/O}$[4]	Voltage on any pin	-0.3 to (V_{DD} + 0.3V)
ESD_{HBM}	HBM ESD Rating	1250V
T_{STG}	Storage temperature	-65 to +150℃
P_D	Maximum power dissipation permitted @ T_C = +125℃	1.667 W
T_J	Maximum junction temperature[2]	+150℃
Θ_{JC}	Thermal resistance, junction-to-case[3]	15℃/W
I_I	DC input current	±10mA

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to +175℃ during burn-in and life test.
3. Test per MIL-STD-883, Method 1012.
4. For Cold Spare mode (V_{DD}=V_{SS}), VI/O may be -0.3V to the maximum recommended operating V_{DD} + 0.3V.
5. Per MIL-STD-883, Method 1012.1, Section 3.4.1, P_D=(T_J(max) – T_C (max) / Θ_{JC}

Recommended Operating Conditions

Symbol	Parameter	Limits
V_{DD}	Positive supply voltage	3.0 to 3.6V
T_C	Case temperature range	-55 to +125℃
V_{IN}	DC input voltage, receiver inputs	0 to 2.4V
	DC input voltage, logic inputs	0 to V_{DD} for EN, SEL

DC Electrical Characteristics*[1]

(V_{DD} = 3.3V ± 0.3V; -55℃ < T_C < +125℃); Unless otherwise noted, T_C is per the temperature noted.

Symbol	Parameter	Condition	MIN	MAX	Unit
CMOS/TTL DC Specifications (EN, SEL)					
V_{IH}	High-level input voltage		2.0	VCC	V
V_{IL}	Low-level input voltage		GND	0.8	V
I_{IH}	High-level input current	V_{IN}=3.6V; V_{DD}=3.6V	-10	+10	µA
I_{IL}	Low-level input current	V_{IN}=0V; V_{DD}=3.6V	-10	+10	µA
V_{CL}	Input clamp voltage	I_{CL}=-18mA		-1.5	V
I_{CS}	Cold Spare Leakage	V_{IN}=3.6V, V_{DD}=V_{SS}	-20	+20	µA
LVDS Output DC Specifications (OUT+, OUT-)					
V_{OD}	Differential Output Voltage	R_L= 35Ω (see Figure 10)	250	450	mV
ΔV_{OD}	Change in VOD between complimentary output states	R_L= 35Ω		35	mV
V_{OS}	Offset Voltage	R_L= 35Ω VOS$\left(\frac{V_{OH} + V_{IN}}{2}\right)$ (see Figure 10)	1.055	1.550	V
ΔV_{OS}	Change in VOS between complimentary output states	R_L=35Ω		35	mV
I_{OZ}	Output Tri-State Current	Tri-State output, V_{DD} = 3.6V V_{OUT}=V_{DD} or GND		±10	µA
I_{CSOU}T	Cold Sparing Leakage Current	V_{OUT}=3.6V, V_{DD}=V_{SS}	-20	+20	µA
I_{OS}[2,3]	Output Short Circuit Current	V_{OUT}+ OR V_{OUT}- = 0 V		-25	mA
V_{TH}[3]	Differential Input High Threshold	V_{CM}= +1.2V		+100	mV
V_{TL}[3]	Differential Input Low Threshold	V_{CM}== +1.2V	-100		mV
V_{CMR}	Common Mode Voltage Range	V_{ID}=200mV	0.2	2.00	V
I_{IN}	Input Current	V_{IN}= +2.4V, V_{DD} = 3.6V	-10	+10	µA
		V_{IN}= 0V, V_{DD} = 3.6V	-10	+10	µA
I_{CSIN}	Cold Spare Leakage Current	V_{IN}=3.6V, V_{DD}=V_{SS}	-20	+20	µA
I_{CCD}	Total Supply Current	R_L = 35Ω EN1 - EN8, ENCK = V_{DD}		220	mA
I_{CCZ}	Tri-State Supply Current	EN1 - EN8, ENCK = V_{SS}		20	mA

Notes:

1. *For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25℃ per MIL- STD-883 Method 1019, Condition A up to the maximum TID level procured.
2. Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground.
3. Output short circuit current (IOS) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.
4. Guaranteed by characterization.

AC Switching Characteristics*

(V_{DD} =+3.3V ± 0.3V, TA = -55 ℃ to +125 ℃); Unless otherwise noted, Tc is per the temperature noted.

Symbol	Parameter	Conditions	MIN	MAX	Unit
t_{SET}[1,2]	Input to SEL Setup Time (Figure 3 and 4)	R_L=35Ω, C_L =10pF	1.6		ns
R_L=35Ω	R_L=35Ω	R_L=35Ω	R_L=35Ω	R_L=35Ω	R_L=35Ω
t_{SWITCH}[1]	SEL to Switched Output (Figure 3 and 4)	R_L=35Ω, C_L =10pF		3.0	ns
t_{PHZ}[1]	Disable Time (Active to Tri-State) High to Z (Figure 5 and 8)	R_L=35Ω, C_L =10pF		4.5	ns
t_{PLZ}[1]	Disable Time (Active to Tri-State) Low to Z (Figure 5 and 8)	R_L=35Ω, C_L =10pF		4.5	ns
t_{PHZ}[1,4]	Enable Time (Tri-State to Active) Z to High (Figure 5 and 8)	R_L=35Ω, C_L =10pF EN on other channels = GND		11.0	ns
t_{PLZ}[1,4]	Enable Time (Tri-State to Active) Z to Low (Figure 5 and 8)	R_L=35Ω, C_L =10pF EN on other channels = GND		11.0	ns
t_{LHT}[3]	Output Low-to-High Transition Time, 20% to 80% (Figure 5 and 6)	R_L=35Ω, C_L =10pF		600	ps
t_{HLT}[3]	Output High-to-Low Transition Time, 80% to 20% (Figure 5 and 6)	R_L=35Ω, C_L =10pF		600	ps
t_{PLHD}	Propagation Low to High Delay (Figure 5 and 7)	R_L=35Ω, C_L =10pF		3.5	ns
T_{PHLD}	Propagation High to Low Delay (Figure 5 and 7)	R_L=35Ω, C_L=10pF		3.5	ns
T_{SKEW}	Pulse Skew TPHLD - TPLHD (Figure 5 and 7)			900	ps
T_{CCS}	Output Channel-to-Channel Skew (Figure 5 and 9)			500	ps

Notes:

1. *For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25℃ per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
2. Guaranteed by characterization.
3. T_{SET} and T_{HOLD} time specify that data must be in a stable state before and after SEL transition.
4. Guaranteed by design.
5. Max t_{PZH} and t_{PZL} = 4.5ns when EN or ENCL = V_{DD} on another channel.

AC Timing Diagrams

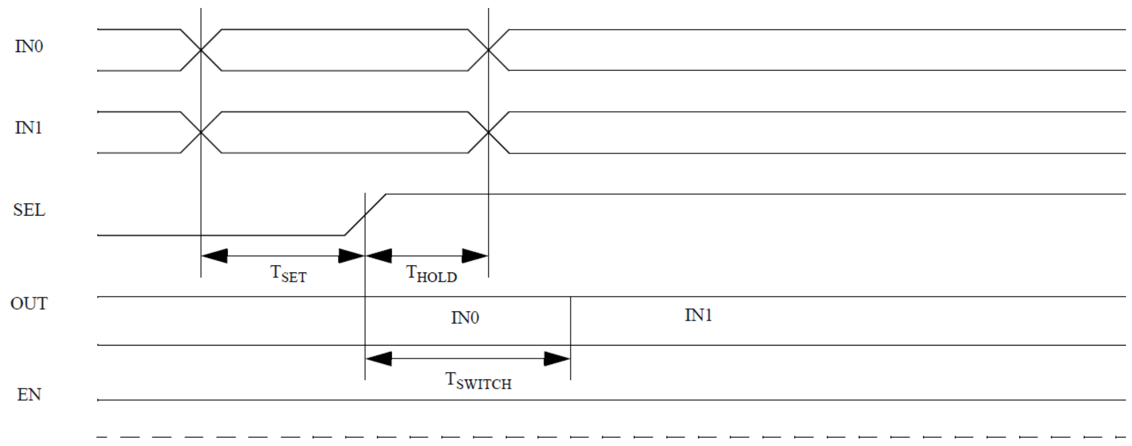

Figure 3. Input-to-Select Rising Edge Setup and Hold Times and MUX Switch Time

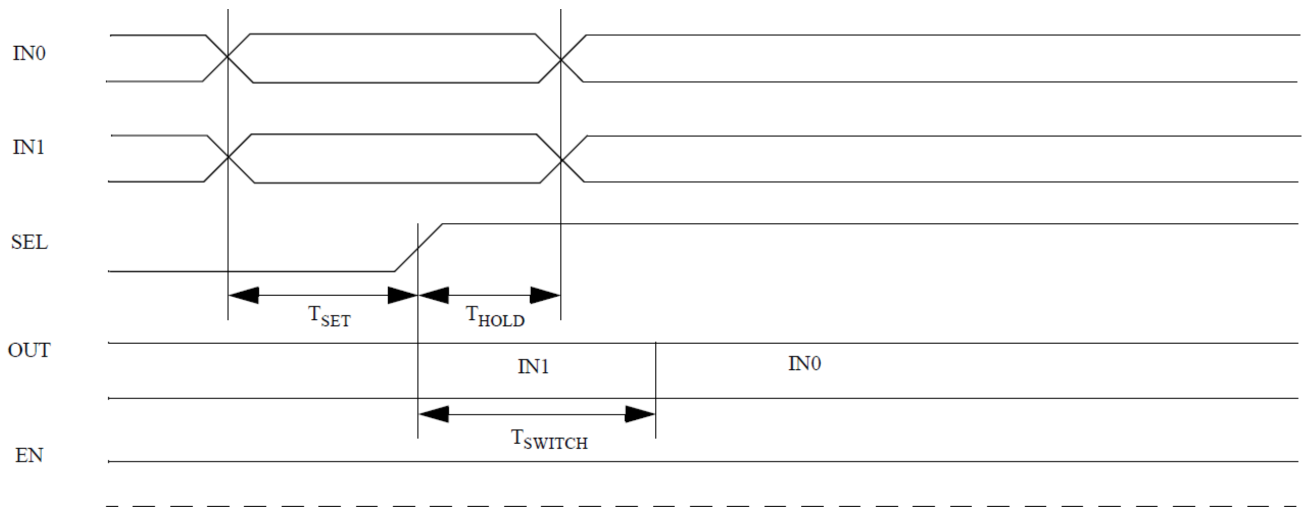

Figure 4. Input-to-Select Falling Edge Setup and Hold Times and MUX Switch Time

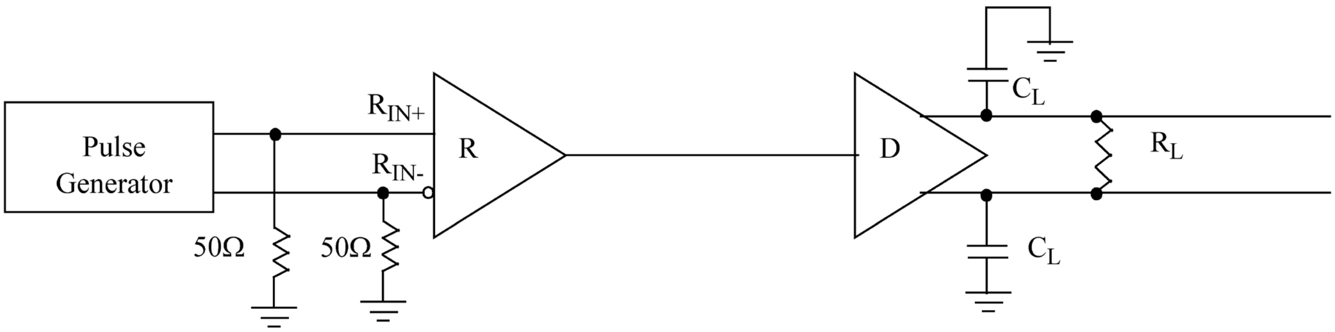

Figure 5. LVDS Output Load

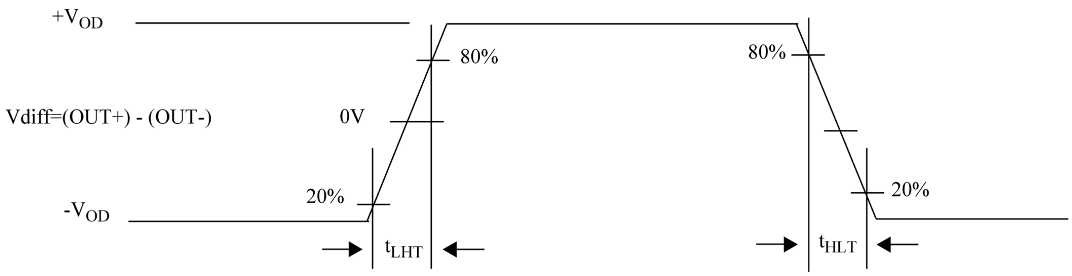

Figure 6. LVDS Output Transition Time

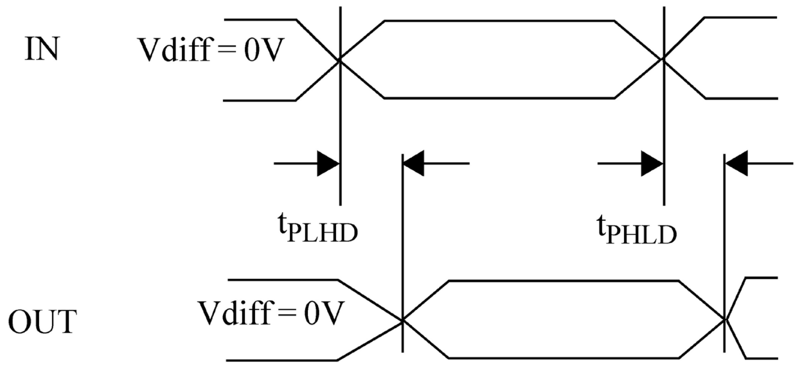

Figure 7. Propagation Delay Low-to-High and High-to-Low

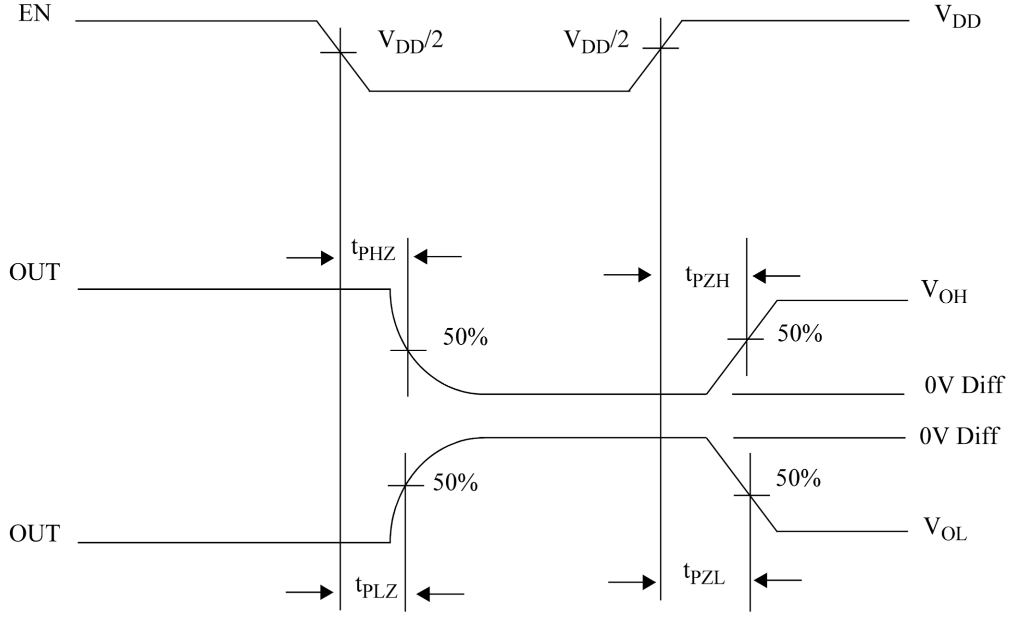

Figure 8. Output active to TRI-STATE and TRI-STATE to active

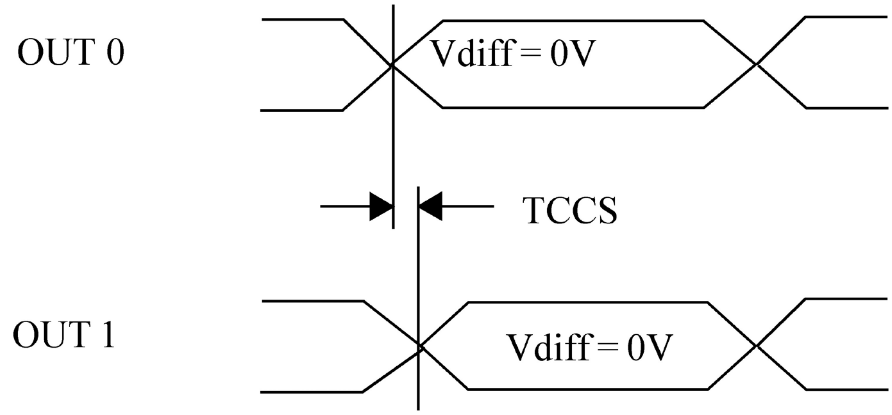

Figure 9. Output Channel-to-Channel Skew in 1:2 splitter mode

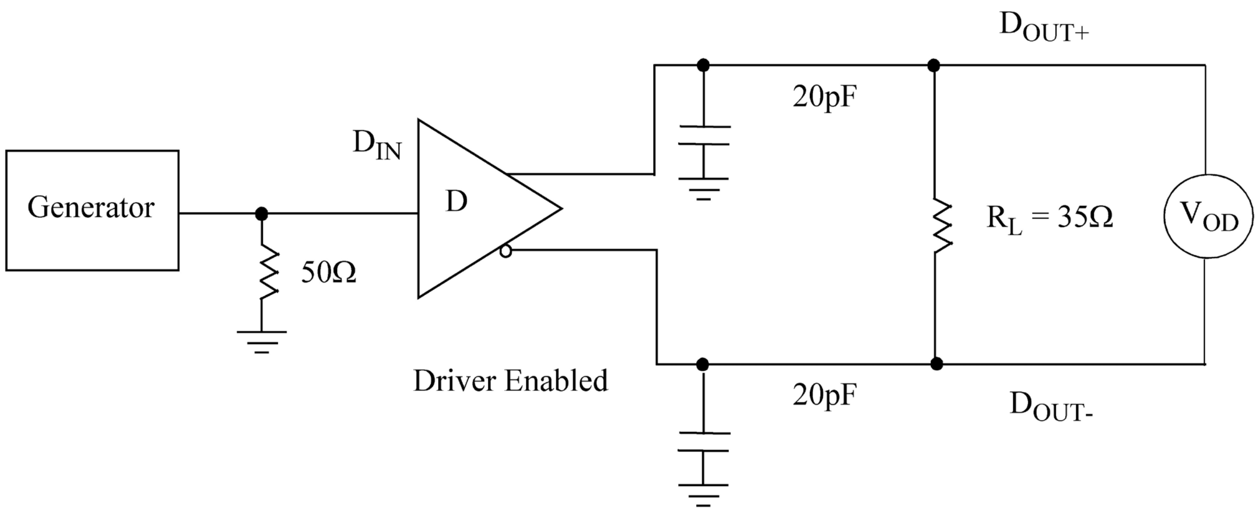

Figure 10. Driver VOD and VOS Test Circuit or Equivalent Circuit

Packaging

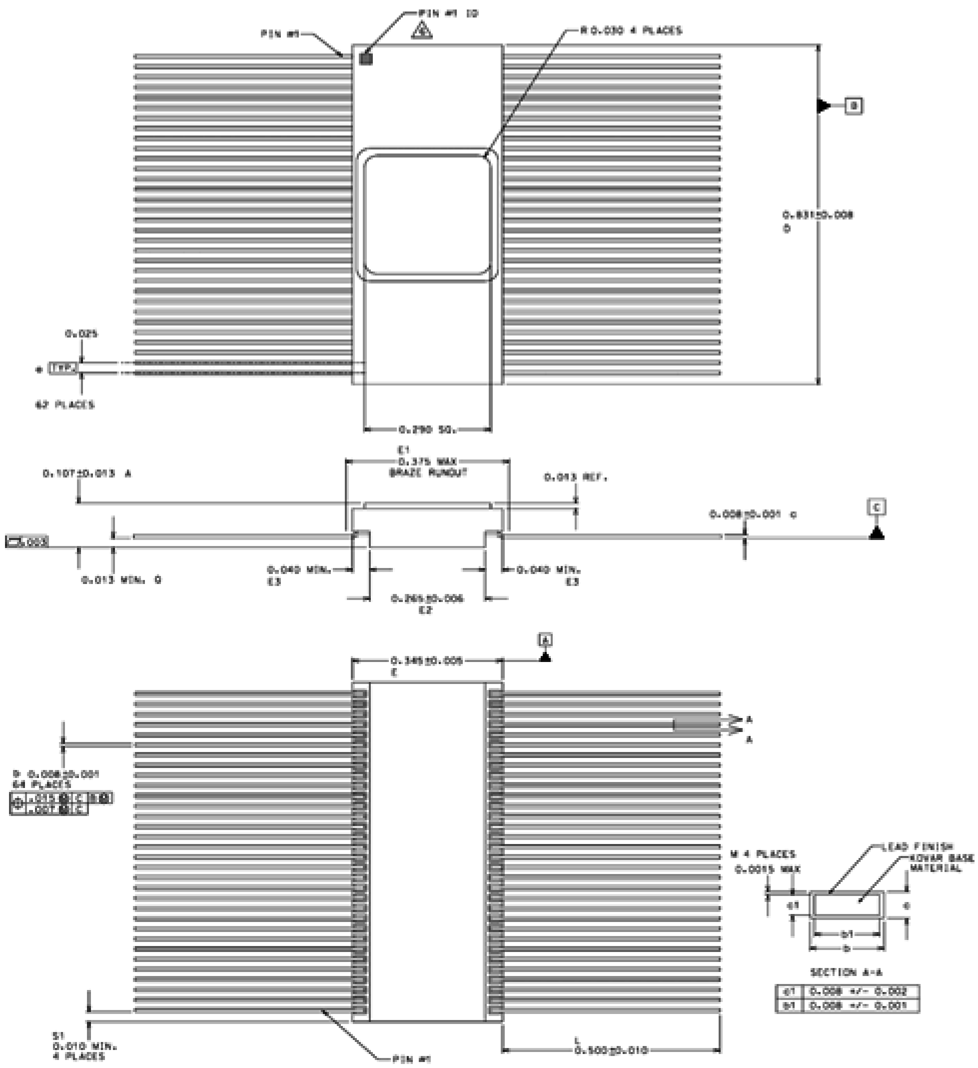

Figure 11. 64-pin Flatpack

Notes:

1. All exposed metalized areas must be gold plated over electrically plated nickel per MIL-PRF-38535.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Dimension symbology is in accordance with MIL-PRF-38535.
5. Lead position and colanarity are not measured.
6. ID mark symbol is vendor option: no alphanumerics.

Ordering Information

Frontgrade Part Numbering Ordering Information

UT54LVDM228 * * * *

Lead Finish:
(A) = Hot Solder Dipped
(C) = Gold
(X) = Factory Option (Gold, Solder)

Screening Level:
(C) = HiRel Temperature Range Flow
(P) = Prototype Flow

Package Type:
(U) = 64-lead Flatpack (dual-in-line)

Access Time:
Not Applicable

Device Type:
UT54LVDM228 Crosspoint Switch

Notes:

1. Lead finish (A, C, F, or X) must be specified.
2. If and "X" is specified when ordering, then the part marking will match the lead finish and will be either “A” (solder) (gold).
3. Prototype Flow per Frontgrade Manufacturing Flows Document. Tested at 25C only. Lead finish is GOLI Radiation neither tested nor guaranteed.
4. HiRel Temperature Range Flow per Frontgrade Manufacturing Flows Document. Devices are tested at -5 room temp, and 125 °C. Radiation neither tested nor guaranteed.

Ordering Information

SMD Part Number Ordering Information

5962 * 01537 ** * * *

Lead Finish:
(A) = Hot Solder Dipped
(C) = Gold
(X) = Factory Option (Gold, Solder)

Case Outline:
(X) = 64-Lead-Flatpack (dual-in-line)

Class Designator:
(Q) = QML Class Q
(V) = QML Class V

Device Type:
(01) = LVDS Crosspoint Switch

SMD Project Number:
01537

Total Dose
(R) = 1E5 rad(Si)
(F) = 3E5 rad(Si)
(G) = 5E5 rad(Si)
(H) = 1E6 rad(Si)

Federal Stock Class Designator
No Options

Notes:

1. Lead finish must be specified.
2. If “X” is specified when ordering, the factory will determine lead finish. Part marking will reflect the lead finish applied to the device shipped.
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.

Revision History

Date	Revision #	Author	Change Description	Page #
1.0.0	11-13	MM	Last official release	
1.0.1	9-17-15	MM	Added package weight. Applied new Frontgrade Data Sheet template to the document.	p.1
1.0.2	8-16-21	BM	Added HBM ESD Rating: AMR Table	p.6
1.0.3	9-22-21	BM	SEL Limit sign	p.1, 6

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.