FRONTGRADE

DATASHEET

UT54LVDM031LV

Low Voltage Bus-LVDS Quad Driver

9/22/2021

Version #: 1.0.3

Features

- >400.0 Mbps (200 MHz) switching rates
- ±340mV nominal differential signaling
- 3.3 V power supply
- TTL compatible inputs
- 10mA output drivers
- Cold sparing all pins
- Ultra low power CMOS technology
- 3.0ns maximum, propagation delay
- 0.4ns maximum, differential skew
- Operational environment; total dose irradiation testing to MIL-STD-883 Method 1019
  - Total-dose: 300 krad(Si)
  - Latchup immune (LET ≤100 MeV-cm^2/mg)
- Packaging options:
  - 16-lead flatpack (0.7 grams)
- Standard Microcircuit Drawing 5962-06201
  - QML Q and V compliant part

Introduction

The UT54LVDM031LV Quad Bus-LVDS Driver is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400.0 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The UT54LVDM031LV accepts low voltage TTL input levels and translates them to low voltage (340mV) differential output signals. In addition, the driver supports a three-state function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state.

The UT54LVDM031LV and companion quad line receiver UT54LVDS032LV provide new alternatives to high power pseudo-ECL devices for high speed point-to-point interface applications.

All pins have Cold Spare buffers. These buffers will be high impedance when VDD is tied to V_{SS}.

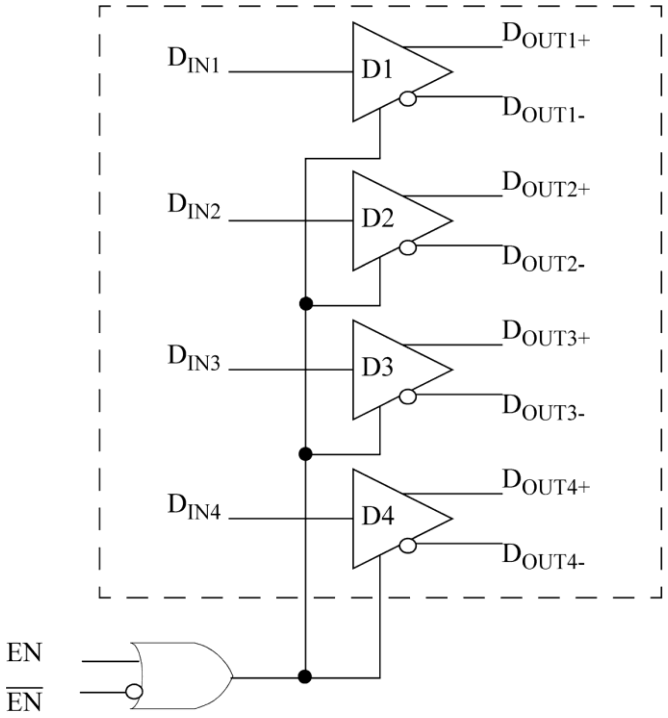

Figure 1. UT54LVDM031LV Bus-LVDS Quad Driver Block Diagram

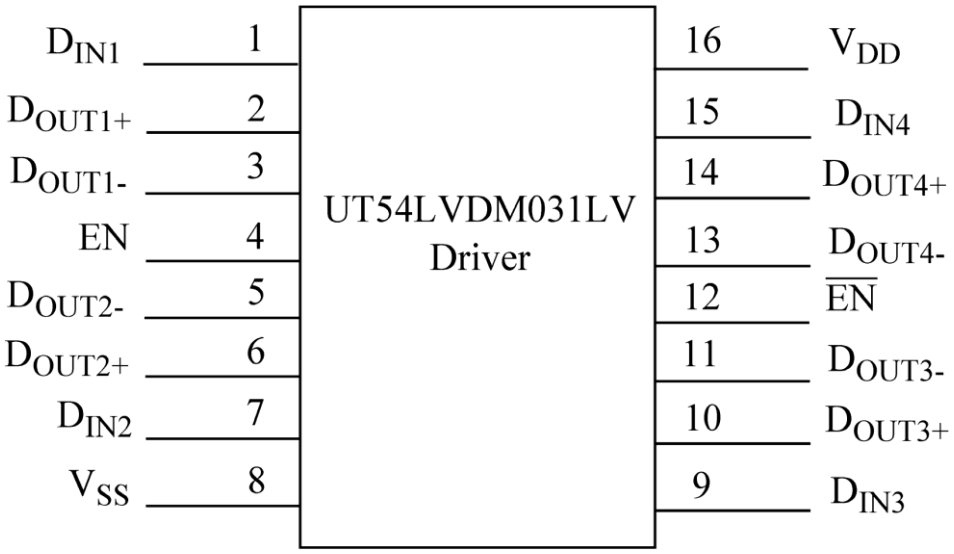

Figure 2. UT54LVDM031LV Pinout

Truth Table

Enables		Input	Output	
EN	$\overline{EN}$	D_{IN}	$D_{OUT}+$	D_{OUT-}
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

Pin Description

Pin No.	Name	Description
1, 7, 9, 15	D_{IN}	Driver input pin, TTL/CMOS compatible
2, 6, 10, 14	$D_{OUT}+$	Non-inverting driver output pin, LVDS levels
3, 5, 11, 13	D_{OUT-}	Inverting driver output pin, LVDS levels
4	EN	Active high enable pin, OR-ed with EN
12	$\overline{EN}$	Active low enable pin, OR-ed with EN
16	V_{DD}	Power supply pin, +3.3V ± 0.3V
8	V_{SS}	Ground pin

Applications Information

The UT54LVDM031LV Bus-LVDS driver's intended use is for both point-to-point (single termination) and multipoint (double termination) data transmissions over controlled impedance media. The transmission media may be

printed-circuit board traces, backplanes, or cables. Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics.

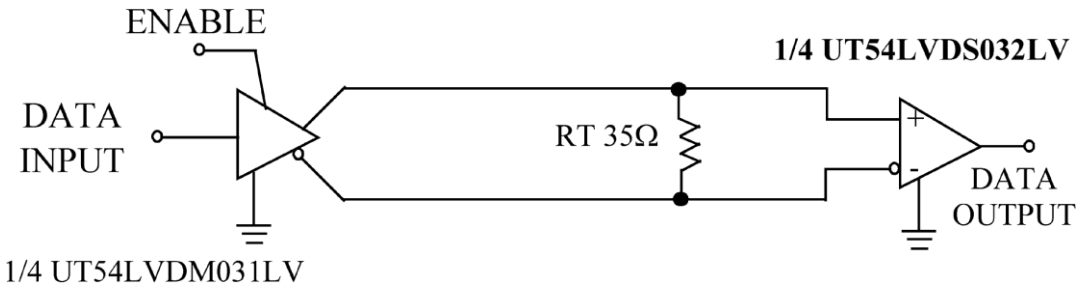

Figure 3. Point-to-Point Application

The UT54LVDM031LV differential line driver is a balanced current source design. A current mode driver, has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The current mode requires (as discussed above) that a resistive termination be employed to terminate the signal and to complete the loop as shown in Figure 3. AC or unterminated configurations are not allowed. The 10mA loop current will develop a differential voltage of 350mV across the 35Ω termination resistor which the receiver detects with a 250mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (340mV - 100mV = 250mV)). The signal is centered around +1.2V (Driver Offset, V_{OS}) with respect to ground as shown in Figure 4.

Note:

1. The steady-state voltage (V_{SS}) peak-to- peak swing is twice the differential voltage (VOD) and is typically 700mV.

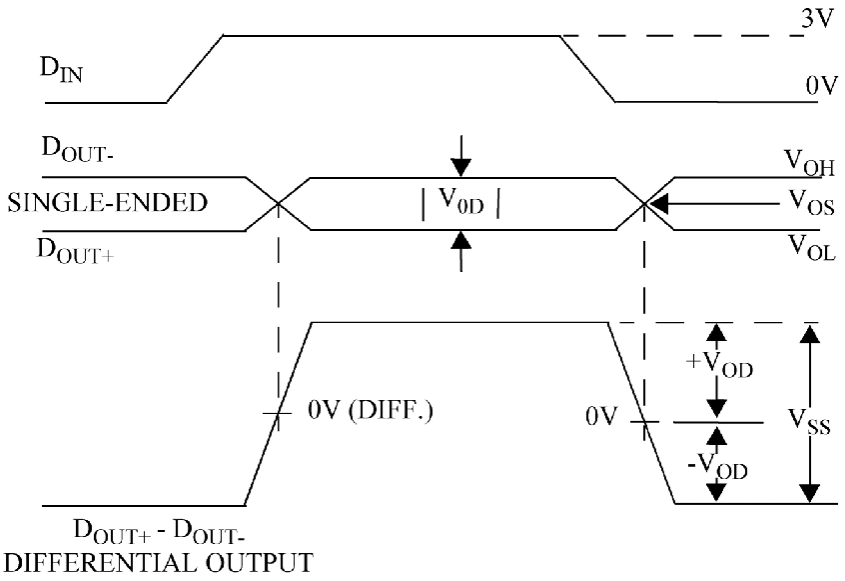

Figure 4. Bus-LVDS Driver Output

Note:

1. The footprint of the UT54LVDM031LV is the same as the industry standard Quad Differential (RS-422) Driver.

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most cases between 20 MHz - 50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static ICC requirements of the ECL/PECL design. LVDS requires 80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers.
The Three-State function allows the driver outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required.

Operational Environment

Parameter	Limit	Units
Total Ionizing Dose (TID)	3E5	rad(Si)
Single Event Latchup (SEL)	≤100	MeV-cm^2/mg

Absolute Maximum Ratings [1]

(Referenced to V_{SS})

Symbol	Parameter	Limits
V_{DD}	DC supply voltage	-0.3 to 4.0V
$V_{I/O}$	Voltage on any pin during operation	-0.3 to (V_{DD} + 0.3V)
	Voltage on any pin during cold spare	-.3 to 4.0V
ESD_{HBM}	HBM ESD Rating	1000V
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	1.25 W
T_J	Maximum junction temperature [2]	+150°C
Θ_{JC}	Thermal resistance, junction-to-case [3]	10°C/W
I_I	DC input current	±10mA

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to +175°C during burn-in and life test.
3. Test per MIL-STD-883, Method 1012.

Recommended Operating Conditions

Symbol	Parameter	Limits
V_{DD}	Positive supply voltage	3.0 to 3.6V
T_C	Case temperature range	-55 to +125°C
V_{IN}	DC input voltage	0 to V_{DD}

DC Electrical Characteristics 1, 2

(V_{DD} = 3.3V ± 0.3V; -55°C < TC < +125°C)

Symbol	Parameter	Condition	MIN	MAX	Unit
V_{IH}	High-level input voltage	(TTL)	2.0	V_{DD}	V
V_{IL}	Low-level input voltage	(TTL)	V_{SS}	0.8	V
V_{OL}	Low-level output voltage	R_L = 35Ω	0.855		V
V_{OH}	High-level output voltage	R_L = 35 Ω		1.750	V
I_{IN}	Input leakage current	V_{IN} = V_{DD} or GND, V_{DD} = 3.6V	-10	+10	µA
I_{CS}	Cold Spare Leakage Current	V_{IN}=3.6V, V_{DD}=V_{SS}	-20	+20	µA
V_{OD}[1]	Differential Output Voltage	R_L = 35Ω (figure 5)	250	400	mV
ΔV_{OD}[1]	Change in Magnitude of VOD for Complementary Output States	R_L = 35Ω (figure 5)		35	mV
V_{OS}	Offset Voltage	R_L = 35Ω, V_{OS} =	1.055	1.550	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States	R_L = 35Ω (figure 5) $\left(\frac{V_{OH}+V_{IN}}{2}\right)$		35	mV
V_{CL}[3]	Input clamp voltage	ICL = +18mA		-1.5	V
I_{OS} [2, 3]	Output Short Circuit Current	V_{IN} = V_{DD}, V_{OUT+} = 0V or V_{IN} = GND, V_{OUT-} = 0V		45	mA
I_{OZ}[3]	Output Three-State Current	EN = 0.8V and $\overline{EN}$ = 2.0 V, VOUT = 0V or V_{DD}, V_{DD} = 3.6V	-10	+10	µA
I_{CCL}	Loaded supply current, drivers enabled	R_L = 35Ω all channels V_{IN} = V_{DD} or V_{SS} (all inputs)		60.0	mA
I_{CCZ}[3]	Loaded supply current, drivers disabled	D_{IN} = V_{DD} or V_{SS} EN = V_{SS}, $\overline{EN}$ = V_{DD}		6.0	mA

Notes:

1. Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except differential voltages.
2. Output short circuit current (IOS) is specified as magnitude only, minus sign indicates direction only.
3. Guaranteed by characterization.

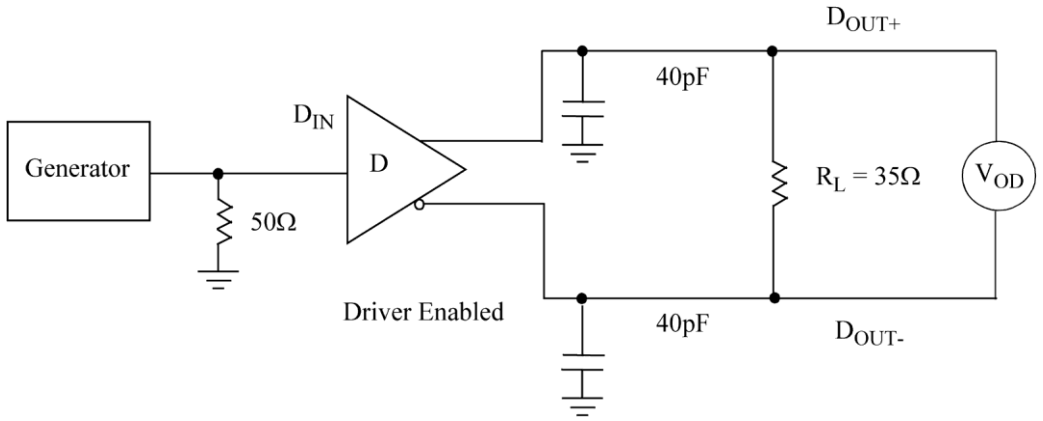

Figure 5. Driver VOD and V_{OS} Test Circuit or Equivalent Circuit

AC Switching Characteristics 1, 2, 3

(V_{DD} = +3.3V ± 0.3V, TA = -55℃ to +125℃)

Symbol	Parameter	MIN	MAX	Unit
t_{PHLD} [6]	Differential Propagation Delay High to Low (figures 6 and 7)	0.5	1.8	ns
t_{PLHD} [6]	Differential Propagation Delay Low to High (figures 6 and 7)	0.5	1.8	ns
t_{SKD}	Differential Skew (t_{PHLD} - t_{PLHD}) (figures 6 and 7)	0	0.4	ns
t_{SK1}	Channel-to-Channel Skew1 (figures 6 and 7)	0	0.5	ns
t_{SK2} [5]	Chip-to-Chip Skew (figure 6 and 7)		1.3	ns
t_{TLH} [4]	Rise Time (figures 6 and 7)		1.5	ns
t_{THL} [4]	Fall Time (figures 6 and 7)		1.5	ns
t_{PHZ}	Disable Time High to Z (figures 8 and 9)		5.0	ns
t_{PLZ}	Disable Time Low to Z (figures 8 and 9)		5.0	ns
t_{PZH}	Enable Time Z to High (figures 8 and 9)		7.0	ns
t_{PZL}	Enable Time Z to Low (figures 8 and 9)		7.0	ns

Notes:

1. Channel-to-Channel Skew is defined as the difference between the propagation delay of the channel and the other channels in the same chip with an event on the inputs.
2. Generator waveform for all tests unless otherwise specified: f = 1 MHz, ZO = 50, $t_r \leq 1$ns, and $t_f \leq 1$ns.
3. CL includes probe and jig capacitance.
4. Guaranteed by characterization
5. Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.
6. May be tested at higher load capacitance and the limit interpolated from characterization data to guarantee this parameter.

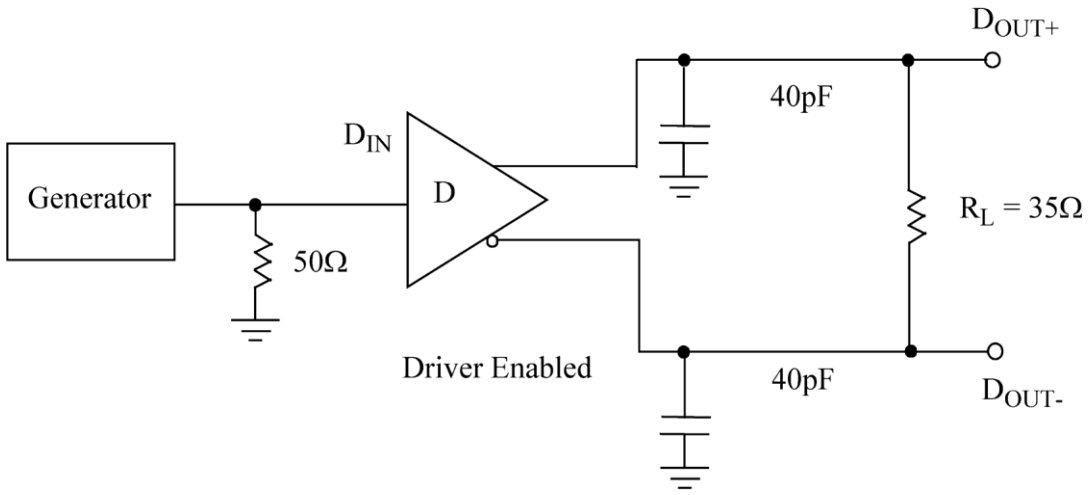

Figure 6. Driver Propagation Delay and Transition Time Test Circuit or Equivalent Circuit

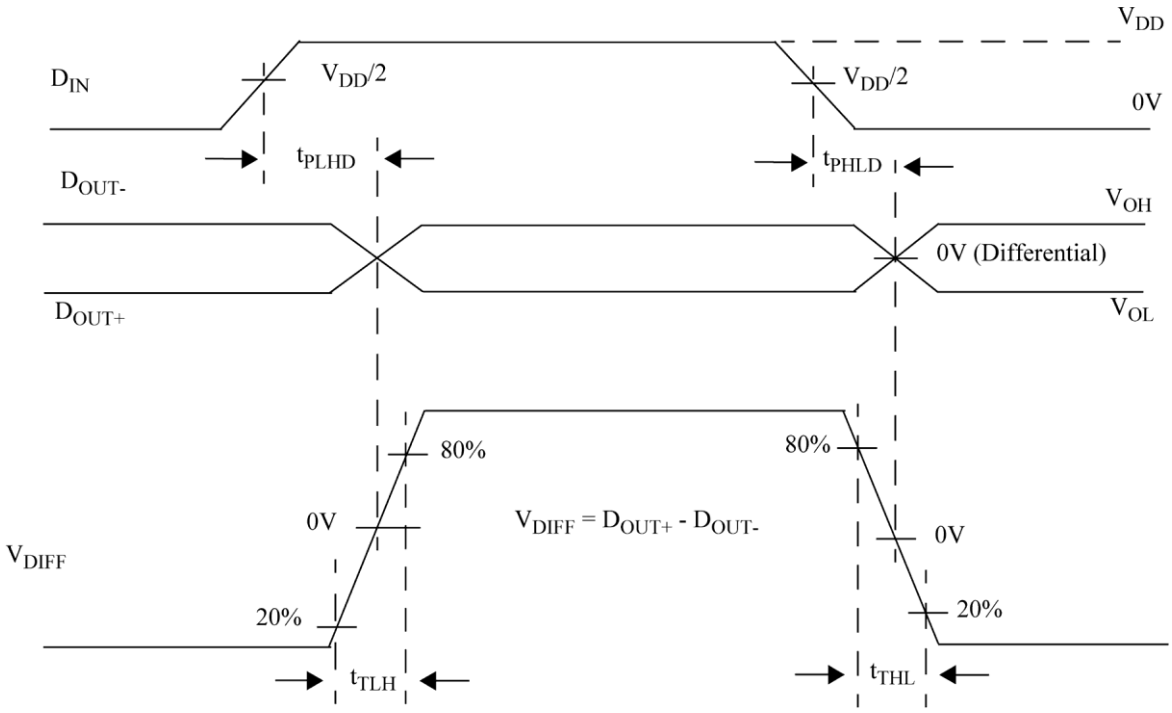

Figure 7. Driver Propagation Delay and Transition Time Waveforms

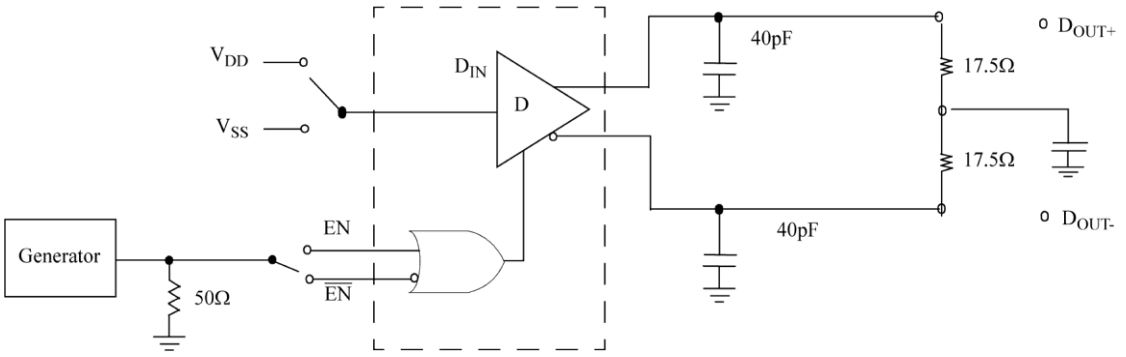

Figure 8. Driver Three-State Delay Test Circuit or Equivalent Circuit

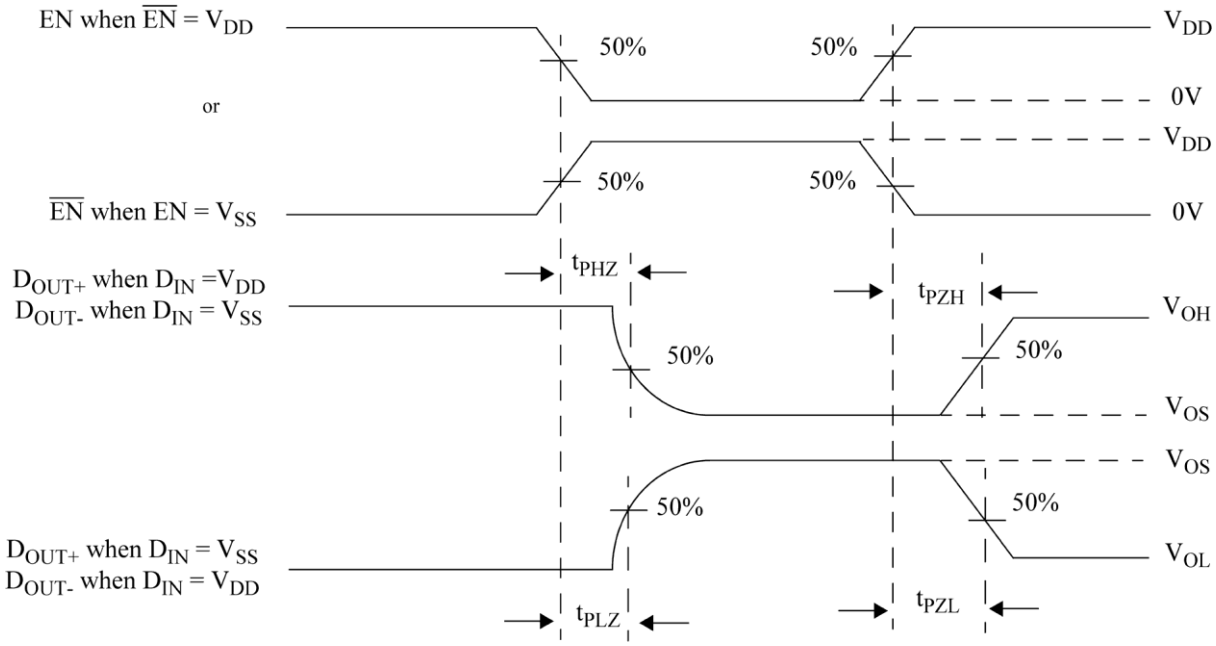

Figure 9. Driver Three-State Delay Waveform

Packaging

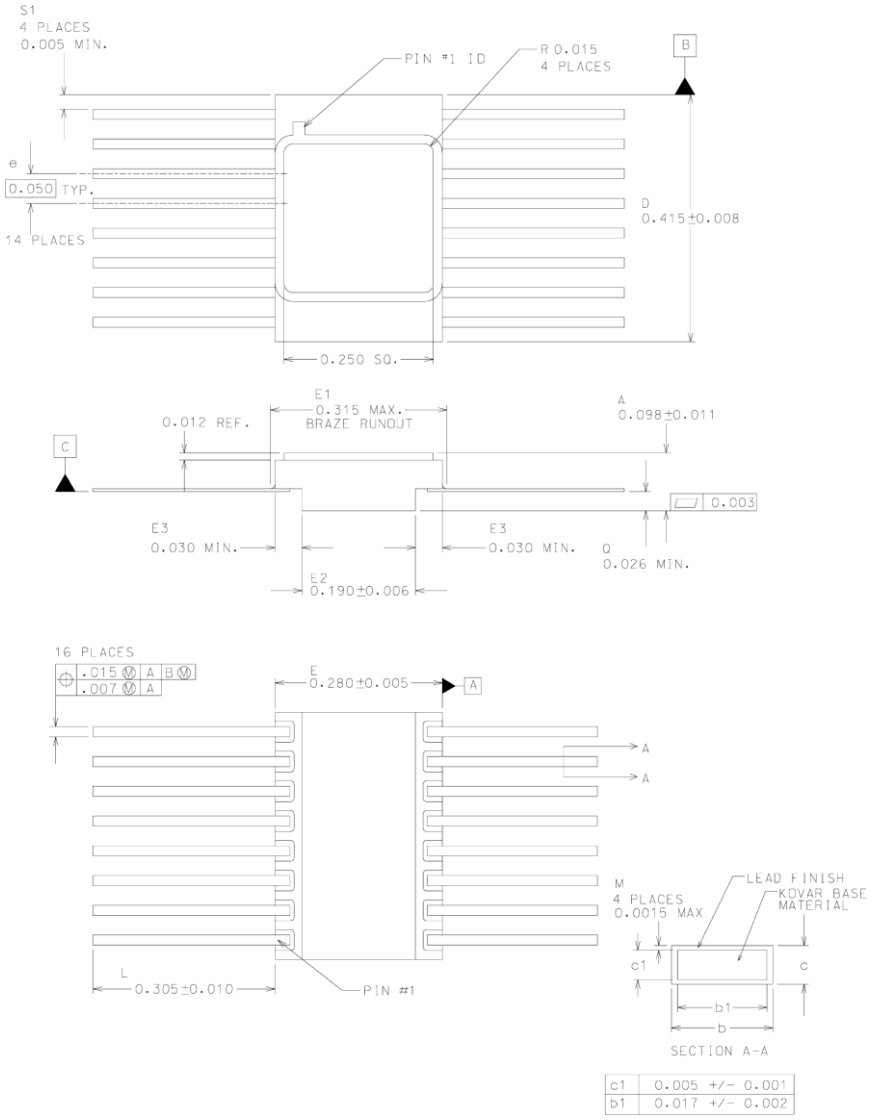

Figure 10. 16-pin Ceramic Flatpack

Notes:

1. All exposed metalized areas must be gold plated over electrically plated nickel per MIL-PRF-38535.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Dimensions symbology is in accordance with MIL-STD-1835.
5. Lead position and coplanarity are not measure.

Ordering Information

Frontgrade Part Numbering Ordering Information

UT54LVDM031LV- ****** ***** ***** *****

Lead Finish:
(A) = Hot Solder Dipped
(C) = Gold
(X) = Factory Option (Gold, Solder)

Screening Level:
(C) = HiRel Temperature Range Flow
(P) = Prototype Flow

Package Type:
(U) = 16-lead Flatpack (dual-in-line)

Access Time:
Not Applicable

Device Type:
UT54LVDM031LV Bus-LVDS Driver

Notes:

1. Lead finish (A, C, F, or X) must be specified.
2. If and "X" is specified when ordering, then the part marking will match the lead finish and will be either “A” (solder) or “C” (gold).
3. Prototype Flow per Frontgrade Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY Radiation neither tested nor guaranteed.
4. HiRel Temperature Range Flow per Frontgrade Manufacturing Flows Document. Devices are tested at -55°C room temp, and 125°C. Radiation neither tested nor guaranteed.

Ordering Information

SMD Part Number Ordering Information

5962 * 06201 ** * * *

Lead Finish:
(A) = Hot Solder Dipped
(C) = Gold
(X) = Factory Option (Gold, Solder)

Case Outline:
(Y) = 16-Lead-Flatpack (dual-in-line)

Class Designator:
(Q) = QML Class Q
(V) = QML Class V

Device Type:
(01) = LVDS Driver 100K, Rad(Si) 300K Rad(Si)

Drawing Number:
5962-0621

Total Dose
(R) = 1E5 rad(Si)
(F) = 3E5 rad(Si)

Federal Stock Class Designator
No Options

Notes:

1. Lead finish (A, C, or X) must be specified.
2. If "X" is specified when ordering, the factory will determine lead finish. Part marking will reflect the lead finish applied to the device shipped.
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.

Revision History

Date	Revision #	Author	Change Description	Page #
9-12	1.0.0	MM	Last official release	
9-17-15	1.0.1	MM	Added package weight. Applied new Frontgrade Data Sheet template to the document.	p. 1
8-16-21	1.0.2	BM	Added HBM ESD Rating: AMR Table	p. 5
9-22-21	1.0.3	BM	Added Operational Environmental Table, SEL Limit sign,	p. 1, 4

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.