



# FRONTGRADE

## DATASHEET

### UT54BS3245

8-bit Bus Switch

8/19/2021  
Version #: 2.0.5

## Features

- 3.3V operating power supply with typical 11 $\Omega$  switch connection between ports
- 5.0V operating power supply with typical 5 $\Omega$  switch connection between ports
- Bidirectional operation
- Ultra-low power CMOS technology
- ESD Rating HBM: 2000V, Class 2
- Signal Isolation: -60dB
- Channel Bandwidth (3dB): 500MHz
- Standard Microcircuit Drawing (SMD):
  - 5962-15244
  - QML Q and V compliant part
- Package Options: 20-Lead Flatpack

## Operational Environment

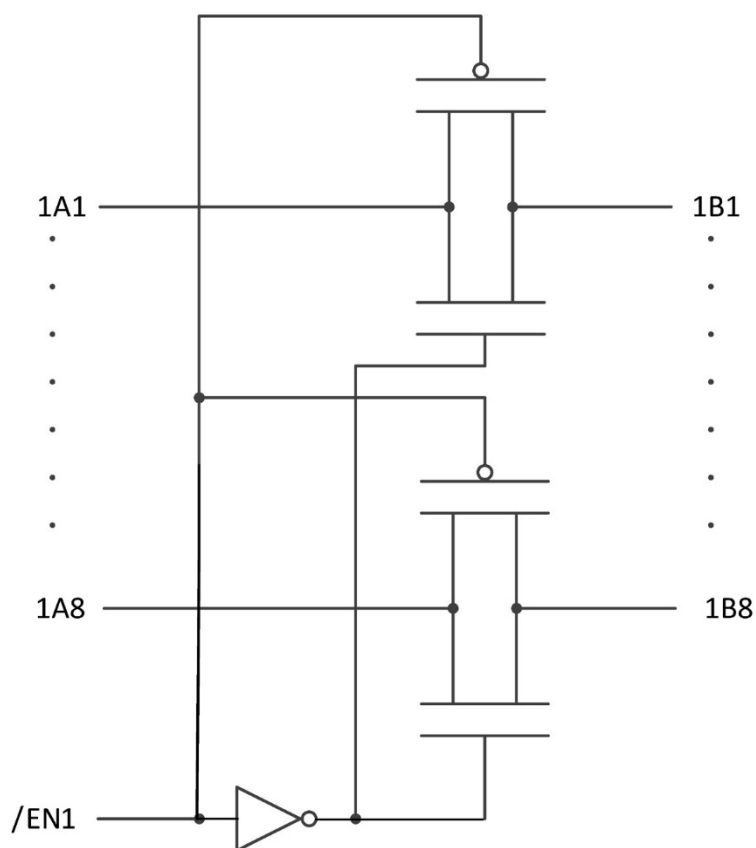
- Temperature Range: -55°C to +125°C
- Total Dose: 300 krad(Si)
- SEL Immune:  $\leq 100$  MeV-cm<sup>2</sup>/mg

## Applications

- Memory Interface
- Bus Isolation
- Redundancy
- Supports Analog Applications

## Introduction

The UT54BS3245 provides 8 bits of high-speed CMOS-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The device is organized as one 8-bit low-impedance switch. When output enable (/EN) is low, the 8-bit bus switch is on and port A is connected to port B. When /EN is high, the switch is open and a high-impedance state exists between the two ports.

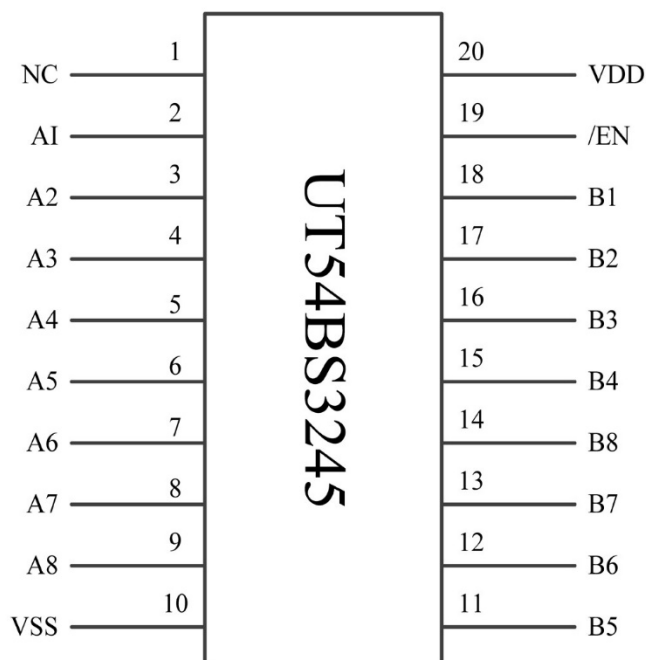


## Pinlist

TO	=	TTL Output
TTB	=	Three-State TTL Bidirectional
CI	=	CMOS Input
TUI	=	TTL Input (Internally Pulled High)
TI	=	TTL Input
TTO	=	Three-State TTL Output
DIO	=	Differential Input/Output

**Table 1: Pinlist**

Number	Name	Description
2, 3, 4, 5, 6, 7, 8, 9,	nA	Port A Pins
11, 12, 13, 14, 15, 16, 17, 18	nB	Port B pins
19	/EN	Active LOW enable pin
10	V <sub>SS</sub>	Ground Pin
20	V <sub>DD</sub>	Supply Pin, +3.3V or +5.0V
1	NC	No Connect (electrically not connected to die)

**Package Pinout Diagram**


## Absolute Maximum Ratings<sup>1,2</sup>

**Table 2: Absolute Maximum Ratings**

Symbol	Parameter	MIN	MAX	Units
V <sub>DD</sub>	Positive Supply Voltage	-0.5	+7.2	V
V <sub>I</sub>	Input Voltage	-0.5	V <sub>DD</sub> +0.3	V
I <sub>CCC</sub>	DC Channel Current		65	mA
P <sub>D</sub>	Max Power Dissipation <sup>3</sup>		1.6	W
T <sub>J</sub>	Junction Temperature		+150	°C
θ <sub>JC</sub>	Thermal resistance, junction-to-case		15	°C/W
T <sub>STG</sub>	Storage Temperature	-65	+150	°C
ESD <sub>HBM</sub>	ESD Protection <sup>4</sup>		2000	V

### Notes:

- Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification are not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
- All voltages referenced to V<sub>SS</sub>
- Per MIL-STD-883, method 1012, section 3.4.1,  $P_D = (T_J(\text{max}) - T_C(\text{max})) / \theta_{JC}$
- Per MIL-STD-883, method 3015, Table 3

## Operational Environment<sup>1</sup>

**Table 3: Operational Environment**

Symbol	Parameter	Limit	Units
TID	Total Ionizing Dose <sup>2</sup>	300	krad(Si)
SEL	Single Event Latchup Immunity <sup>3</sup>	≤100	MeV-cm <sup>2</sup> /mg

### Notes:

- For devices with procured with a total ionizing dose tolerance guarantee, post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to maximum TID level procured.
- Per MIL-STD-883, method 1019, condition A
- SEL is performed at  $V_{DD}$  = Max Voltage at 125°C

## Recommended Operating Conditions (1)

**Table 4: Recommended Operating Conditions**

Symbol	Parameter	Conditions	MIN	MAX	Units
$V_{DD}$	Positive Supply Voltage		3.0 or 4.5	3.6 or 5.5	V
$V_{IN}$	Input Voltage on any pin		0.0	$V_{DD}$	V
$T_C$	Case Temperature Range		-55	+125	°C
$t_R$	Rise time, logic inputs	Transition from $V_{IL}$ to $V_{IH}$		5	ns
$t_F$	Fall time, logic inputs	Transition from $V_{IH}$ to $V_{IL}$		5	ns
$I_{CCC}$	DC Channel Current			60	mA

### Note:

- All voltages referenced to  $V_{SS}$

## Electrical Characteristics<sup>1</sup>

( $V_{DD} = 5.0V \pm 0.5V$ ,  $3.3V \pm 0.3V$ ,  $-55^{\circ}C < T_C < +125^{\circ}C$ ); Unless otherwise noted,  $T_C$  is per the temperature range ordered

**Table 5: DC Electrical Characteristics**

Symbol	Parameter	Conditions	MIN	MAX	Units
$V_{IH}$	High digital input voltage	$V_{DD} = 3.6, 5.5$	$0.7 * V_{DD}$		V
$V_{IL}$	Low digital input voltage	$V_{DD} = 3.0, 4.5$		$0.3 * V_{DD}$	V
$I_{ID}$	Leakage current digital	$V_{DD} \text{ (max)}; V_I = V_{DD} \text{ or } V_{SS}$	-1	1	$\mu A$
$I_{IA}$	Leakage current analog	$V_{DD} \text{ (max)}; V_I = V_{DD} \text{ or } V_{SS}$	-1	1	$\mu A$
$I_{DD}$	Active supply current	$V_{DD} = 3.6, 5.5$		0.1	mA/MHz
$I_{DDQ}$	Quiescent Supply Current	$V_{DD} \text{ (max)}; I_O = 0mA; /EN = V_{DD}$		10	$\mu A$
$C_i$	Input Capacitance (/EN) <sup>2</sup>	$V_I = V_{DD} \text{ or } V_{SS}$		18	pF
$C_{IO(OFF)}$	Channel pin capacitance (channel disabled) <sup>2</sup>	$V_{DD} \text{ (max)}; V_O = V_{DD} \text{ or } V_{SS}; V_I = V_{DD}/2; /EN = V_{DD}$		18	pF
$R_{ONL}$	Resistance through switch (channel input low) <sup>3</sup>	$V_{DD} = 4.5V, V_I = V_{SS}, /EN = 0V, I_O = 30mA$		10	$\Omega$
		$V_{DD} = 4.5V, V_I = V_{SS}, /EN = 0V, I_O = 15mA$		10	$\Omega$
		$V_{DD} = 3.0V, V_I = V_{SS}, /EN = 0V, I_O = 30mA$		12	$\Omega$
		$V_{DD} = 3.0V, V_I = V_{SS}, /EN = 0V, I_O = 15mA$		12	$\Omega$
$R_{ONH}$	Resistance through switch (channel input high) <sup>3</sup>	$V_{DD} = 4.5V, V_I = V_{DD}, /EN = 0V, I_O = -30mA$		10	$\Omega$
		$V_{DD} = 4.5V, V_I = V_{DD}, /EN = 0V, I_O = -15mA$		10	$\Omega$
		$V_{DD} = 3.0V, V_I = V_{DD}, /EN = 0V, I_O = -30mA$		12	$\Omega$
		$V_{DD} = 3.0V, V_I = V_{DD}, /EN = 0V, I_O = -15mA$		12	$\Omega$
$R_{ON(FLAT)}$	Switch on resistance <sup>3</sup>	$V_{DD} = 4.5V, /EN = 0V, I_O = \pm 15mA, 25^{\circ}C$ $V_{IN} = V_{SS}, V_{DD}/2, V_{DD}$		2	$\Omega$
		$V_{DD} = 3.0V, /EN = 0V, I_O = \pm 15mA, 25^{\circ}C$ $V_{IN} = V_{SS}, V_{DD}/2, V_{DD}$		10	$\Omega$

### Notes:

1. All voltages referenced to  $V_{SS}$
2. Per MIL-STD-883, method 3012
3. Guaranteed by characterization

## AC Electrical Characteristics<sup>1</sup>

( $V_{DD} = 5.0V \pm 0.5V$ ,  $3.3V \pm 0.3V$ ,  $-55^{\circ}C < T_C < +125^{\circ}C$ ); Unless otherwise noted,  $T_C$  is per the temperature range ordered

**Table 6: AC Electrical Characteristics**

Symbol	Parameter	Conditions	MIN	MAX	Units
$t_{PD15}$	Channel Propagation Delay <sup>1</sup>	$V_{DD} = 5.0V \pm 0.5V$ , $I_1 = \pm 15mA$ , $/EN = V_{SS}$		250	ps
$t_{EN}$	Channel Enable Delay <sup>2</sup>	$V_{DD} = 5.0V \pm 0.5V$	1	5	ns
$t_{DIS}$	Channel Disable Delay <sup>2</sup>	$V_{DD} = 5.0V \pm 0.5V$	1	5	ns
$t_{PD15}$	Channel Propagation Delay <sup>1</sup>	$V_{DD} = 3.3V \pm 0.3V$ , $I_1 = \pm 15mA$ , $/EN = V_{SS}$		250	ps
$t_{EN}$	Channel Enable Delay <sup>2</sup>	$V_{DD} = 3.3V \pm 0.3V$	1	7	ns
$t_{DIS}$	Channel Disable Delay <sup>2</sup>	$V_{DD} = 3.3V \pm 0.3V$	1	7	ns

### Notes:

1. The propagation delay through the channel is based on the RC time constant of the channel capacitance and maximum channel resistance for defined  $V_{DD}$
2. Measured at 300mV above or below steady state output voltage using output test load circuit

## Table 7: Signal Characteristics

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
$X_{TALK}^1$	Channel Cross-Talk <sup>1,2</sup>	$V_{DD} = 5.0V$			-60	dB
$X_{TALK}^1$	Channel Cross-Talk <sup>1,2</sup>	$V_{DD} = 3.3V$			-60	dB
$ISO_{OFF}^1$	Off Isolation <sup>1,2</sup>				-60	dB

### Notes:

1. Guaranteed by design
2.  $R_L = 50\Omega$ ,  $C_L = 50pF$ ,  $f_{in} = 1MHz$ ,  $V_{IN} = 1VRMS$  centered at  $V_{DD}/2$



## Timing Diagram

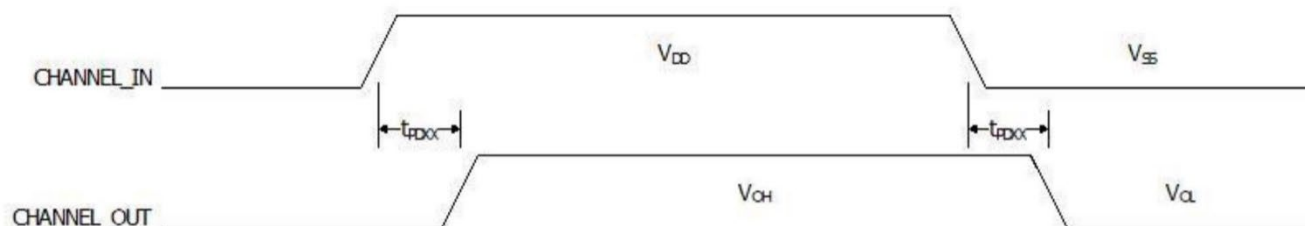


Figure 3: Channel Propagations Delay (/EN =  $V_{SS}$ )

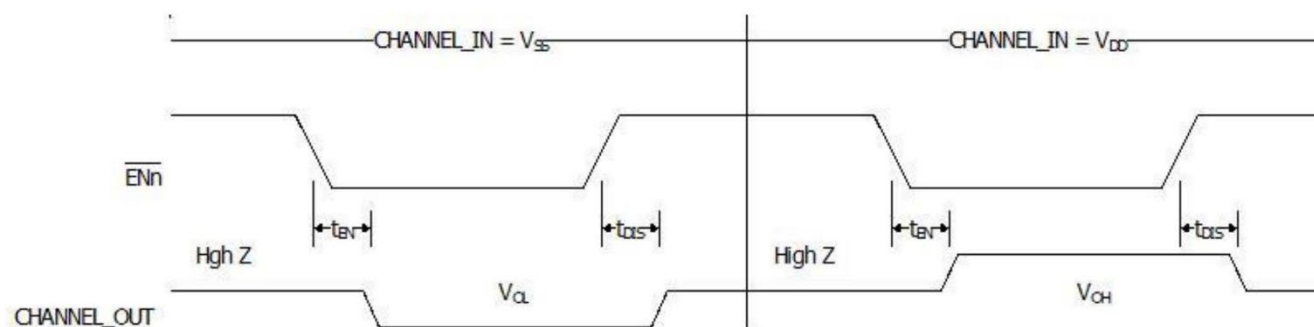


Figure 4: Enable Timing

## Test Loads

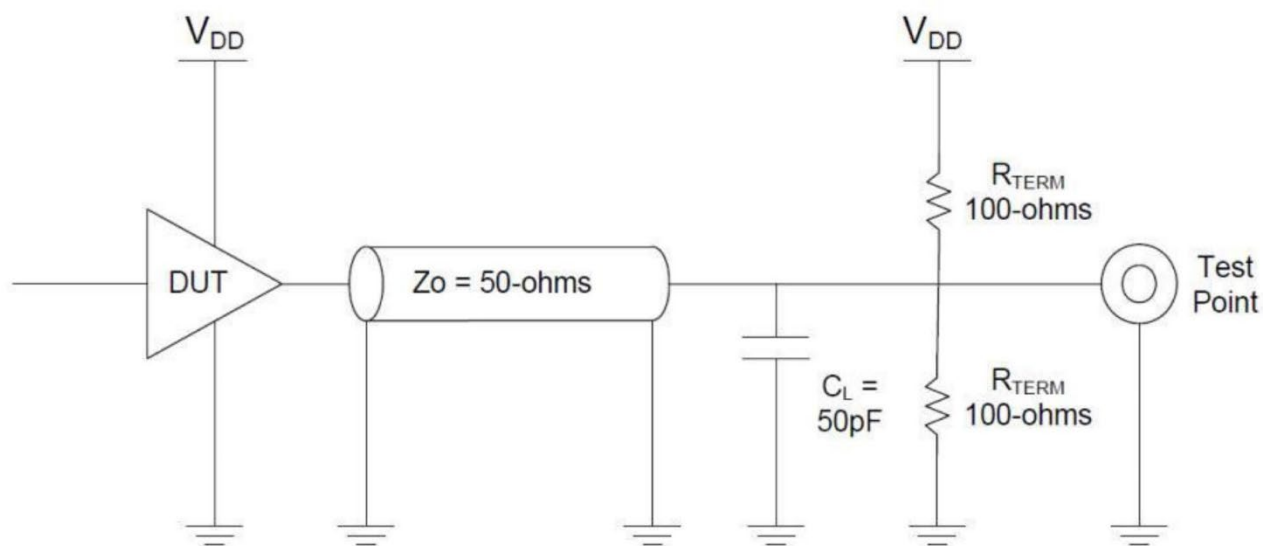
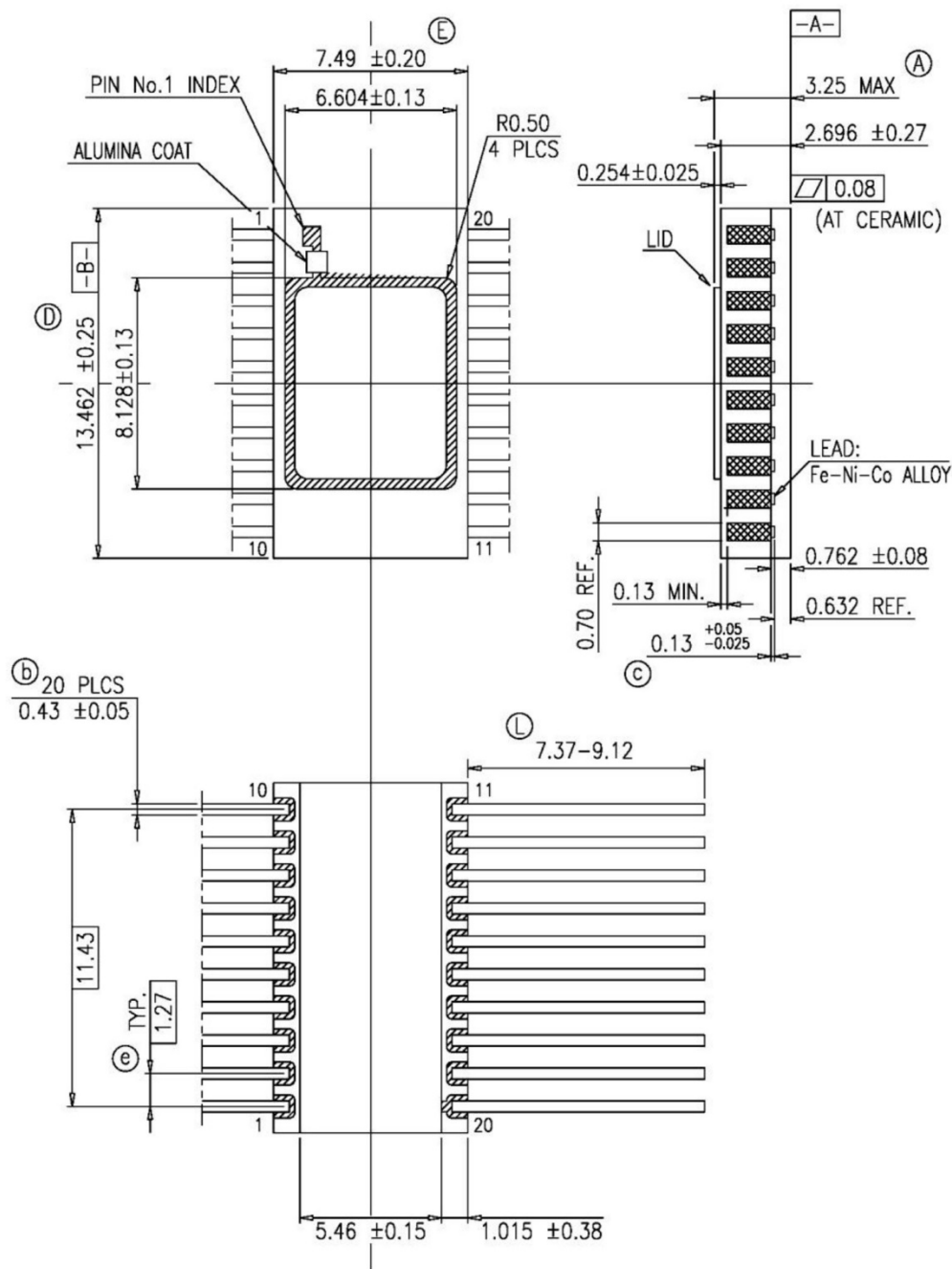


Figure 5: Standard Test Load

### Package Drawings

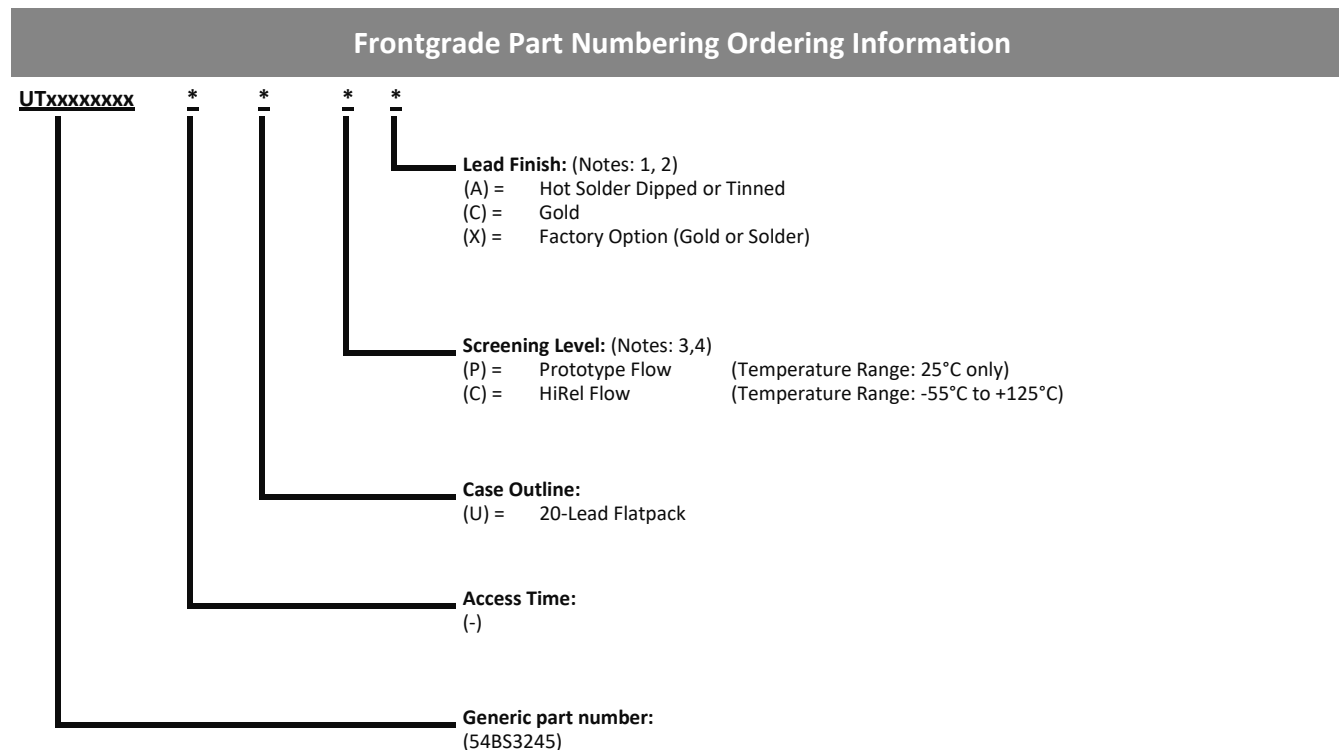


#### Notes:

1. The Lid Is Connected to  $V_{SS}$ .
2. Dimensions are in Millimeters.

## Ordering Information

### Generic Datasheet Part Numbering

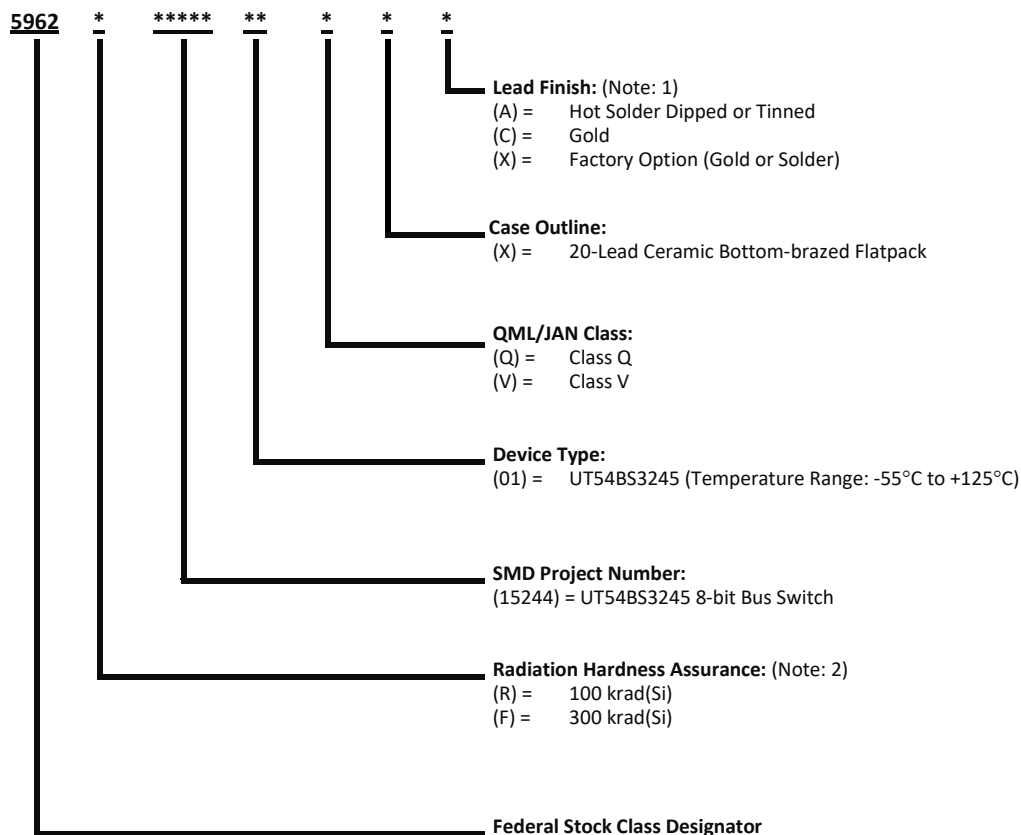


#### Notes:

- Lead finish (A, C, F, or X) must be specified.
- If an "X" is specified when ordering, then the part marking will match the lead finish applied to the device shipped
- Prototype Flow per Frontgrade Manufacturing Flows Document. Lead finish is Factory Option "C" only. Radiation is neither tested nor guaranteed.
- HiRel Flow per Frontgrade Manufacturing Flows Document. Radiation TID tolerance may (or may not) be ordered.

### SMD Part Numbering

#### SMD Part Number Ordering Information



#### Notes:

1. Lead finish must be specified. If "X" is specified when ordering, the factory will determine lead finish. Part marking will reflect the lead finish applied to the device shipped.
2. A radiation hardness assurance level must be selected. The use of "-" indicates no radiation hardness assurance guarantee.

## Revision History

**Table 8: Revision History**

Date	Revision #	Author	Change Description	Page #
05/01/2016	1.0.0	MM	Updated datasheet to reflect Frontgrade logo, colors, and modified format. Updated the following specifications: $R_{ON}$ , $I_{IA}$ , $I_{DD}$ , $I_{DDQ}$ , $T_{EN}$ , and $T_{DIS}$ .	
06/23/2016	2.0.0	BM	Released Datasheet. Updated capacitance, propagation delay, and minor formatting.	
6/30/2016	2.0.1	BM	FEATURES: 20-Lead Flatpack; IDDQ: CONDITIONS: $/EN=V_{DD}$	
01/04/2017	2.0.2	BM	FEATURES: QML Q, V compliant part	
09/12/2019	2.0.3	BM	Package Pinout Diagram, Fig. 2 - Error Correction: Pins 11-14	3
08/19/2021	2.0.5	BM	ROC Table, Input $t_R$ , $t_F$ parameter updates.	4

## Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the <b>datasheet is subject to change</b> . Specifications can be <b>TBD</b> and the part package and pinout are <b>not final</b> .
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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