

FRONTGRADE

DATASHEET

UT54ACTS86/UT54ACS86

Quadruple 2-Input Exclusive OR Gates

10/2/2017

Version #: 1.0

Features

- 1.2μ CMOS (ACTS) and 0.6μ CRH CMOS (ACS)
 - > Latchup immune
- High speed
- Low power consumption
- Single 5-volt supply
- Available QML Q or V processes
- Flexible package
 - > 14-pin DIP (ACTS only)
 - > 14-lead flatpack
- UT54ACS86 - SMD 5962-96538
- UT54ACTS86 - SMD 5962-96539

Description

The UT54ACS86 and the UT54ACTS86 are quadruple 2-input exclusive OR gates. The devices perform the Boolean function $Y = A \oplus B = \bar{A}B + A\bar{B}$ in positive logic.

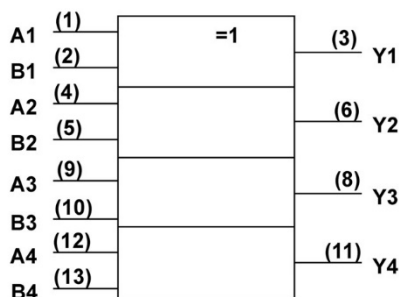
An application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The devices are characterized over full military temperature range of -55°C to +125°C.

Function Table

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Logic Symbol



Note:

1. Logic symbol in accordance with ANSI/IEEE standard 91-1984 and IEC Publication 617.12

Pinouts

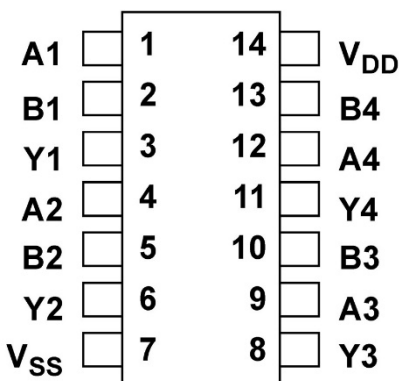


Figure 1: 14-Pin Dip Top View

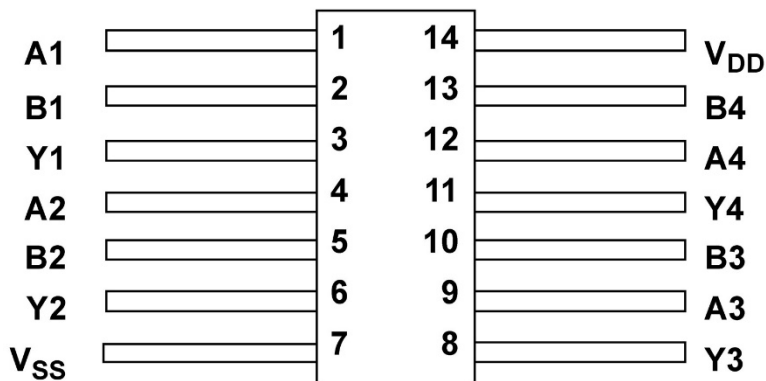
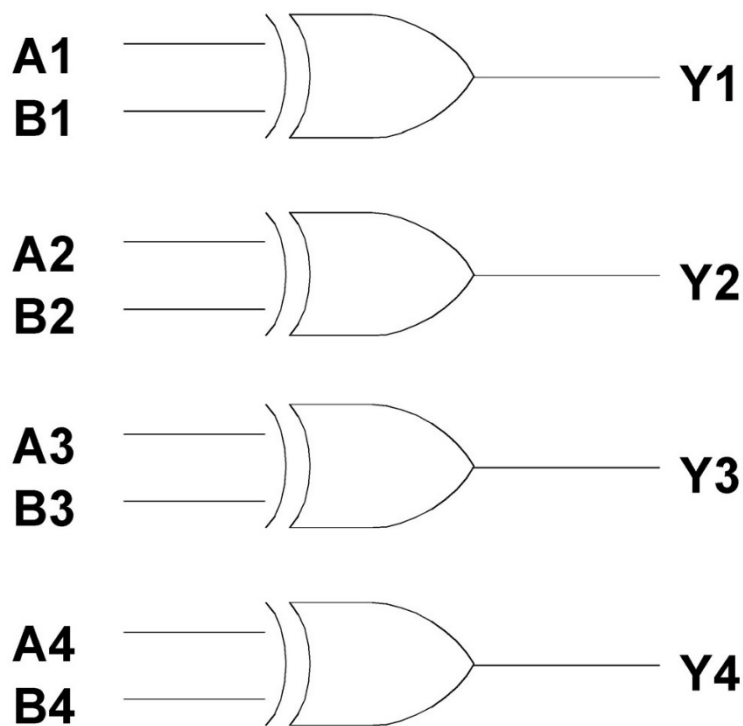


Figure 2: 14-Lead Flatpack Top View

Logic Diagram



Operational Environment¹

Parameter	Limit	Units
Total Dose	1.0E6 (ACTS) 500K (ACS)	rads(Si)
SEU Threshold ²	80	MeV-cm ² /mg
SEL Threshold	120	MeV-cm ² /mg
Neutron Fluence	1.0E14	n/cm ²

Notes:

1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

Absolute Maximum Ratings

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage any pin	-.3 to $V_{DD} + .3$	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
T_{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ_{JC}	Thermal resistance junction to case	15	°C/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation	1	W

Notes:

- Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other condition beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	4.5 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to + 125	°C

DC Electrical Characteristics⁷

($V_{DD} = 5.0V \pm 10\%$; $V_{SS} = 0V^6$, $-55^\circ C < T_C < +125^\circ C$); Unless otherwise noted, T_C is per the temperature range ordered.

Symbol	Parameter		Condition	MIN	MAX	Unit
V_{IL}	Low-level input voltage ¹ ACTS ACS				0.8 .3 V_{DD}	V
V_{IH}	High-level input voltage ¹ ACTS ACS			.5 V_{DD} .7 V_{DD}		V
I_{IN}	Input leakage current ACTS/ACS		$V_{IN} = V_{DD} \text{ or } V_{SS}$	-1	1	μA
V_{OL}	Low-level output voltage ³ ACTS ACS		$I_{OL} = 8.0mA$ $I_{OL} = 100\mu A$		0.40 0.25	V
V_{OH}	High-level output voltage ³ ACTS ACS		$I_{OH} = -8.0mA$ $I_{OH} = -100\mu A$.7 V_{DD} $V_{DD} - 0.25$		V
I_{OS}	Short-circuit output current ^{2,4} ACTS/ACS		$V_O = V_{DD} \text{ and } V_{SS}$	-200	200	mA
I_{OL}	Output current ¹⁰ (Sink)		$V_{IN} = V_{DD} \text{ or } V_{SS}$ $V_{OL} = 0.4V$	8		mA
I_{OH}	Output current ¹⁰ (Source)		$V_{IN} = V_{DD} \text{ or } V_{SS}$ $V_{OH} = V_{DD} - 0.4V$	-8		mA
P_{total}	Power dissipation ^{2,8,9}		$C_L = 50pF$		1.8	mW/ MHz
I_{DDQ}	Quiescent Supply Current	Pre-Rad	$V_{DD} = V_{DD} \text{ MAX}$		10	μA
		Post-Rad Device Type - 01			50	
ΔI_{DDQ}	Quiescent Supply Current Delta ACTS		For input under test $V_{IN} = V_{DD} - 2.1V$ For all other inputs $V_{IN} = V_{DD} \text{ or } V_{SS}$ $V_{DD} = 5.5V$		1.6	mA
C_{IN}	Input capacitance ⁵		$f = 1MHz @ 0V$		15	pF
C_{OUT}	Output capacitance ⁵		$f = 1MHz @ 0V$		15	pF

Notes:

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH(min)} + 20\%$, -0% ; $V_{IL} = V_{IL(max)} + 0\%$, -50% , as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH(min)}$ and $V_{IL(max)}$.
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density $\leq 5.0E5$ amps/cm², the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6. Maximum allowable relative shift equals 50mV.
7. Device type 01 is only offered with a TID tolerance guarantee of 1E6 rads(Si) (ACTS only), 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.
8. Power does not include power contribution of any TTL output sink current.
9. Power dissipation specified per switching output.
10. This value is guaranteed based on characterization data, but not tested.

AC Electrical Characteristics²

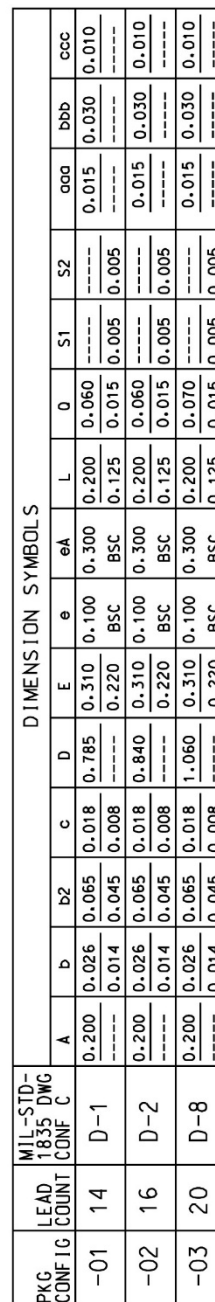
($V_{DD} = 5.0V \pm 10\%$; $V_{SS} = 0V^1$, $-55^\circ C < T_C < +125^\circ C$); Unless otherwise noted, T_C is per the temperature range ordered.

Symbol	Parameter	Minimum	Maximum	Unit
t_{PHL}	Data to input	1	14	ns
t_{PLH}	Data to input	1	13	ns

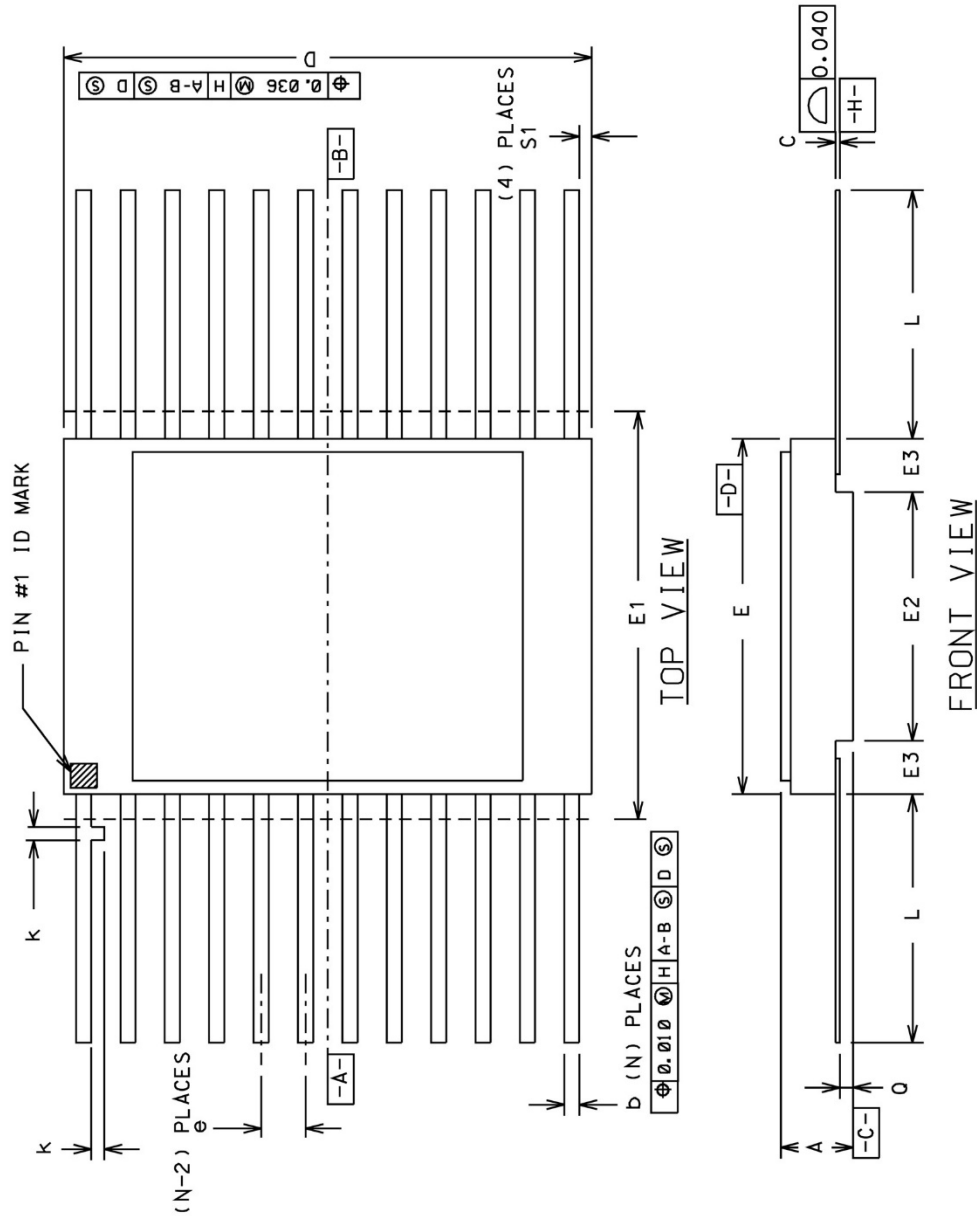
Notes:

1. Maximum allowable relative shift equals 50mV.
2. Device type 01 is only offered with a TID tolerance guarantee of 1E6 rads(Si) (ACTS only), 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

Side-Brazed Packages



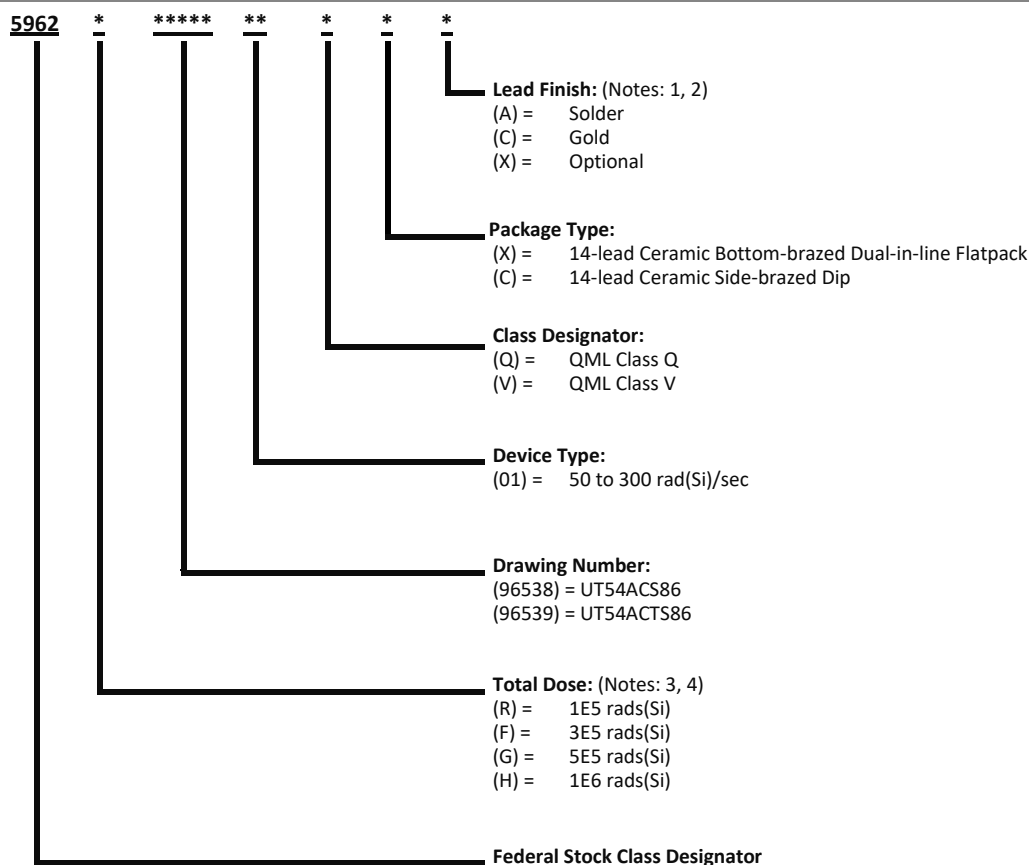
Flatpack Packages



PKG. CONFIG	LEAD COUNT	ML-STD 1835 DWG CONF B	DIMENSION SYMBOLS												
			A	b	c	D	E	E1	E2	E3	e	k	L	Q	S1
-03	14	F-2A	0.115 0.045	0.022 0.015	0.009 0.004	0.390 -----	0.260 0.235	0.290 -----	----- 0.130	----- 0.030	0.050 BSC	0.015 0.008	0.370 0.270	0.045 0.026	----- 0.005
-04	16	F-5A	0.115 0.045	0.022 0.015	0.009 0.004	0.440 -----	0.285 0.245	0.315 -----	----- 0.130	----- 0.030	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	----- 0.005
-05	20	F-9A	0.115 0.045	0.022 0.015	0.009 0.004	0.540 -----	0.300 0.245	0.330 -----	----- 0.130	----- 0.030	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	----- 0.000

Ordering Information

UT54ACS86/UT54ACTS86 SMD Part Number Ordering Information



Notes:

- Lead finish (A, C, or X) must be specified.
- If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
- Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
- Device type 01 is only offered with a TID tolerance guarantee of 1E6 rads(Si) (ACTS only), 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

Revision History

Date	Revision #	Author	Change Description	Page #
10/17		RT	Edited IDDQ Applied new CAES Data Sheet template to the document.	4
1/18		RT	Updated to reflect current SMD	

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet is subject to change . Specifications can be TBD and the part package and pinout are not final .
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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