



FRONTGRADE

DATASHEET

UT54ACS373/UT54ACTS373

Octal Transparent Latches with
Three State Outputs

11/1/2010
Version #: 1.0

Features

- 8 latches in a single package
- Three-state bus-driving true outputs
- Full parallel access for loading
- 1.2μ CMOS
 - > Latch up immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
 - > 20-pin DIP
 - > 20-lead flatpack
- UT54ACS373 - SMD 5962-96588
- UT54ACTS373 - SMD 5962-96589

Description

The UT54ACS373 and the UT54ACTS373 are 8-bit latches with three-state outputs designed for driving highly capacitive or relatively low-impedance loads. The device is suitable for buffer registers, I/O ports, and bidirectional bus drivers.

The eight latches are transparent D latches. While the enable(C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

An output-control input (\overline{OC}) places the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. The high-impedance third state and increased drive provide the capability to drive the bus line in a bus-organized system without need for interface or pull-up components.

The output control \overline{OC} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The devices are characterized over full military temperature range of -55°C to +125°C.

Function Table

Inputs		Outputs	
\overline{OC}	C	nD	nQ
L	H	H	H
L	H	L	L
L	L	X	nQ ₀
H	X	X	Z ¹

Note:

1. Data may be latched internally.

Pinouts

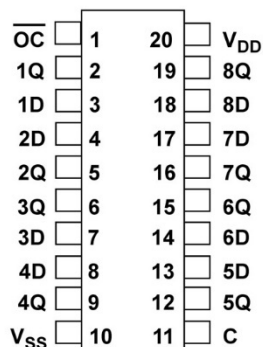


Figure 1: 20-Pin DIP, Top View

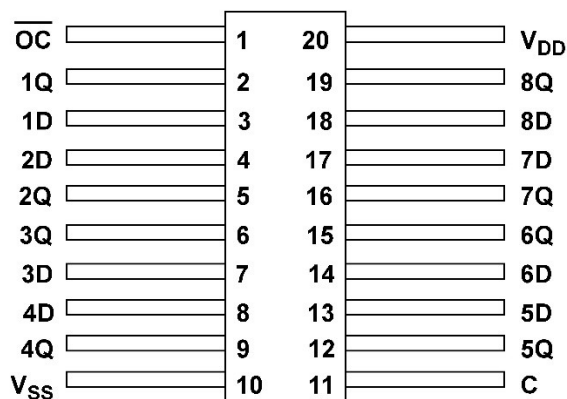
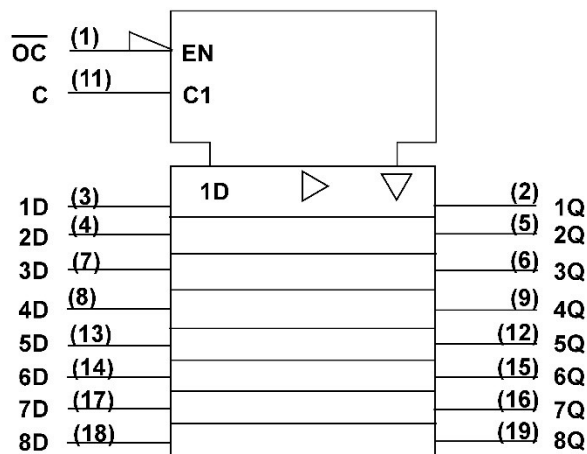


Figure 2: 20-Lead Flatpack, Top View

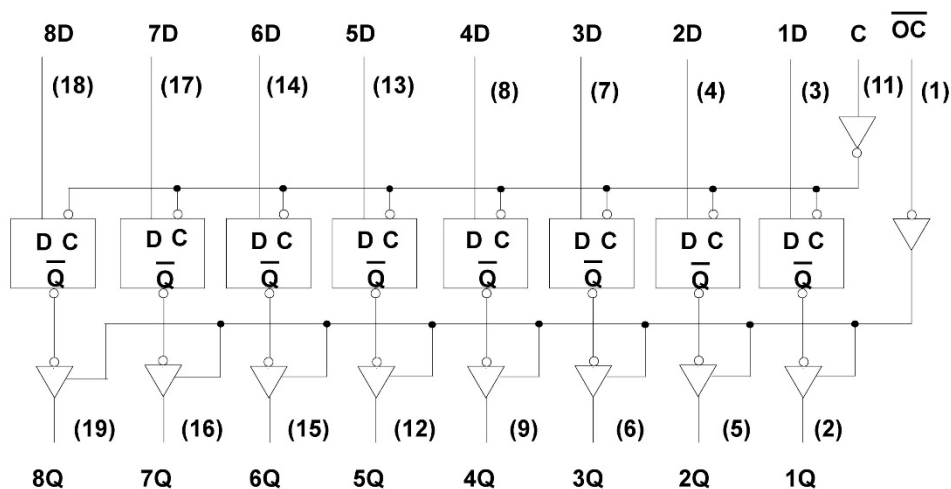
Logic Symbol



Note:

1. Logic symbol in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Logic Diagram



Operational Environment¹

Parameter	Limit	Units
Total Dose	1.0E6	rads (Si)
SEU Threshold ²	80	MeV-cm ² /mg
SEL Threshold	120	MeV-cm ² /mg
Neutron Fluence	1.0E14	n/cm ²

Notes:

1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

Absolute Maximum Ratings

Symbol	Parameter	Limit	Units
V _{DD}	Supply voltage	-0.3 to 7.0	V
V _{I/O}	Voltage any pin	-.3 to V _{DD} +.3	V
T _{STG}	Storage Temperature range	-65 to +150	°C
T _J	Maximum junction temperature	+175	°C
T _{LS}	Lead temperature (soldering 5 seconds)	+300	°C
θ _{JC}	Thermal resistance junction to case	20	°C/W
I _I	DC input current	±10	mA
P _D	Maximum power dissipation	1	W

Note:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	4.5 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to + 125	°C

DC Electrical Characteristics⁷

($V_{DD} = 5.0V \pm 10\%$; $V_{SS} = 0V^6$, $-55^\circ C < T_C < +125^\circ C$); unless otherwise noted, T_C is per the temperature range ordered.

Symbol	Parameter	Condition	MIN	MAX	Unit
V_{IL}	Low-level input voltage ¹ ACTS ACS			0.8 .3 V_{DD}	V
V_{IH}	High-level input voltage ¹ ACTS ACS		.5 V_{DD} .7 V_{DD}		V
I_{IN}	Input leakage current ACTS/ACS	$V_{IN} = V_{DD}$ or V_{SS}	-1	1	μA
V_{OL}	Low-level output voltage ³ ACTS ACS	$I_{OL} = 8.0mA$ $I_{OL} = 100\mu A$		0.40 0.25	V
V_{OH}	High-level output voltage ³ ACTS ACS	$I_{OH} = -8.0mA$ $I_{OH} = -100 \mu A$.7 V_{DD} $V_{DD} - 0.25$		V
I_{OZ}	Three-state output leakage current	$V_O = V_{DD}$ and V_{SS}	-20	20	μA
I_{OS}	Short-circuit output current ^{2,4} ACTS/ACS	$V_O = V_{DD}$ and V_{SS}	-200	200	mA
I_{OL}	Output current ¹⁰ (Sink)	$V_{IN} = V_{DD}$ or V_{SS} $V_{OL} = 0.4V$	8		mA
I_{OH}	Output current ¹⁰ (Source)	$V_{IN} = V_{DD}$ or V_{SS} $V_{OH} = V_{DD} - 0.4V$	-8		mA
P_{total}	Power dissipation ^{2,8,9}	$C_L = 50pF$		1.9	mW/MHz
I_{DDQ}	Quiescent Supply Current	$V_{DD} = 5.5V$		10	μA
ΔI_{DDQ}	Quiescent Supply Current Delta ACTS	For input under test $V_{IN} = V_{DD} - 2.1V$ For all other inputs $V_{IN} = V_{DD}$ or V_{SS} $V_{DD} = 5.5V$		1.6	mA
C_{IN}	Input capacitance ⁵	$f = 1MHz @ 0V$		15	pF
C_{OUT}	Output capacitance ⁵	$f = 1MHz @ 0V$		15	pF

Notes:

- Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(\text{min}) + 20\%$, -0% ; $V_{IL} = V_{IL}(\text{max}) + 0\%$, -50% , as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$.
- Supplied as a design limit but not guaranteed or tested.
- Per MIL-PRF-38535, for current density $\leq 5.0E5$ amps/cm², the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
- Not more than one output may be shorted at a time for maximum duration of one second.
- Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and signal amplitude of 50mV rms maximum.
- Maximum allowable relative shift equals 50mV.
- All specifications valid for radiation dose $\leq 1E6$ rads (Si).
- Power does not include power contribution of any TTL output sink current.
- Power dissipation specified per switching output.
- This value is guaranteed based on characterization data, but not tested.

AC Electrical Characteristics²

($V_{DD} = 5.0V \pm 10\%$; $V_{SS} = 0V^6$, $-55^\circ C < T_C < +125^\circ C$); unless otherwise noted, T_C is per the temperature range ordered.

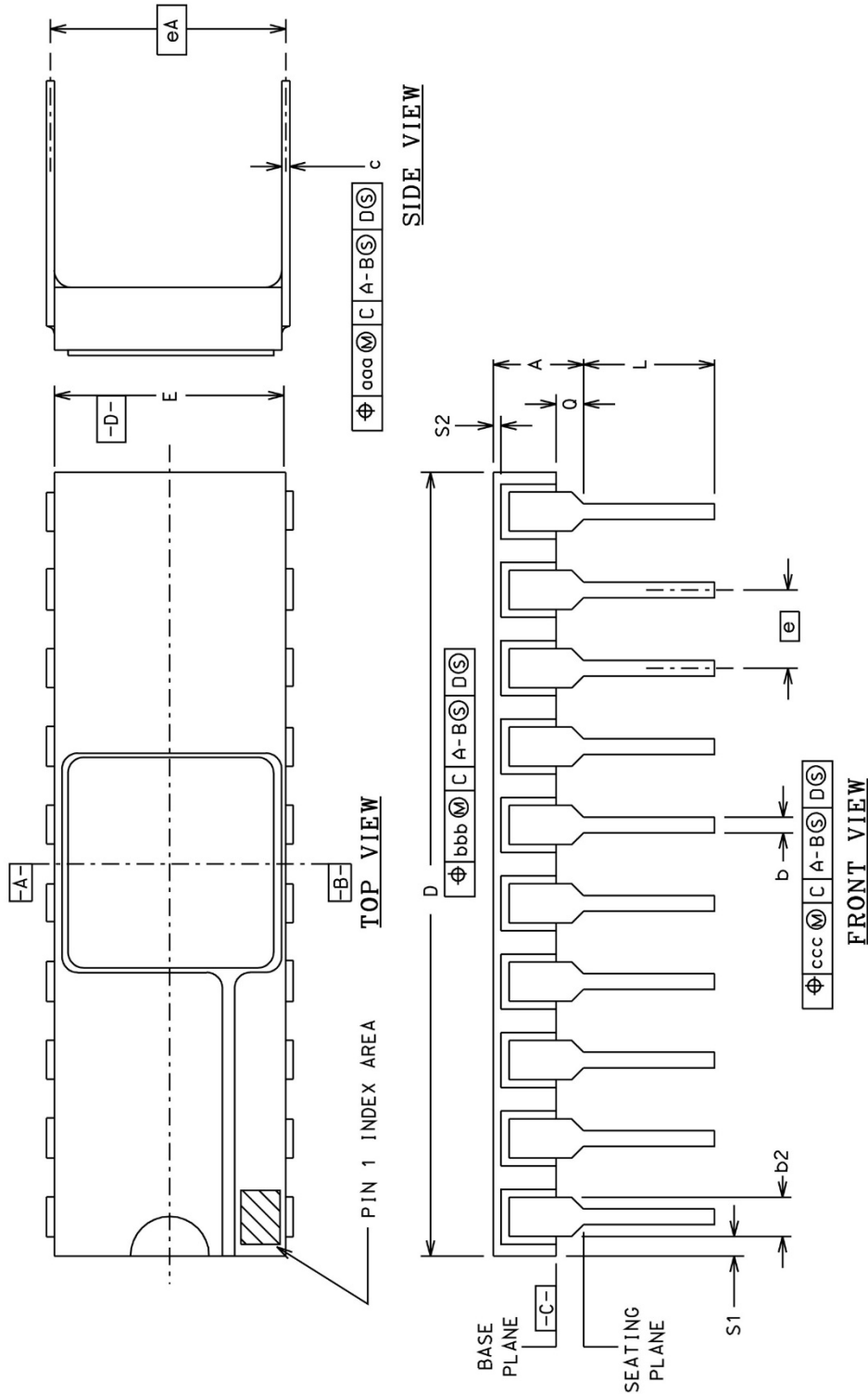
Symbol	Parameter	Minimum	Maximum	Unit
t_{PLH}	Data to Qn	1	14	ns
t_{PHL}	Data to Qn	1	16	ns
t_{PLH}	C \uparrow to Qn	1	16	ns
t_{PHL}	C \uparrow to Qn	1	18	ns
t_{PZL}	\overline{OC} low to Qn	1	14	ns
t_{PZH}	\overline{OC} low to Qn	1	14	ns
t_{PLZ}	\overline{OC} high to Qn three-state	1	14	ns
t_{PHZ}	\overline{OC} high to Qn three-state	1	14	ns
f_{MAX}	Maximum clock frequency		71	MHz
t_{SU}	Data setup time before C \downarrow	5		ns
t_H	Data hold time after C \downarrow	4		ns
t_W	Minimum pulse width C high	7		ns

Notes:

- Maximum allowable relative shift equals 50mV.
- All specifications valid for radiation dose $\leq 1E6$ rads (Si)

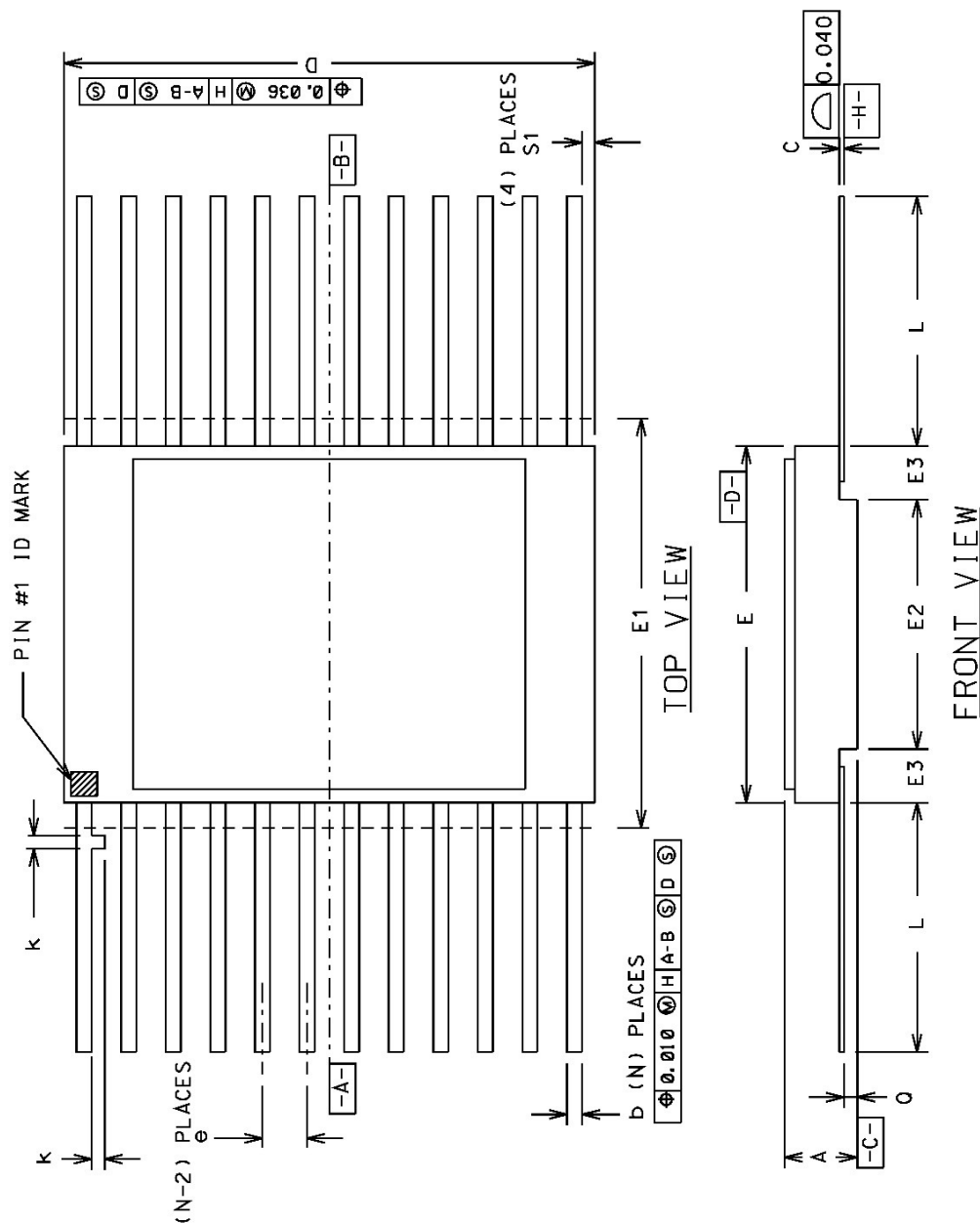
Packaging

Side-Braced Packages



PKG CONF IG	LEAD COUNT	MIL-STD- 1835 DWG CONF C	DIMENSION SYMBOLS														
			A	b	b2	c	D	E	e	eA	L	Q	S1	S2	aaa	bbb	ccc
-01	14	D-1	0.200	0.026	0.065	0.018	0.785	0.310	0.100	0.300	0.200	0.060	-----	-----	0.015	0.030	0.010
			-----	0.014	0.045	0.008	-----	0.220	BSC	BSC	0.125	0.015	0.005	0.005	-----	-----	-----
-02	16	D-2	0.200	0.026	0.065	0.018	0.840	0.310	0.100	0.300	0.200	0.060	-----	-----	0.015	0.030	0.010
			-----	0.014	0.045	0.008	-----	0.220	BSC	BSC	0.125	0.015	0.005	0.005	-----	-----	-----
-03	20	D-8	0.200	0.026	0.065	0.018	1.060	0.310	0.100	0.300	0.200	0.070	-----	-----	0.015	0.030	0.010
			-----	0.014	0.045	0.008	-----	0.220	BSC	BSC	0.125	0.015	0.005	0.005	-----	-----	-----

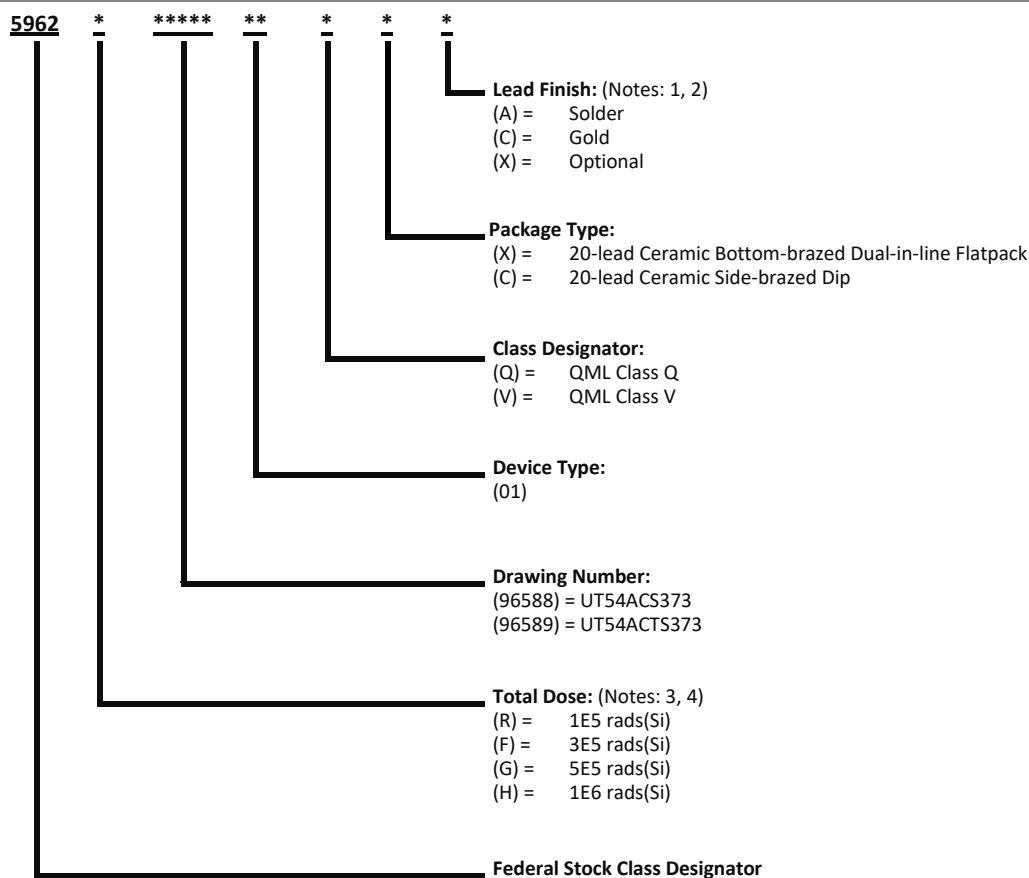
Flatpack Packages



PKG CONFIG	LEAD COUNT	MIL-STD 1835, DWG CONF B	DIMENSION SYMBOLS												
			A	B	C	D	E	E1	E2	E3	ø	k	L	Q	S1
-03	14	F-2A	0.115 0.045	0.022 0.015	0.009 0.004	0.390 -----	0.260 0.235	0.290 -----	----- 0.130	----- 0.030	0.050 BSC	0.015 0.008	0.370 0.270	0.045 0.026	----- 0.005
-04	16	F-5A	0.115 0.045	0.022 0.015	0.009 0.004	0.440 -----	0.285 0.245	0.315 -----	----- 0.130	----- 0.030	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	----- 0.005
-05	20	F-9A	0.115 0.045	0.022 0.015	0.009 0.004	0.540 -----	0.300 0.245	0.330 -----	----- 0.130	----- 0.030	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	----- 0.000

Ordering Information

UT54ACS373/UT54ACTS373 SMD Part Number



Notes:

- Lead finish (A, C, or X) must be specified.
- If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
- Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation Hardening. For prototype inquiries, contact factory.
- Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads (Si) or 1E6 rads (Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads (Si), 3E5 rads (Si), and 5E5 rads (Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

Revision History

Date	Revision #	Author	Change Description	Page #

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet is subject to change . Specifications can be TBD and the part package and pinout are not final .
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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