FRONTGRADE

DATASHEET

UT54ACTS220

Clock and Wait-State Generation Circuit

10/30/2023
Version #:

Features

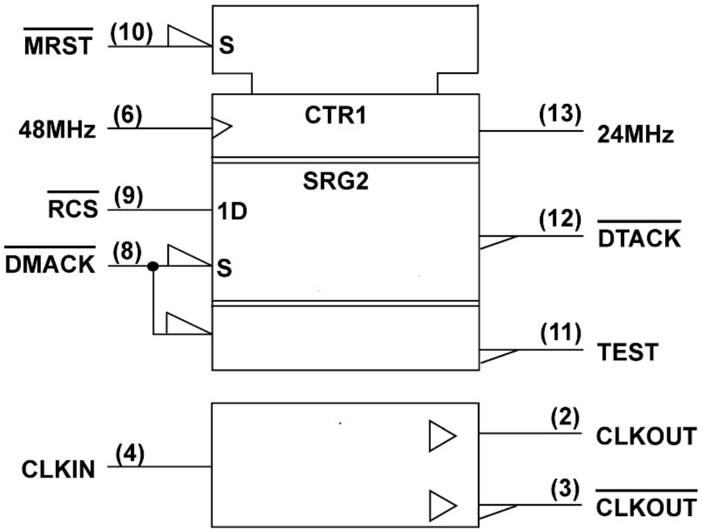
- 1.2µ CMOS
  - > Latchup immune
- High speed
- Low power consumption
- Single 5-volt supply
- Available QML Q or V processes
- Flexible package
  - > 14-pin DIP
  - > 14-lead flatpack
- UT54ACTS220 - SMD 5962-96753

Description

The UT54ACTS220 is designed to be a companion chip to Frontgrade's UT69151 SµMMIT family for the purpose of generating clock and wait-state signals. The device contains a divide by two circuit that accepts TTL input levels and drives CMOS output buffers. The chip accepts a 48MHz clock and generates a 24MHz clock. The 48MHz clock can have a duty cycle that varies by ± 20%. The UT54ACT220 generates a 24MHz clock with a ± 5% duty cycle variation. The wait-state circuit generates a single wait-state by delaying the falling edge of $\overline{\text{DTACK}}$ into the SµMMIT. The clock/timing device generates $\overline{\text{DTACK}}$ from the falling edge of input $\overline{\text{RCS}}$ which is synchronized by the falling edge of 24MHz. The SµMMIT drives inputs $\overline{\text{RCS}}$ and $\overline{\text{DMACK}}$.

The devices are characterized over full military temperature range of -55°C to +125°C.

Logic Symbol



Note:

1. Logic symbol in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pinouts

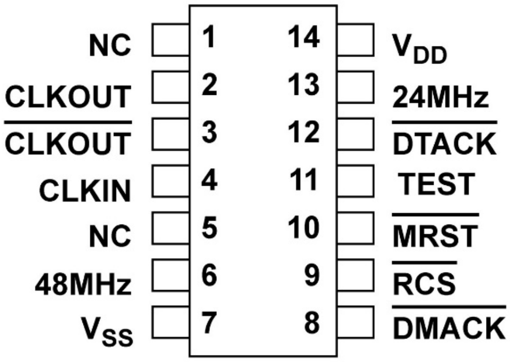


Figure 1: 14-Pin DIP
Top View

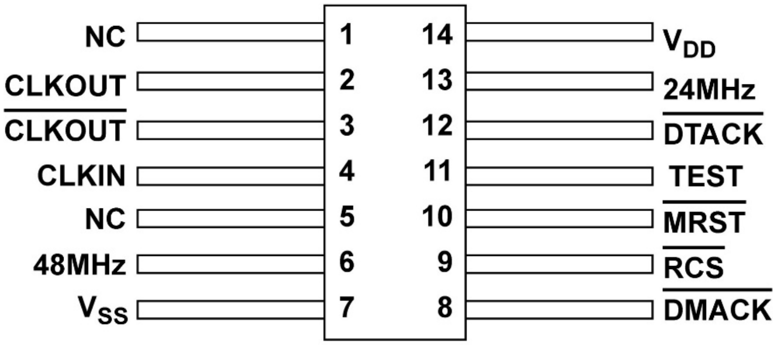


Figure 2: 14-Lead Flatpack
Top View

Pin Description

Pin Number	Pin Name	Description
2	CLKOUT	Buffered version of CLKIN.
3	$\overline{\text{CLKOUT}}$	Inverted version of CLKIN.
4	CLKIN	Clock Input. This signal can be any arbitrary signal that the user wishes to buffer.
6	48MHz	48MHz Clock. The 24MHz clock is created by dividing this signal by two.
8	$\overline{\text{DMACK}}$	DMA Acknowledge. This input is generated by the SµMMIT. When high, this signal will cause $\overline{\text{DTACK}}$ output to be forced high.
9	$\overline{\text{RCS}}$	RAM Chip Select. This input is generated by the SµMMIT.
10	$\overline{\text{MRST}}$	Master Reset. This input can be used to preset 24MHz, $\overline{\text{DTACK}}$ and TEST. For normal operation tie $\overline{\text{MRST}}$ to V_{DD} through a resistor.
11	TEST	Test output signal.
12	$\overline{\text{DTACK}}$	Data Transfer Acknowledge. This signal can be used to drive the $\overline{\text{DTACK}}$ signal of the SµMMIT if the user requires one wait state during the memory transfer.
13	24MHz	24MHz Clock. This output runs at half the frequency of the 48MHz input. The falling edge of 24MHz is the signal that latches the $\overline{\text{DTACK}}$ outputs. 24MHz is forced high whenever $\overline{\text{MRST}}$ is low. Properly loaded, 24MHz will have a 50% duty cycle ± 5%.

Functional Timing: Single SµMMIT Wait-State

For both read and write memory cycles, $\overline{\text{DTACK}}$ is an input to the SµMMIT E and SµMMIT LXE/DXE. A non-wait state memory requires two clock cycles, T1 and T2 of figure 1. For accessing slower memory devices, the UT54ACTS220 holds $\overline{\text{DTACK}}$ to a logical “1”. This results in the stretching of memory cycles by one clock to three clock cycles, TW of figure 1. The SµMMIT E and SµMMIT LXE/DXE samples the $\overline{\text{DTACK}}$ on the rising edge of the 24 MHz clock. If $\overline{\text{DTACK}}$ is not generated before the rising edge of the clock, the SµMMIT E and SµMMIT LXE/DXE extends the memory cycle.

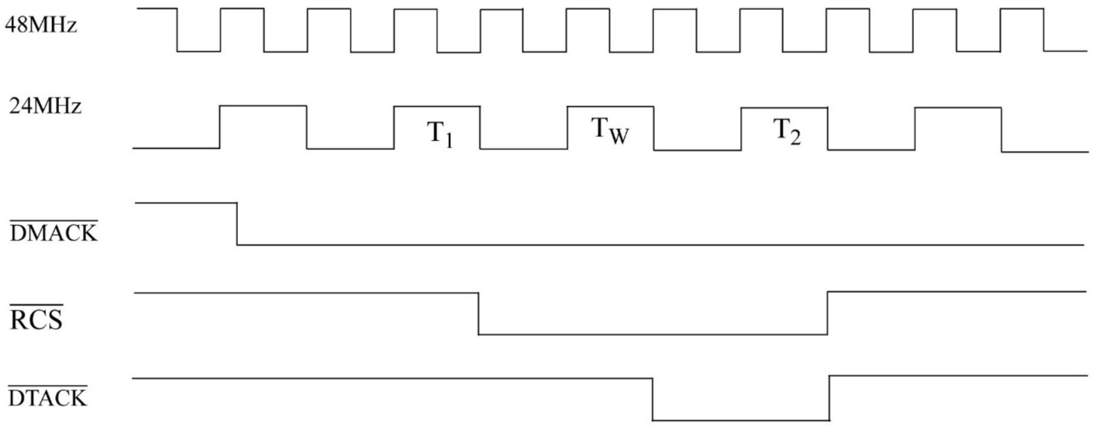
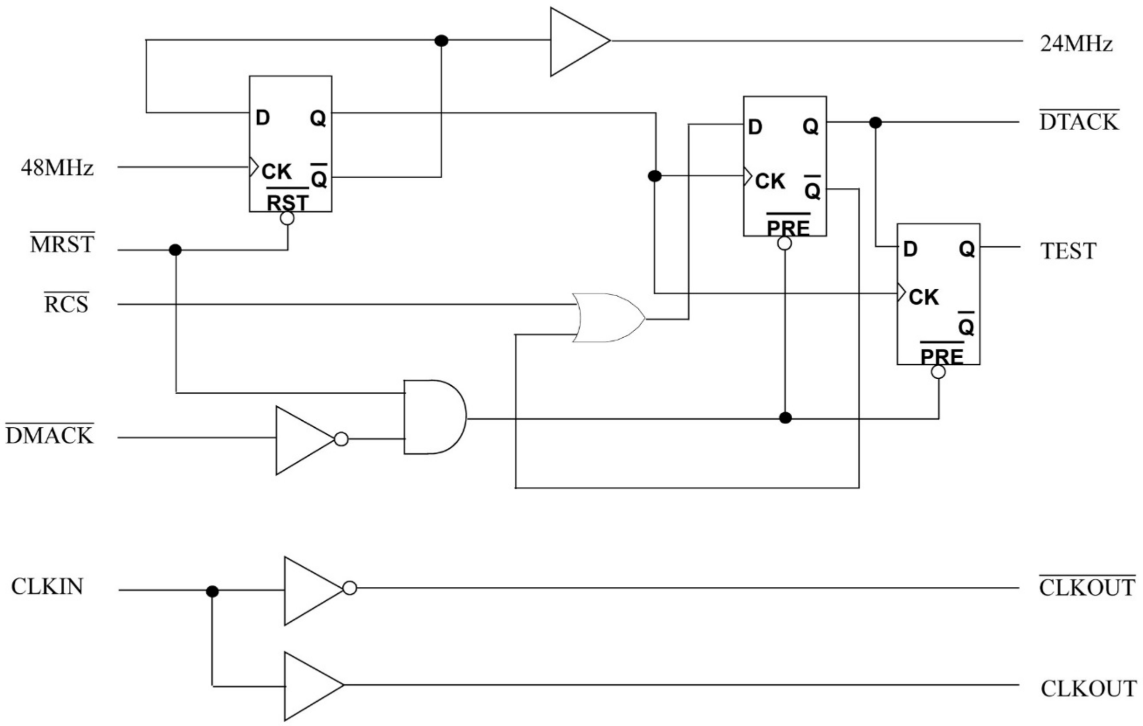


Figure 3: Functional Timing

Logic Diagram



Operational Environment

Parameter	Limit	Units
Total Dose	1.0E6	rads(Si)
SEU Threshold[1]	80	MeV-cm^2/mg
SEL Threshold	>120	MeV-cm^2/mg
Neutron Fluence[2]	1.0E14	n/cm^2

Notes:

1. Device storage elements are immune to SEU affects.
2. Not tested, inherent of CMOS technology.

Absolute Maximum Ratings

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage any pin	-0.3 to V_{DD} +0.3	V
T_{STG}	Storage Temperature range	-65 to +150	℃
T_J	Maximum junction temperature	+175	℃
T_{LS}	Lead temperature (soldering 5 seconds)	+300	℃
Θ_{JC}	Thermal resistance junction to case	20	℃/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation	1	W

Note:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	4.5 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to + 125	℃
48MHz	Duty Cycle	50 ± 20%	MHz

DC Electrical Characteristics[7]

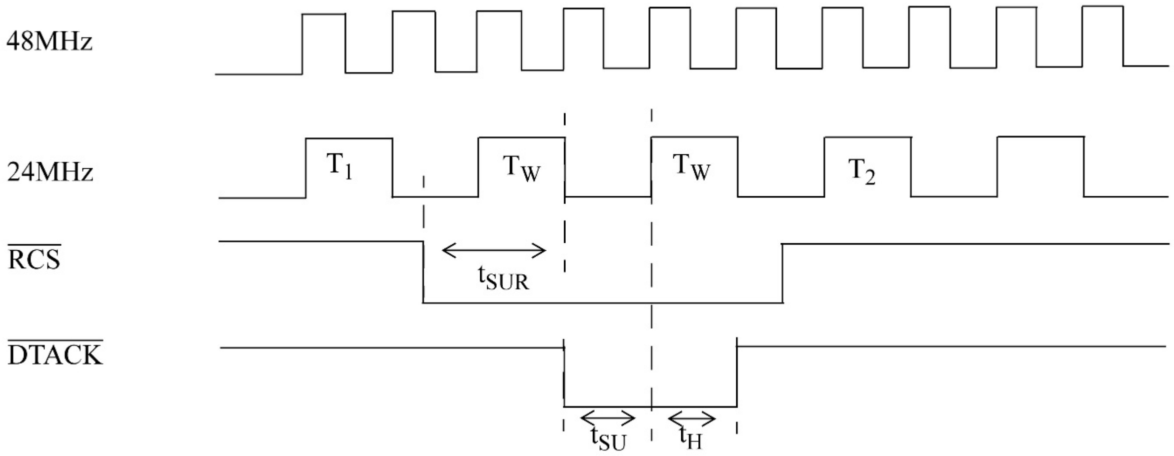
(V_{DD} = 5.0V ±10%; V_{SS} = 0V[6], -55°C < TC < +125°C); Unless otherwise noted, T_C is per the temperature range ordered.

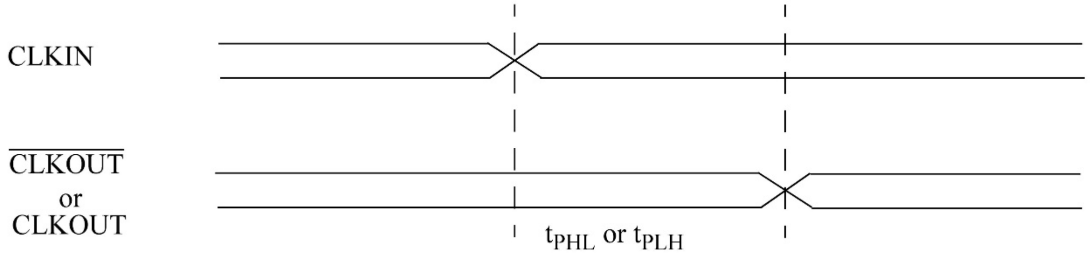
Symbol	Parameter	Condition	MIN	MAX	Unit
V_{IL}	Low-level input voltage[1] TTL			0.8	V
V_{IH}	High-level input voltage[1] TTL		2.25		V
I_{IN}	Input leakage current TTL	V_{DD} = 5.5V V_{IN} = V_{DD} or V_{SS}	-1	1	µA
V_{OL1}	Low-level output voltage[3] Except CLKOUT/$\overline{\text{CLKOUT}}$	I_{OL} = 8.0mA V_{DD} = 4.5V I_{OL} = 100µA		0.4 0.25	V
V_{OH1}	High-level output voltage[3] Except CLKOUT/$\overline{\text{CLKOUT}}$	I_{OH} = -8.0mA, V_{DD} = 4.5V	3.15		V
V_{OL2}	CLKOUT/$\overline{\text{CLKOUT}}$ Low-level output voltage[3]	IOL = 100µA		0.25	V
V_{OH2}	CLKOUT/$\overline{\text{CLKOUT}}$ High-level output voltage[3]	I_{OH} = -100µA	4.25		V
I_{OS}	Short-circuit output current[2,4]	V_O = V_{DD} and V_{SS} V_{DD} = 5.5V		+300	mA
I_{OL1}	Output current[10] (Sink), Except CLKOUT/$\overline{\text{CLKOUT}}$	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V	8		mA
I_{OH1}	Output current[10] (Source), Except CLKOUT/$\overline{\text{CLKOUT}}$	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD} - 0.4V	-8		mA
I_{OL2}	CLKOUT/$\overline{\text{CLKOUT}}$ Output current[10] (Sink)	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V	12		mA
I_{OH2}	CLKOUT/$\overline{\text{CLKOUT}}$ Output current[10] (Source)	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD} - 0.4V	-12		mA
I_{IH}	Input current high	V_{IN} = V_{DD} or V_{SS} V_{IN} = 5.5V		+1.0	µA
I_{IL}	Input current low	V_{IN} = V_{DD} or V_{SS} V_{IN} = V_{SS}		-1.0	µA
P_{total}	Power dissipation[2,8,9]	C_L = 50pF		1.0	mW/MHz
I_{DDQ}	Quiescent Supply Current	V_{DD} = 5.5V V_{IN} = V_{DD} or V_{SS}		10	µA
ΔI_{DDQ}	Quiescent Supply Current Delta	For input under test V_{IN} = V_{DD} - 2.1V For all other inputs V_{IN} = V_{DD} or V_{SS} V_{DD} = 5.5V		1.6	mA
C_{IN}	Input capacitance[5]	f = 1MHz @ 0V		15	pF
C_{OUT}	Output capacitance[5]	f = 1MHz @ 0V		15	pF

Notes:

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: V_{IH} = V_{IH}(min) + 20%, - 0%; V_{IL} = V_{IL}(max) + 0%, -50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL}(max).
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density ≤5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF/MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6. Maximum allowable relative shift equals 50mV.
7. All specifications valid for radiation dose ≤ 1E6 rads(Si).
8. Power does not include power contribution of any TTL output sink current.
9. Power dissipation specified per switching output.
10. This value is guaranteed based on characterization data, but not tested.

AC Electrical Diagram





AC Electrical Characteristics[2]

(V_{DD} = 5.0V ±10%; V_{SS} = 0V[1], -55°C < T_C < +125°C); Unless otherwise noted, T_C is per the temperature range ordered.

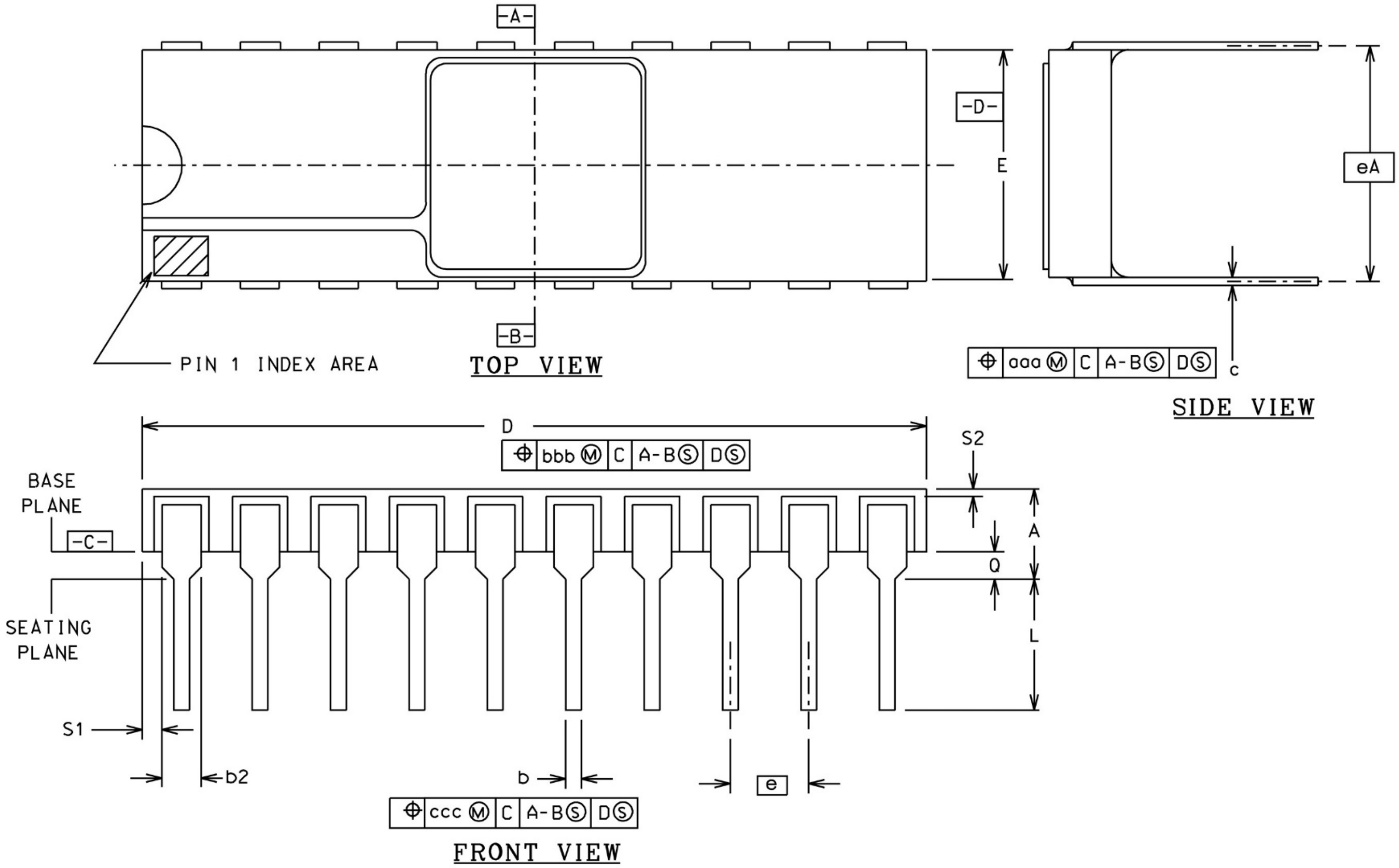
Symbol	Parameter	Minimum	Maximum	Units
t_{PHL}^{1}	48MHz ↑ to 24MHz ↓	0	15	ns
t_{PLH}^{1}	48MHz ↑ to 24MHz ↑	0	15	ns
t_{PHL}^{2}	24MHz ↓ to $\overline{\text{DTACK}}$ ↓	0	7	ns
t_{PLH}^{2}	24MHz ↓ to $\overline{\text{DTACK}}$ ↑	0	6	ns
t_{PLH}^{3}	$\overline{\text{DMACK}}$ ↑ to $\overline{\text{DTACK}}$ ↑	3	16	ns
t_{PLH}^{4}	$\overline{\text{MRST}}$ ↓ to 24MHz ↑, $\overline{\text{DTACK}}$ ↑	3	16	ns
t_{PHL}^{5}	CLKIN ↓ to CLKOUT ↓	0	11	ns
t_{PLH}^{5}	CLKIN ↑ to CLKOUT ↑	0	11	ns
t_{PHL}^{6}	CLKIN ↑ to $\overline{\text{CLKOUT}}$ ↓	0	11	ns
t_{PLH}^{6}	CLKIN ↓ to $\overline{\text{CLKOUT}}$ ↑	0	11	ns
t_{SU}^{3}	$\overline{\text{DTACK}}$ ↓ to 24MHz ↑, setup time	12		ns
t_{H}^{3}	24MHz ↑ to $\overline{\text{DTACK}}$ ↑, hold time	20		ns
t_{SUR}	Setup time from $\overline{\text{RCS}}$ ↓ to 24MHz ↓	7		ns
t_{WM}	$\overline{\text{MRST}}$ pulse width low	5		ns
t_{WC}	CLKIN pulse width	12		ns
f_{MAX}	Maximum CLKIN frequency		40	MHz

Notes:

1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose ≤ 1E6 rads(Si).
3. Guaranteed by design but not tested.

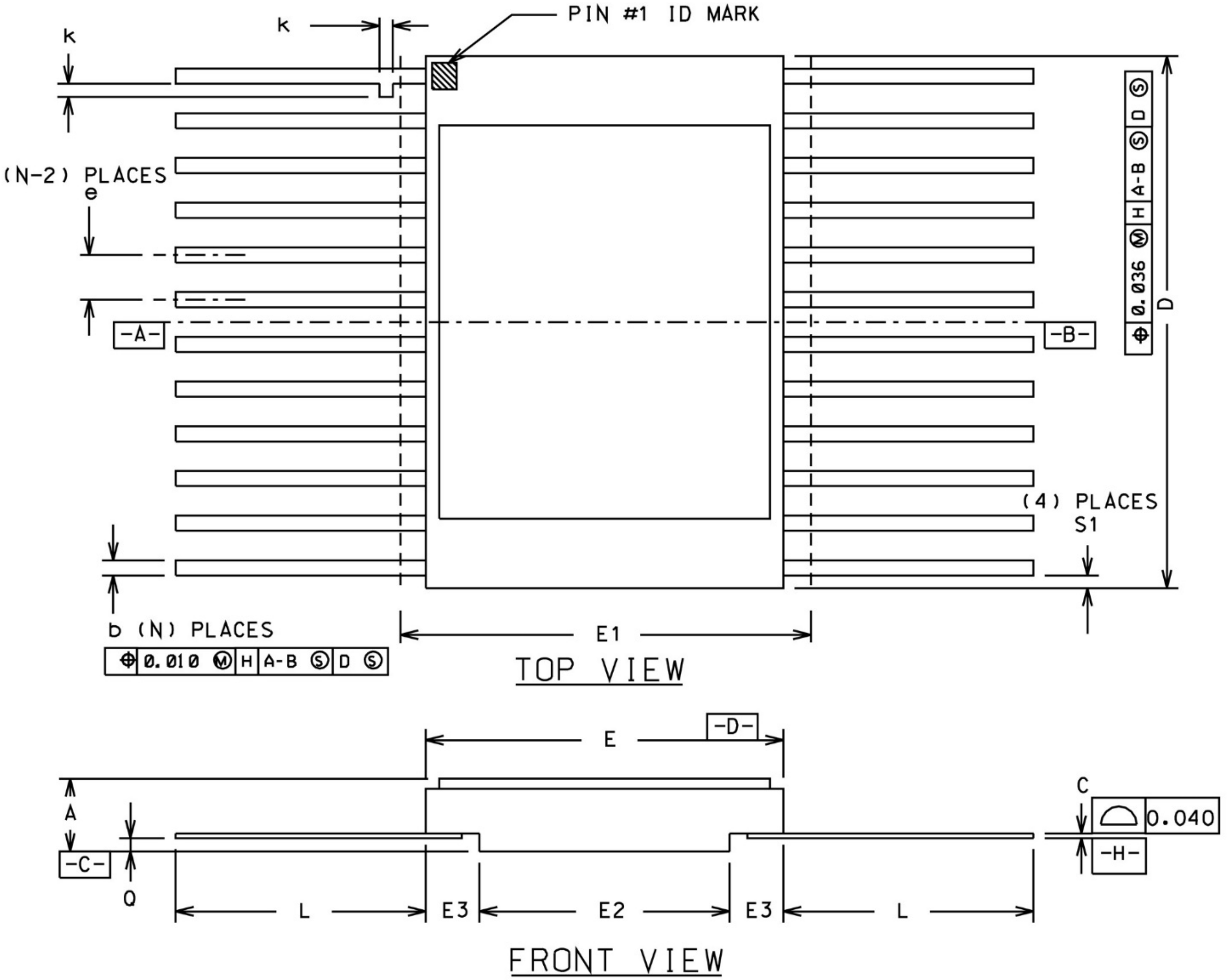
Packaging

Side-Brazed Packages



PKG CONFIG	LEAD COUNT	MIL-STD-1835 DWG CONF C	DIMENSION SYMBOLS														
			A	b	b2	c	D	E	e	eA	L	Q	S1	S2	aaa	bbb	ccc
-01	14	D-1	0.200 -----	0.026 0.014	0.065 0.045	0.018 0.008	0.785 -----	0.310 0.220	0.100 BSC	0.300 BSC	0.200 0.125	0.060 0.015	----- 0.005	----- 0.005	0.015 -----	0.030 -----	0.010 -----
-02	16	D-2	0.200 -----	0.026 0.014	0.065 0.045	0.018 0.008	0.840 -----	0.310 0.220	0.100 BSC	0.300 BSC	0.200 0.125	0.060 0.015	----- 0.005	----- 0.005	0.015 -----	0.030 -----	0.010 -----
-03	20	D-8	0.200 -----	0.026 0.014	0.065 0.045	0.018 0.008	1.060 -----	0.310 0.220	0.100 BSC	0.300 BSC	0.200 0.125	0.070 0.015	----- 0.005	----- 0.005	0.015 -----	0.030 -----	0.010 -----

Flatpack Packages



PKG CONFIG	LEAD COUNT	MIL-STD 1835 DWG CONF B	DIMENSION SYMBOLS												
			A	b	c	D	E	E1	E2	E3	e	k	L	Q	S1
-03	14	F-2A	0.115 0.045	0.022 0.015	0.009 0.004	0.390 -----	0.260 0.235	0.290 -----	----- 0.130	----- 0.030	0.050 BSC	0.015 0.008	0.370 0.270	0.045 0.026	----- 0.005
-04	16	F-5A	0.115 0.045	0.022 0.015	0.009 0.004	0.440 -----	0.285 0.245	0.315 -----	----- 0.130	----- 0.030	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	----- 0.005
-05	20	F-9A	0.115 0.045	0.022 0.015	0.009 0.004	0.540 -----	0.300 0.245	0.330 -----	----- 0.130	----- 0.030	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	----- 0.000

Ordering Information

UT54ACTS220 SMD Part Number Ordering Information

5962 * ***** ** * * *

Lead Finish: (Notes: 1, 2)
(A) = Solder
(C) = Gold
(X) = Optional

Package Type:
(X) = 14-lead Ceramic Bottom-brazed Dual-in-line Flatpack
(C) = 14-lead Ceramic Side-brazed Dip

Class Designator:
(Q) = QML Class Q
(V) = QML Class V

Device Type:
(01)

Drawing Number:
(96753) = UT54ACTS220

Total Dose: (Notes: 3, 4)
(R) = 1E5 rads(Si)
(F) = 3E5 rads(Si)
(G) = 5E5 rads(Si)
(H) = 1E6 rads(Si)

Federal Stock Class Designator

Notes:

1. Lead finish (A, C or X) must be specified.
2. If an “X” is specified when ordering, part marking will match the lead finish and will be either “A” (solder) or “C” (gold).
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
4. Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) or 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

Revision History

Date	Revision #	Author	Change Description	Page #

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.