FRONTGRADE

DATASHEET

UT01VS50D

Voltage Supervisor

8/1/2022

Version #: 1.0

Features

- 4.75V to 5.5V Operating voltage range
- Power supply (V_{DD}) monitor set by the internal voltage reference at 4.65V
- Precision Input Voltage Monitor using an internal 1.25V voltage reference
- Watchdog Timer Circuit monitoring activity on WDI input
  - Nominal timeout 1.6s
- $\overline{\text{RESET\_OD}}$ output responding to the V_{DD} monitor and the manual reset input $\overline{\text{MR}}$
  - Nominal $\overline{\text{RESET\_OD}}$ pulse width 200ms
- $\overline{\text{RESET\_OD}}$ level valid for V_{DD}>=1.2V
- Operating Temperature Range -55℃ to +125℃
- Low Power, Typical 400uA
- Operational environment:
  - Total dose: 300 krad(Si)
  - SEL Immune: ≤110 MeV-cm^2/mg @125℃
  - SET Immune: ≤80 MeV-cm^2/mg
- Packaging options:
  - 8-lead dual-in-line flatpack
- Standard Microelectronics Drawing (SMD) 5962-11213
  - QML Q and V

Introduction

The UT01VS50D's function is to monitor vital supply and signal voltages in microprocessor systems. It provides for safe reset during power up, power down and brownout conditions by using an internal precision voltage reference.

The UT01VS50D monitors activity at an independent watchdog input by employing an internal timer and a watchdog output that goes low if the input is not toggled within 1.6s. It provides for precision voltage threshold detection on an independent voltage input which could be used for battery or supply-low monitoring of a supply voltage other than V_{DD}.

The UT01VS50D includes an active low manual reset with an open drain output.

Applications

- Voltage Supervisor function for various systems including microprocessors, microcontrollers, DSPs and FPGAs
- Critical battery and power supply monitoring
- Replacement of older discrete solutions to improve reliability, accuracy and reduce complexity of the systems

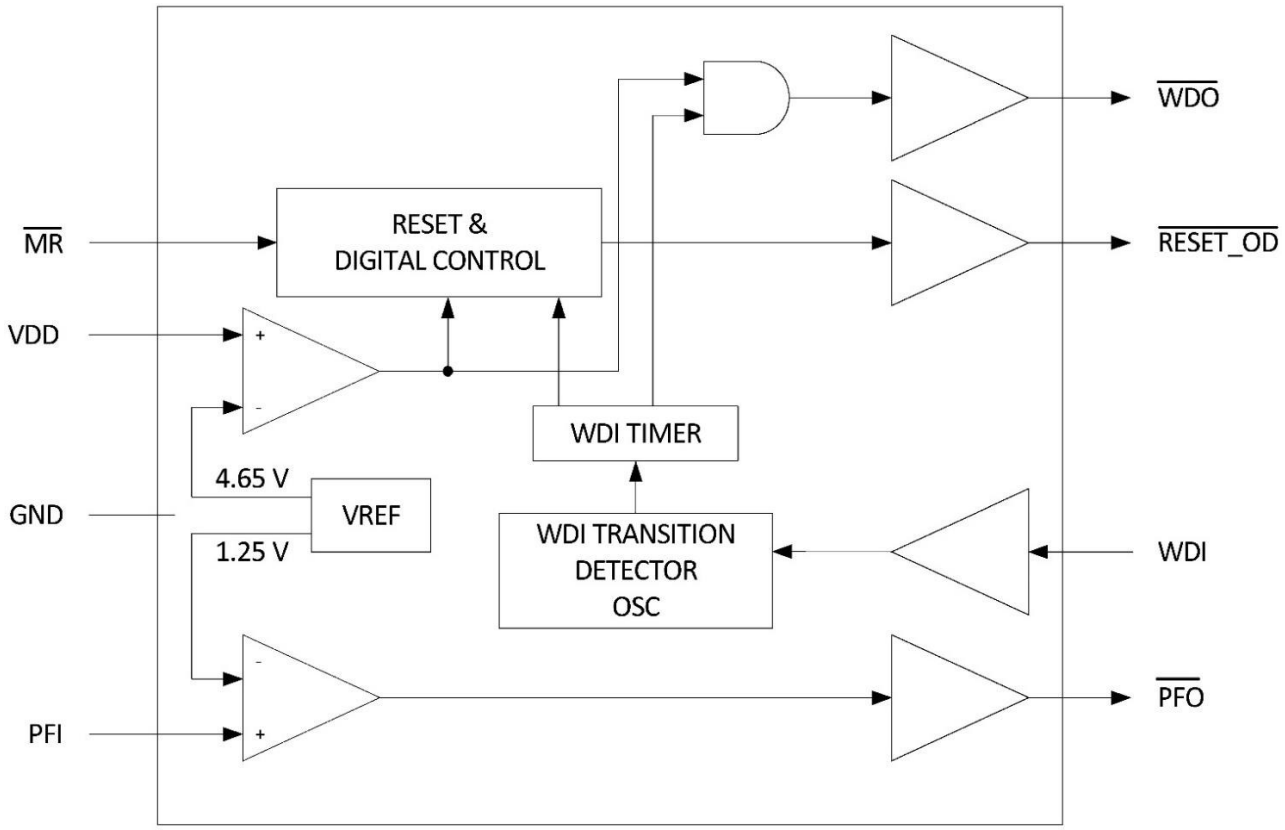


Figure 1. UT01VS50D Functional Block Diagram

Pin Descriptions

Number	Pins	Type	Description
1	$\overline{MR}$	Digital Input TTL/CMOS compatible	**Manual Reset Input with an internal pull-up.** Active low. $\overline{MR}$ low forces the reset output $\overline{RESET\_OD}$ low. Required minimum $\overline{MR}$ pulse width is 150ns. $\overline{RESET\_OD}$ is held low for duration of the reset timer.
2	VDD	Supply	**Power supply.** Operating voltage range is 4.75V to 5.5V. V_{DD} level is monitored internally by a dedicated comparator circuit, which employs an internal bandgap voltage reference nominally equal to 1.25V. Every time V_{DD} falls below the threshold voltage, nominally 4.65V, $\overline{RESET\_OD}$ and $\overline{WDO}$ outputs are forced low. (See $\overline{WDO}$ and $\overline{RESET\_OD}$ descriptions.) (Figure 4.)
3	GND	Supply	**ASIC Ground.** This pin should be tied to ground and establishes the reference for voltage detection.
4	PFI	Analog Input	**Threshold detector input.** Voltage on this input is fed directly to an internal comparator where it is compared to the bandgap voltage reference of 1.25vV It can be used for detection of low battery or power failure of voltage supplies other than V_{DD}. When voltage at PFI input drops below its threshold value of 1.25V. $\overline{PFO}$ output is forced low, otherwise, stays high.
5	$\overline{PFO}$	Digital Output	**Threshold detector output.** Active low. It responds directly to PFI input. If PFI voltage is below the bandgap reference voltage, $\overline{PFO}$ is low. If PFI is above the reference voltage, $\overline{PFO}$ output is high.
6	WDI	Digital Input	**Watchdog timer input pin.** This pin is typically used to monitor microprocessor activity. It can assume three states: low, high and float. If WDI is floating or connected to a high impedance three state buffer, the watchdog timer is not active, and the corresponding watchdog output $\overline{WDO}$ is high. Watchdog timer is also not active any time $\overline{RESET\_OD}$ is low. Providing that $\overline{RESET\_OD}$ is not asserted, any change of state at WDI that is longer than 50ns will start the timer, or restart it, if the timer is already running (Figure 3.). If there is no activity within the timeout period, nominally 1.6sec, the timer will stop running and $\overline{WDO}$ output will go low (Figure 3).

Number	Pins	Type	Description
7	$\overline{\text{RESET\_OD}}$	Open Drain Digital Output	**Reset output.** Active low open drain output. This pin is pulled up with a resistor consistent with the sink and voltage current as specified in the electrical characteristics table. This output responds to both: V_{DD} monitoring circuits and the manual reset input $\overline{\text{MR}}$. On power up, $\overline{\text{RESET\_OD}}$ is guaranteed to be logic low for all V_{DD} values from 1.2V up to the reset threshold, nominally 4.65V. Once this threshold is reached, an internal $\overline{\text{RESET\_OD}}$ timer is activated. During the countdown $\overline{\text{RESET\_OD}}$ output is kept low. It is raised high upon completion of countdown, typically after 200ms. If a brown out condition occurs during the reset timer countdown, the reset timer would be reset and another countdown would start after V_{DD} levels were restored above the reset threshold. On power down, when V_{DD} falls below the threshold voltage, $\overline{\text{RESET\_OD}}$ goes low and is guaranteed to stay low until VDD drops below 1.2V. If MR is asserted low, $\overline{\text{RESET\_OD}}$ is forced low and the reset timer is kept reset. When MR is released high, the timer is activated and $\overline{\text{RESET\_OD}}$ is kept low until completion of the reset timeout, when it is raised high.
8	$\overline{\text{WDO}}$	Digital Output	**Watchdog output.** Active low. This pin is usually connected to a non- maskable interrupt input of a microprocessor. On power up, $\overline{\text{WDO}}$ responds to V_{DD} monitoring circuitry. It stays low until the reset threshold, 4.65V nominally, is reached. At that point, $\overline{\text{WDO}}$ is raised high. The internal watchdog timer is activated after $\overline{\text{RESET\_OD}}$ is released. If there is no activity on WDI input, $\overline{\text{WDO}}$ goes low after the watchdog timer times out, which is typically after 1.6sec. Any activity on WDI will force $\overline{\text{WDO}}$ output to go high and the watchdog timer will be activated. If WDI is floating or connected to a high impedance buffer output, the timer is kept in a reset state and $\overline{\text{WDO}}$ stays high. When VDD drops below 4.65V, $\overline{\text{WDO}}$ goes low regardless of whether the watchdog timer has timed out or not. $\overline{\text{RESET\_OD}}$ goes low simultaneously which prevents an interrupt. If WDI input is left unconnected, $\overline{\text{WDO}}$ can be used as a low line output. Since a floating WDI disables the internal watchdog timer, $\overline{\text{WDO}}$ goes low when V_{DD} drops below 4.65V, thus, functioning as a low line output. (Figure 4.)

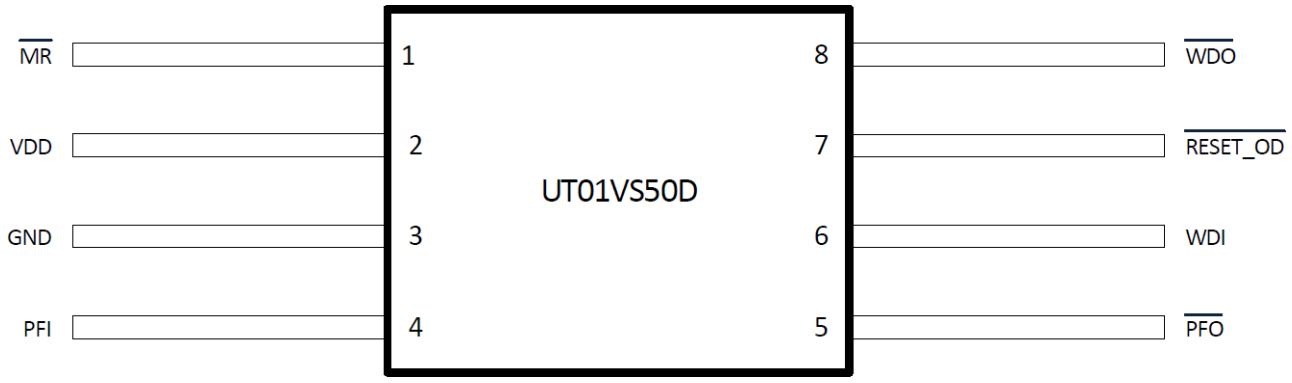


Figure 2. UT01VS50D Pin Configuration

Operational Environment

Parameter	Limit	Units
Total Ionizing Dose (TID)	300	Krad(Si)
Single Event Latchup Immune (SEL)	≤110	MeV-cm²/mg
Single Event Transient Immune (SET)	≤80	MeV-cm²/mg

Absolute Maximum Ratings[1]

(Referenced to GND)

Symbol	Parameter	Limits	Units
V_{DD}	Voltage supply	7.2	V
T_J	Maximum junction temperature	175	℃
T	Storage temperature	-65 to +150	℃
P_D	Power dissipation	2.5	W
V_{IN}	Input voltages	-0.3V to (V_{DD}+0.3V)	V
T_{IEAD}	Lead Temperature (soldering, 10 seconds)	+300	℃
ΘJC	Thermal resistance, junction-to-case	15	℃/W
V_{ESD}	ESD_{HBM}	1000	V

Note:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Limits	Units
V_{DD}	Positive supply voltage	4.75 to 5.5	V
T_C	Case temperature range	-55 to +125	℃
GND	Negative supply voltage	0.0	V

Electrical Characteristics[1,2]

(V_{DD} = 4.75V to 5.5V: -55°C ≤ T_C ≤+125°C)

Symbol	Parameter	Condition	MIN	MAX	Unit
Power Supply					
I_{DD}	V_{DD} supply current	V_{DD}=5.5V		530	µA
Digital Inputs and Outputs ($\overline{MR}$, $\overline{RESET\_OD}$, WDI, $\overline{WDO}$, $\overline{PFO}$)					
V_{IL}	Digital input low	V_{DD}=4.75V		0.8	V
V_{IH}	Digital input high	V_{DD}=5.5V	3.5		V
VIL_$\overline{MR}$	Manual reset input low	V_{DD}=4.75V		0.8	V
VIL_$\overline{MR}$	Manual reset input high	V_{DD}=5.5V	2.0		V
VOL	Digital output low	V_{DD}=4.75V, IOL =1.2mA $\overline{WDO}$		0.4	V
VOL	Digital output low	V_{DD}=4.75V, I_{SINK}=3.2mA $\overline{RESET\_OD}$, $\overline{PFO}$		0.4	V
Timing and Threshold Voltages					
$t_{RST-ASSRT}$[3]	V_{DD} falling reset assertion	V_{DD} < 4.5V	0.2	0.8	µs
t_{RS}	Reset pulse width	V_{DD} = 4.75V	140	280	ms
t_{WD}	Watchdog time-out period	V_{DD} = 5.5V	1.0	2.25	s
t_{WP}	Watchdog input pulse width	V_{DD} = 4.75V, V_{IL} = 0.4V, V_{IH} = 0.8XV_{DD}	50		ns
V_{RT}	Reset threshold voltage		4.5	4.75	V
V_{RTHYS}	Reset threshold voltage hysteresis		20		mV
$t_{\overline{MR}}$	Manual reset ($\overline{MR}$) input pulse width	V_{DD} = 4.75V	150		ns
t_{MD}	Manual reset ($\overline{MR}$) to reset out delay	V_{DD} = 4.75V		100	ns
Analog Input PFI					
I_{PFI}[3]	Threshold detector input (PFI) current	V_{DD}=5.5V	-20	20	nA
V_{PFI}	Threshold detector input (PFI) threshold voltage	V_{DD}=5.0V	1.20	1.30	V
$I_{\overline{MR}}$	Manual reset pull-up current	V_{DD}=5.5V, $\overline{MR}$ =0.0V	-500	-100	µA
I_{WDI}	Watchdog input (WDI) current	WDI pin = V_{DD}= 5.5V WDI pin = 0V; V_{DD}= 5.5V	-35	35	µA
t_{RPFI}	PFI rising threshold crossing to PFO delay			15	µs
t_{FPFI}	PFI falling threshold crossing to PFO delay			35	µs
I_{LEAK}	Reset output leakage current	V_{OUT} = V_{DD}		1	µA

Notes:

1. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance at 25°C per MIL-STD- 883 Method 1019, Condition A, up to the maximum TID level procured (see ordering information).
2. Unless otherwise specified, VDD = 4.75V to 5.5V, -55°C ≤ TC ≤ +125°C. $\overline{RESET\_OD}$ is the only parameter operable within 1.2V and the minimum recommended operating supply voltage.
3. Guaranteed by design, but not tested.

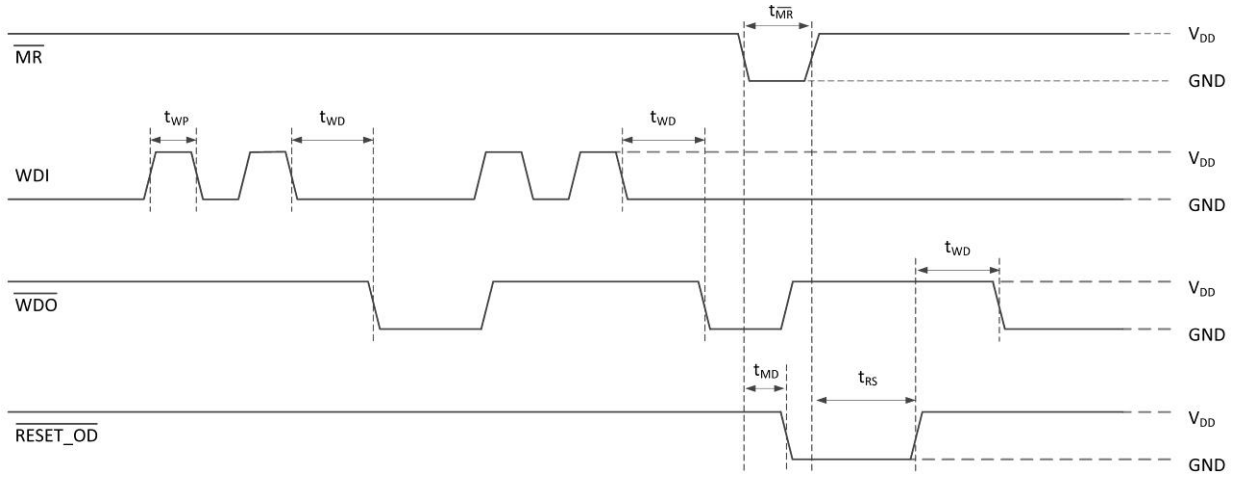


Figure 3. WDI and $\overline{WDO}$ timing waveforms. Reset externally triggered by $\overline{MR}$

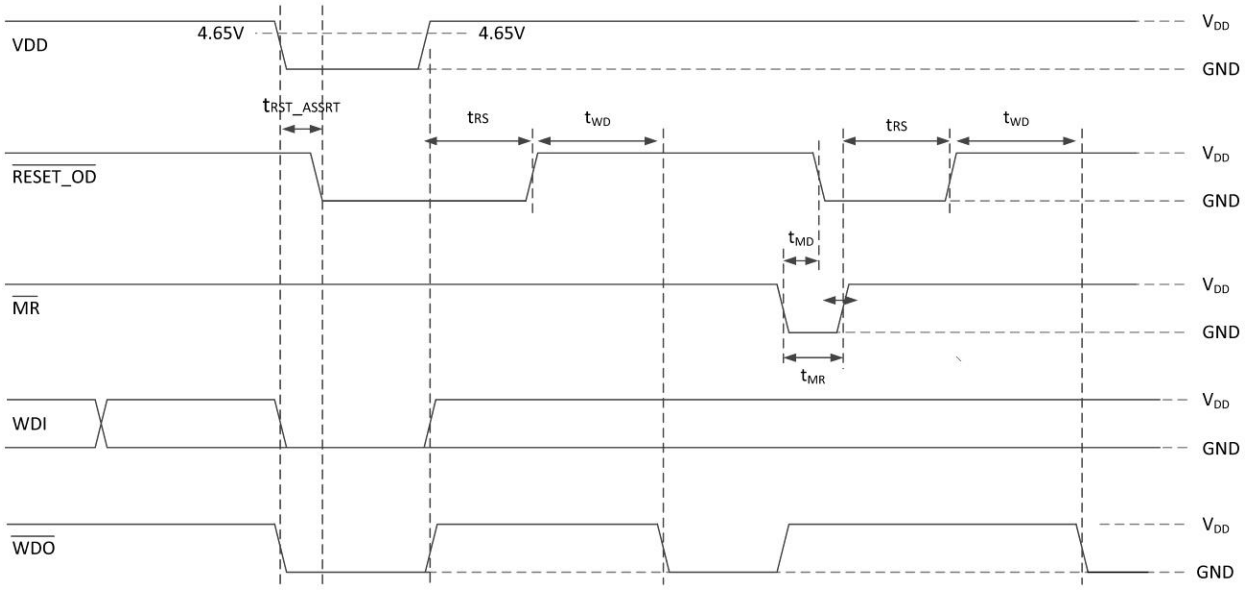


Figure 4. $\overline{RESET\_OD}$ and $\overline{WDO}$ are driven low for V_{DD} <4.65 volts. $\overline{WDO}$ is driven high when $\overline{MR}$ is low

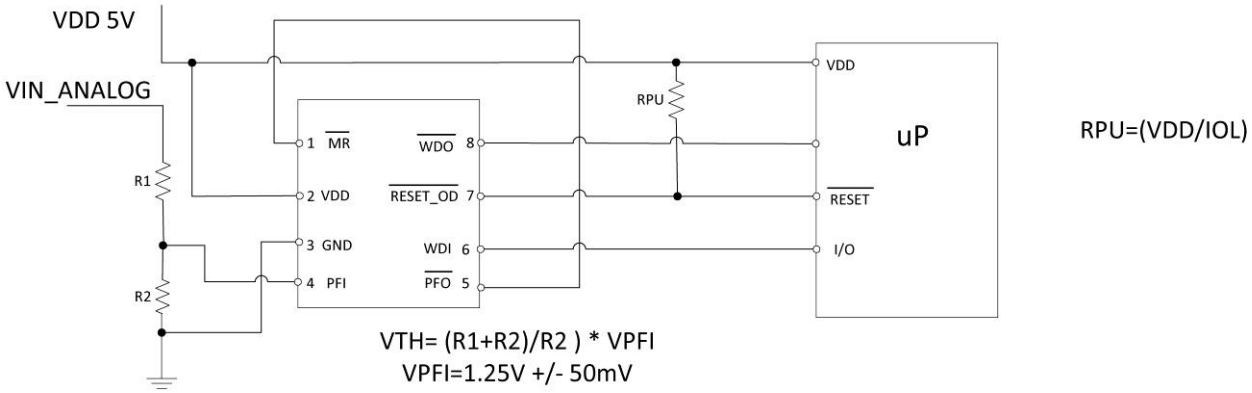


Figure 5. UT01VS50D Under Voltage Monitor and Detection

Shown in Figure 5 is an application for monitoring the under voltage of a power supply connected to a microprocessor or ASIC. If the analog voltage monitored falls below the desired threshold value, the $\overline{\text{PFO}}$ output connected to the $\overline{\text{MR}}$ input will transition low causing the $\overline{\text{RESET\_OD}}$ output to be asserted low indicating an under voltage condition.

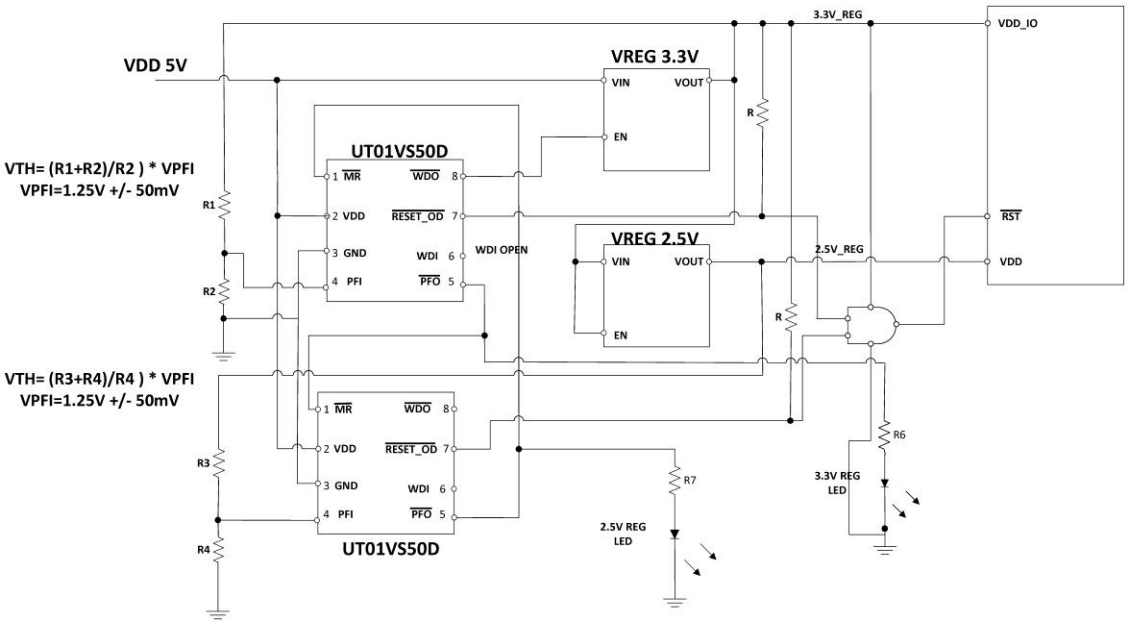


Figure 6. Under Voltage Monitoring and sequencing of 3.3V and 2.5V Power Supplies

Shown in Figure 6 are two Voltage Supervisors configured to monitor both the 3.3V and 2.5V power supplies of a system. The 3.3V regulated supply is monitored by the PFI pin of the top Voltage Supervisor, while the 2.5 V regulated supply is monitored by the PFI pin of the bottom Voltage Supervisor. The cross coupled connection of $\overline{\text{PFO}}$ to $\overline{\text{MR}}$ assures that $\overline{\text{RESET\_OD}}$ will be asserted when a brown out occurs on either the 3.3V or 2.5V regulated supplies.

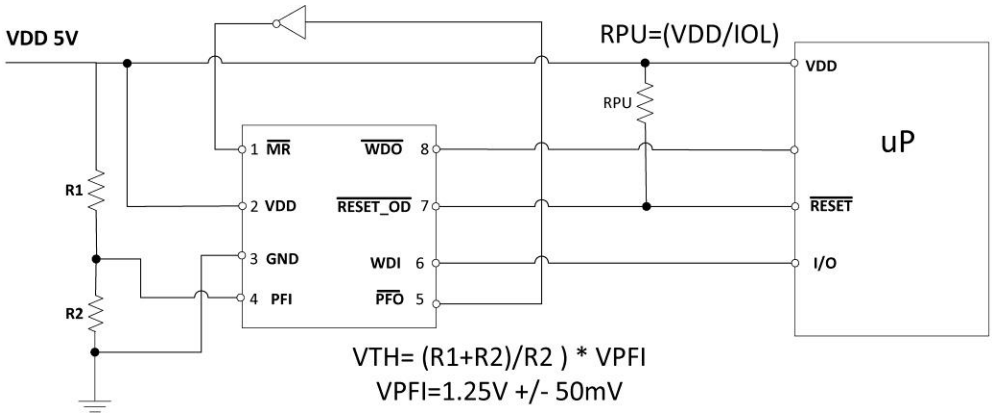


Figure 7. UT01VS50D Over Voltage Power Supply Monitoring and Reset

Shown in Figure 7 is an application to monitor and detect power supply over voltage through the use of the PFI pin. When the voltage at the PFI input, (VTH) exceeds VREF, (1.2 to 1.3V) the $\overline{\text{PFD}}$ output transitions from low to high causing the $\overline{\text{MR}}$ output to transition from high to low. This asserts a $\overline{\text{RESET\_OD}}$ indicating the voltage being monitored has exceeded the over voltage monitor limit.

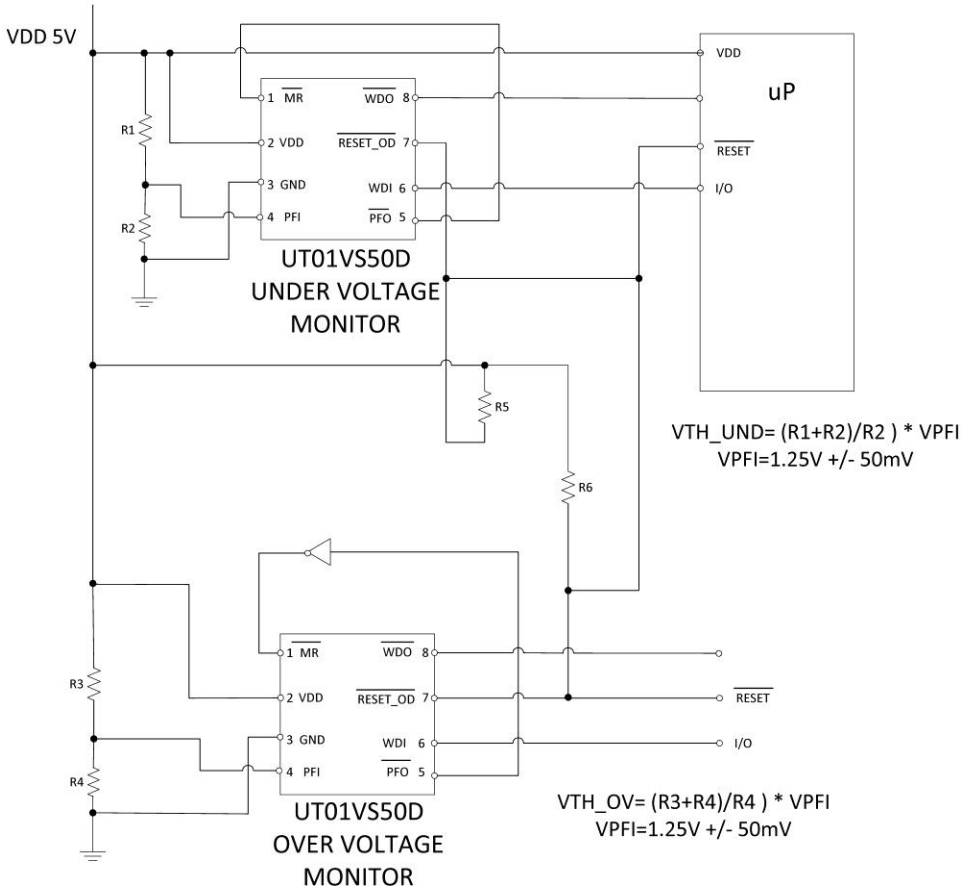


Figure 8. UT01VS50D Over Voltage Power Supply Monitoring and Reset

Shown in Figure 8 is an application using two UT01VS50D Voltage Supervisors to monitor both under voltage and over voltage of a power supply. In this application the top Voltage Supervisor monitors the under-voltage of a 5V power supply while the bottom Voltage Supervisor monitors the over voltage of the same 5V power supply. The 5V supply is monitored through the PFI input of both Voltage Supervisors. Resistor values for both under voltage and over voltage monitoring can be set to accommodate a range of power supply voltages.

During normal operation where VDD is within the allowed range (VDD_UND < VDD < VDD_OV), $\overline{\text{RESET\_OD}}$ of both Voltage Supervisors will be at logic high level. The Table 1 below shows the truth table for functional, under voltage detection and over voltage detection.

Table 1. Under Voltage Over Voltage Truth Table

VDD	$\overline{\text{PFO\_UND}}$	$\overline{\text{PFO\_OV}}$	$\overline{\text{RESET\_OD\_UND}}$	$\overline{\text{RESET\_OD\_OV}}$	$\overline{\text{RESET\_OD}}$	uP or ASIC Mode
Normal Operation	HIGH	LOW	HIGH	HIGH	HIGH	Normal
VDD < VDD_UND	LOW	LOW	LOW	HIGH	LOW	Reset Asserted
VDD > VDD_OV	HIGH	HIGH	HIGH	LOW	LOW	Reset Asserted

Note:

1. -UND specifies under voltage case. -OV specifies overvoltage case

Packaging

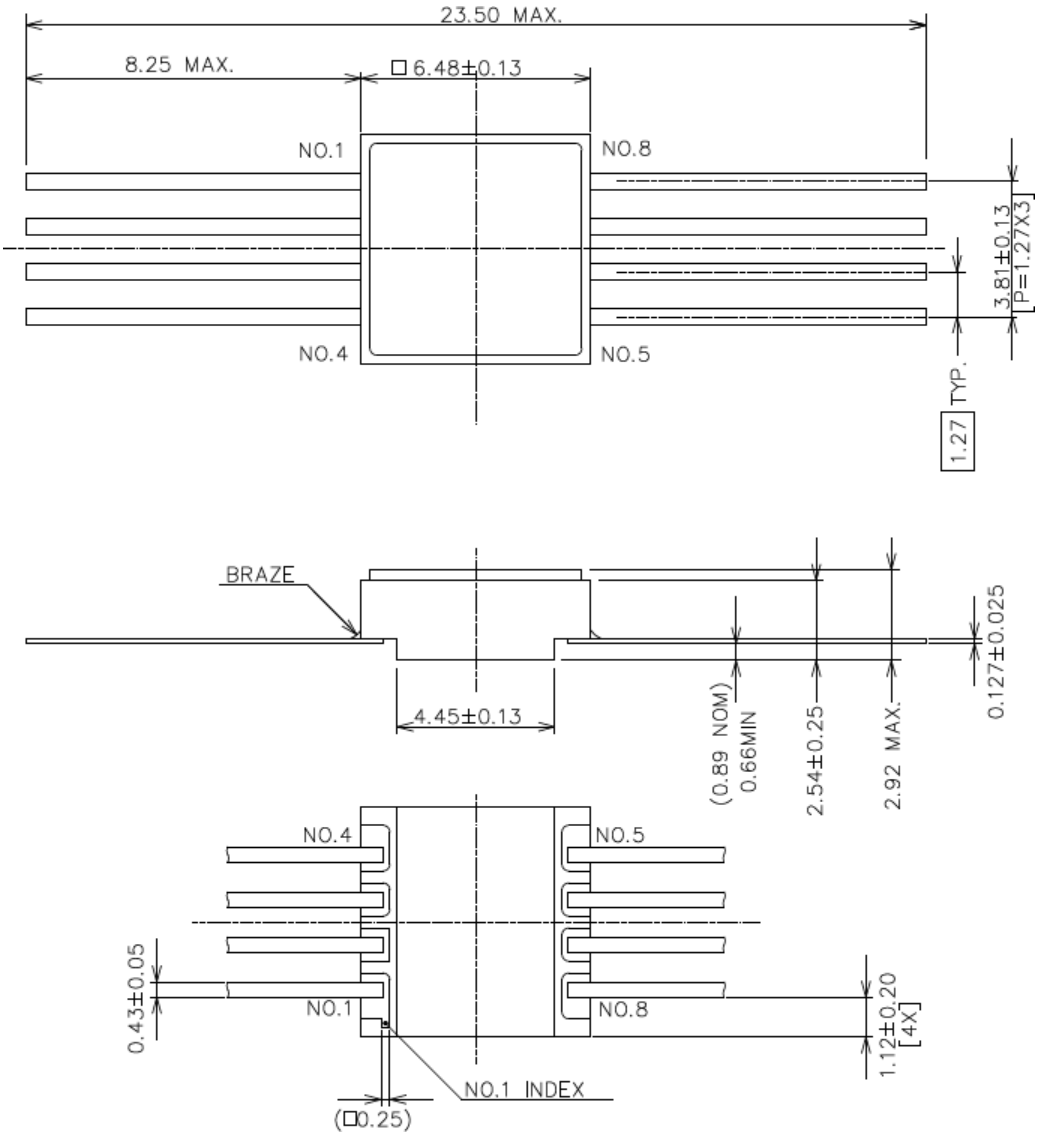


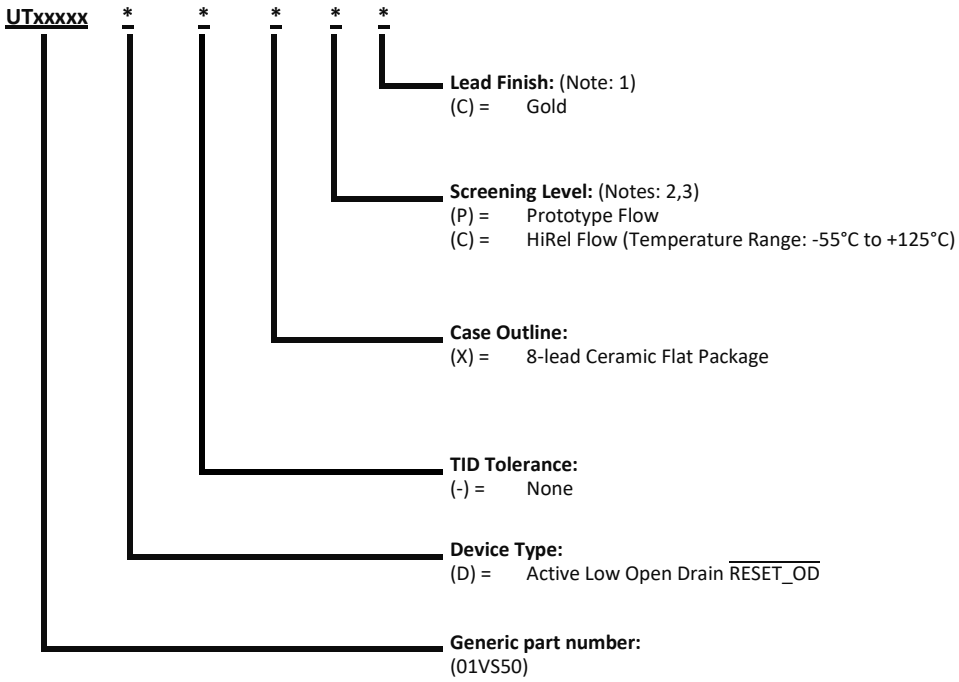
Figure 9. 8-pin Dual-In-Line Flatpack

Notes:

1. Package material: Opaque 90% minimum alumina ceramic.
2. All exposed metal areas must be gold plated 100 to 225 microinches thick over electroplated nickel undercoating 100 to 350 microinches thick per MIL-PRF-38535.
3. The seal ring is electrically connected to VSS.

Ordering Information

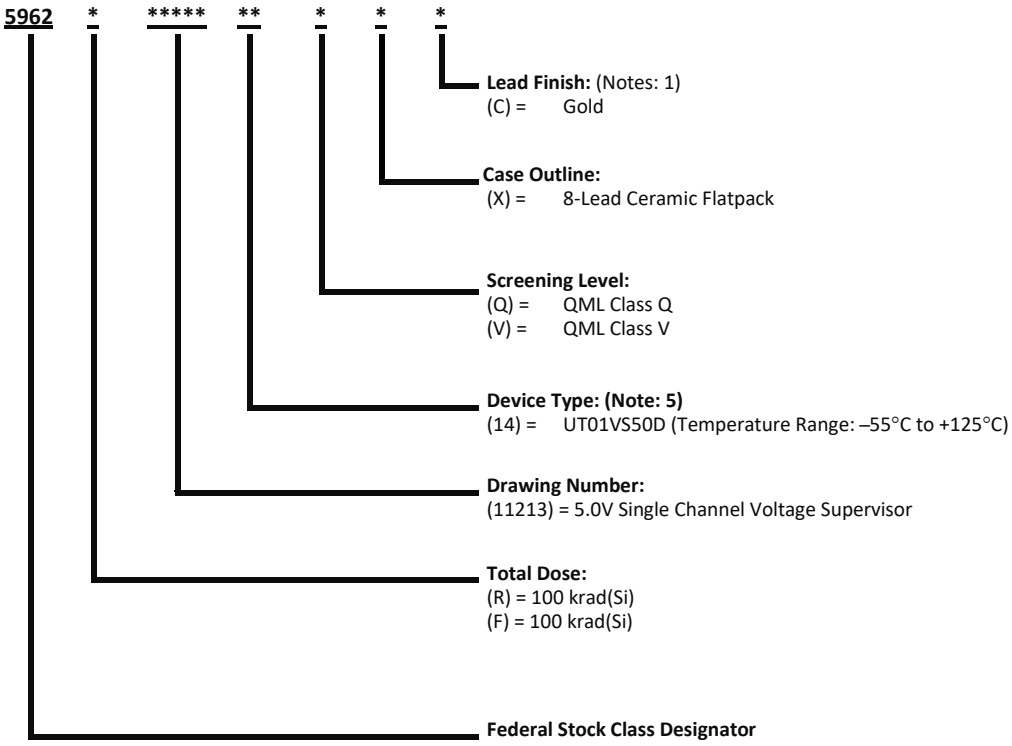
UT01VS50D Voltage Supervisor Frontgrade Part Numbering Ordering Information



Notes:

1. Lead finish is "C" (Gold) only.
2. Prototype flow per CAES Manufacturing Flows Document. Devices are tested at 25℃ only. Radiation neither tested nor guaranteed.
3. HiRel Flow per CAES Manufacturing Flows Document. Radiation neither tested nor guaranteed.

UT01VS50D Voltage Supervisor SMD Part Number Ordering Information



Revision History

Date	Revision #	Author	Change Description	Page #
12/16		RL	Frontgrade Datasheet format added along with edit to SMD Ordering on Device Type and Gold Finish.	
10/18		BM	Electrical Characterization Table - edits to VOL and ILEAK and removed VOH to match SMD	5
08/22		BM	Updated Package Drawing to current version.	11

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.