FRONTGRADE

APPLICATION NOTE

UT699-AN-01

UT699 Power Calculator

3/18/2010
Version #: 1.0.0

Product Name:	Manufacturer Part Number	SMD #	Device Type	Internal PIC Number:
LEON 3FT Microprocessor	UT699	5962-08228	01	WG07

Table 1: Cross Reference of Applicable Products

1.0 Introduction

This application note describes how to use the UT699 Power Calculator spreadsheet to calculate total device power dissipation. The application note is intended to provide the system designer with a better understanding of how power dissipation varies according to the specific operating conditions of the device, and how each individual core in the UT699 contributes to total power dissipation.

Disclaimer: The power figures determined by the power calculator should not be considered as absolute values as actual power dissipation will vary based upon the specific application. The power calculator is intended to provide a power estimate that is within +/-10% of the actual power dissipation in order to allow a system designer to budget for core and I/O power.

2.0 Understanding the Power Models

Determining power dissipation in a complex device such as the UT699 can be difficult without a complete understanding of the operating conditions of the device. Frequency and voltage will affect power dissipation. Furthermore, power dissipation is highly dependent on how the device is utilized. Each peripheral core independently contributes to the total power, and these contributions are a function of how each core is exercised by software or by the system. Section 3 will assist the designer by providing a description of the power models that apply to each core in the UT699, and how to properly enter values into the spreadsheet. From a power supply perspective, total device power dissipation is a sum of the power from the core logic (2.5V) supply and the I/O (3.3V) supply, and are calculated separately. From an operational perspective, total power is the sum of baseline power dissipation and activity-based power dissipation. These are described in this section.

2.1 Operating Modes

There are three operating modes for the UT699. Each is described in this section. The power calculator spreadsheet is primarily used to calculate power dissipation in the active mode of operation. However, the spreadsheet can also be used to quickly determine power dissipation in power-down mode by selecting the mode button for the

IU+STATIC function. All modes of operation assume that the core and I/O voltages are within the limits as specified in the UT699 Data Sheet.

2.1.1 Active

In active mode the system clock is ≥ 1MHz and the integer unit is actively processing instructions.

2.1.2 Standby

Standby mode is a static mode where all clocks are 0MHz. Power losses are due to quiescent current leakage. Static power losses can be obtained from the static currents as indicated in the UT699 Data Sheet.

2.1.3 Power Down

Power-down mode is a special mode of operation where the system clock is active, but the instruction pipeline is halted. In this mode the integer unit is partially active but is not actively processing instructions. Power-down mode is entered by performing a WRASR instruction to ASR19. Active mode is resumed via any interrupt.

2.2 Core and I/O Power

The UT699 uses separate power supplies for core logic and I/O, which operate from a 2.5V supply and a 3.3V supply, respectively. All of the UT699 peripheral cores draw power from the core logic supply. Any peripheral core that communicates outside of the device, such as the fault-tolerant memory controller (FTMCTRL) and PCI core, also draws current from the I/O supply. Power dissipation for each of the two supplies is calculated independently in order to be able to separately budget the power requirements for the two supplies.

2.3 Baseline Power

Baseline activity is defined as the minimum activity that can occur while the UT699 is performing some function. Practically speaking, this assumes an active integer unit (IU) and memory controller unit where the processor would be executing continuous NOP instructions. All other peripherals are assumed to be inactive with their corresponding clock inputs disabled. Total device power dissipation is therefore the sum of baseline power dissipation and the static power dissipated by all of the other cores. Power-down and standby are modes that represent idle or static operating conditions where the processor is not executing instructions. As such, they are not used as the baseline operating condition. Baseline power dissipation is a function of the frequency of the system clock, temperature, and memory controller activity. Frequency and temperature dependency will be treated in the following sections.

2.4 Frequency Dependency

Power dissipation is mostly linear over frequency from 1MHz to the maximum operating frequency of 66MHz. The linear nature occurs because switching losses are linear with frequency and tend to dominate dc leakage losses. Figure 1 shows power as a function of frequency for a typical application normalized to 66MHz. Power dissipation in Figure 1 includes both core logic and I/O power for a typical application that is exercising only the IU and FTMCTRL e.g. the Dhrystone benchmark.

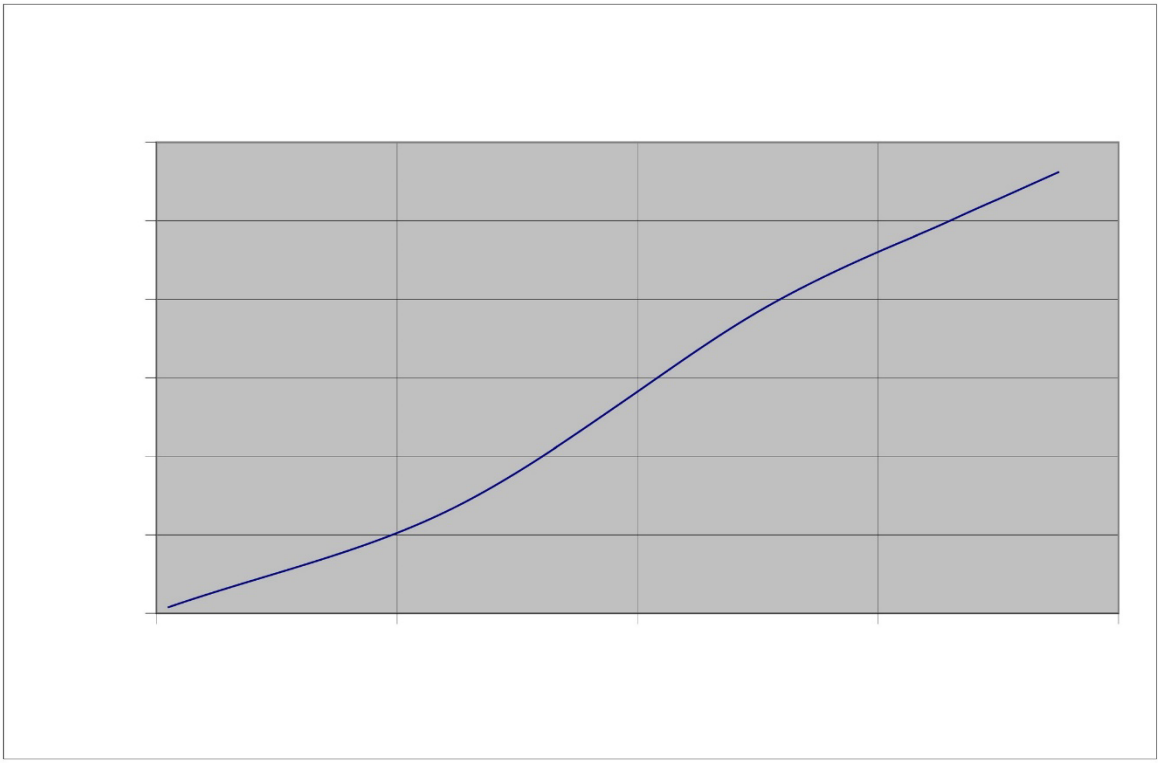

Figure 1. Normalized Power Dissipation as a Function of Frequency

2.5 Temperature Dependency

Power dissipation is nearly flat over temperature. Figure 2 shows that power is approximately 1% higher at the low and high temperature extremes of -40C and +125C from the normalized power at +25C. Power dissipation in Figure 2 includes both core logic and I/O and represents a typical application that is exercising only the IU and FTMCTRL e.g. the Dhrystone benchmark. Because of the nearly flat dependency with temperature, calculated power is assumed to not vary over temperature.

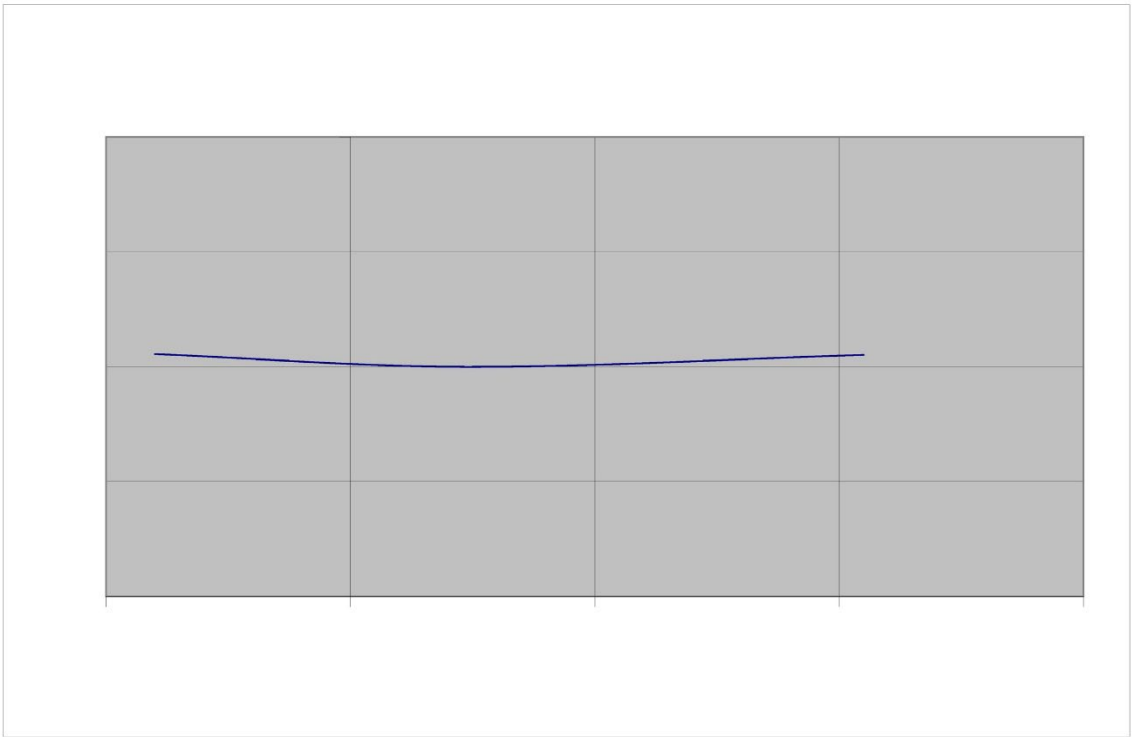

Figure 2. Normalized Power Dissipation as a Function of Temperature

2.6 Activity-based Models

Each core in the UT699 will dissipate power according to its utilization. For example, power dissipation of the memory controller is a function the occurrence of read and write activity. Power dissipation in the SpaceWire core will depend upon the SpaceWire clock frequency, the number of active SpaceWire nodes, and the occurrence of signal transmission and reception. The activity-based model for each core takes into account the manner in which each core is utilized in the system and by software. The following cores have activity-based models that are described in Section 3.

- Integer Unit (IU)
- Fault-Tolerant Memory Controller Unit (FTMCTRL)
- Instruction Cache (ICACHE) and Data Cache (DCACHE)
- Floating Point Unit (FPU)
- Frontgrade Research PCI (GRPCI)
- SpaceWire Ports 1-4 (SPW1-SPW4)
- CAN Ports 1-2
- Ethernet

The power contributions from the following cores are negligible and are therefore not included in the power calculator.

- Memory Management Unit (MMU)
- General Purpose Timer (GPTIMER) 1-4
- APBUART
- General Purpose Input/Output (GPIO)

3.0 Using the Power Calculator Spreadsheet

3.1 Integer Unit

The Integer Unit (IU) operates at the same frequency as the system clock. Therefore, power dissipation is a function of the system clock frequency, which is set via the System Clock parameter at the top of the spreadsheet. The IU is always active except when the processor is in standby mode. Power dissipated by the IU represents the activity of the core logic of the LEON 3FT during normal processing activity. In practice, it is difficult to know the percent utilization of the IU as some sections of the logic will be active, and others inactive, during any execution of code. To simplify the activity model two modes of operation are assumed: Active and Power Down. The active state represents the activity level during normal code execution, while the power-down state represents core logic activity when the processor is in power-down mode. Sections of the core logic are active during power-down mode even though the instruction pipeline is halted. This is necessary in order for an interrupt to be able to wake up the processor from this mode.

3.1.1 Integer Unit Mode

The IU can be enabled or disabled by selecting the mode button or by selecting the PWR DOWN preset configuration.

3.2 Fault-Tolerant Memory Controller

The Fault-Tolerant Memory Controller (FTMCTRL) operates at the same frequency as the system clock. Therefore, power dissipation is a function of the system clock frequency, which is set via the System Clock parameter at the top of the spreadsheet. Instruction and/or data memory accesses are always occurring normal processor activity. When instruction or data memory is not cached the FTMCTRL makes the accesses from external memory. The user can select one of three modes of operation: High Read, High Write, and Low. These modes are explained in the next section.

3.2.1 FTMCTRL Mode

The FTMCTRL unit is always enabled except in power-down mode. The mode of operation is used to select the values for the %Reads and %Writes fields. These fields indicate the percentage of total CPU activity that is dedicated to performing memory read and write accesses, respectively.

The percentage of read and write activity can be difficult to determine without an extensive understanding of the assembly code, a thorough knowledge of interrupt activity, and a complete understanding of CPU activity introduced by the peripheral cores such as PCI and SpaceWire that can perform DMA accesses to external memory. Write activity is especially difficult to estimate as each write necessarily requires one or more read accesses to read the instruction(s) corresponding to the write instruction. The following activity models are provided to assist the user. The percentages provided represent approximations, as actual activity is highly code dependent. Note that the percentages will not sum to 100% as some CPU time is taken up by the instruction pipeline.

- High read activity: The CPU is continuously fetching instructions and no write activity is occurring except an update to a loop index. All instructions take two clock cycles to execute. Read activity is 83% and write activity is 3%.
- High write activity: The CPU is performing continuous data writes to memory. Read activity is 71% and write activity is 19%. This activity will result in the highest power dissipation from the FTMCTRL.
- Low activity: The CPU is executing continuous instructions that take a large number of CPU clock cycles with no write activity occurring. Read activity is 76% and write activity is 0%.

3.3 Cache

The cache core consists of the instruction cache (ICACHE) and data cache (DCACHE) and operates at the same frequency as the system clock. Therefore, power dissipation is a function of the system clock frequency, which is set via the System Clock parameter at the top of the spreadsheet. The instruction and data caches have two states: enabled and disabled. During normal processor activity, instruction and data are constantly being read from or written to memory. The instruction and data are either located in the external memory accessed by the memory controller, or they reside in cache and are accessed directly by the LEON 3FT core. Accesses to cache are faster, but always consume slightly higher core power than accesses from external memory. Read accesses from cache result in lower I/O power as the memory controller is not used to fetch data or instructions from external memory. Conversely, write accesses to cache result in higher I/O power because any time the cache is updated, a write-through to external memory must also occur.

Cache utilization is highly code dependent. If the code or data is compact or use a contiguous memory space, more cache hits will occur. Conversely, if code or data is large are scattered throughout a large memory space, more cache misses will occur. The power calculator power model for cache assumes 100% cache hits.

3.3.1 Cache Mode

Instruction and data caches are either enabled or disabled.

3.4 FPU

The Floating-Point Unit (FPU) operates at the same frequency as the system clock. Therefore, power dissipation is a function of the system clock frequency, which is set via the System Clock parameter at the top of the spreadsheet. In order to understand how the FPU affects power, it is necessary to understand how compiled code is optimized to take advantage of the FPU. The UT699 includes a full IEEE-754 floating-point unit that is capable of performing floating-point operations in parallel with the integer unit instruction pipeline. Without the FPU, the assembly code listing of floating-point intensive code would be larger than code assembled without the FPU, as single floating-point instructions would have to be emulated using several integer instructions. The activity model for the FPU compares the continuous execution of floating-point instructions with and without the FPU enabled. With the FPU enabled, core power for floating-point intensive code that is executing continuous FMUL and FDIV instructions is reduced by about 2%, and I/O power is reduced by about 6%.

3.4.1 FPU Mode

The FPU is either enabled or disabled.

3.5 PCI

Power consumption from the Frontgrade Research PCI (GRPCI) core is a contribution from the PCI clock tree and the PCI core. Both of these must be considered in order to accurately calculate total PCI power.

3.5.1 PCI Clock

PCI frequency is set via the PCI Clock parameter at the top of the spreadsheet. The PCI clock tree dissipates power whenever a 33MHz clock is applied to the PCICLK pin. The clock input to this pin should be disabled when the PCI core is disabled for maximum power savings.

3.5.2 PCI Mode

The PCI core is either enabled or disabled using the clock-gating unit. This allows the system to power down the PCI core for power savings when it is not being utilized. With the PCI core enabled, power dissipation is a function of the system clock frequency independent of whether or not a clock input is applied to the PCICLK pin. This is because the PCI core consists of FIFO interfaces to the AMBA bus that operates from the SYSCLK domain.

3.6 SpaceWire

SpaceWire power consumption is a contribution from the SpaceWire clock tree and the mode of operation. Both of these must be considered in order to accurately calculate total SpaceWire power.

3.6.1 SpaceWire Clock

SpaceWire transmit frequency is set via the SpaceWire TX Clock parameter at the top of the spreadsheet. The SpaceWire clock tree dissipates power whenever the clock is applied to the SPWCLK pin. The clock input to this pin should be disabled when the SpaceWire core is disabled for maximum power savings.

3.6.2 SpaceWire Mode

Each SpaceWire core is either enabled or disabled using the clock-gating unit. This allows the user to power down any SpaceWire core for power savings when it is not being utilized. SpaceWire cores 1-4 can operate in common, or standard, mode. Cores 3 and 4 can additionally operate in RMAP mode. The mode can be selected from the pulldown menu. With any SpaceWire core enabled, power dissipation is a function of the system clock frequency independent of whether or not a clock input is applied to the SPWCLK pin. This is because each SpaceWire core consists of FIFO interfaces to the AMBA bus that operates from the SYSCLK domain. Note that there is no discernible power difference between common and RMAP modes.

3.7 Control Area Network (CAN)

CAN power consumption is a function of the mode of operation.

3.7.1 CAN Mode

The CAN cores are either enabled or disabled using the clock-gating unit. This allows the user to power down the CAN cores for power savings when they are not being utilized. The clock-gating unit can be used to enable or disable both CAN cores. They cannot be enabled or disabled independently of one another. Modes of operation include BasicCAN and PeliCAN. PeliCAN mode will result in slightly higher power dissipation than BasicCAN mode. The mode can be selected from the pulldown menu.

3.8 Ethernet

Ethernet power consumption is a contribution from the Ethernet clock tree and the mode of operation. Both of these must be considered in order to accurately calculate total Ethernet power.

3.8.1 Ethernet Clock

Ethernet frequency is set via the Ethernet Clock parameter at the top of the spreadsheet. The Ethernet clock tree dissipates power whenever a clock is applied to the ETH_TX and ETH_RX pins. The clock inputs to these pins should be disabled when the Ethernet core is disabled for maximum power savings.

3.8.2 Ethernet Mode

The Ethernet core is either enabled or disabled using the clock-gating unit. This allows the user to power down the Ethernet core for power savings when it is not being utilized. When enabled, the user can select from 10 Base-T and 100 Base-T operation.

3.9 Using the Nominal Preset Button

The Nominal Preset button places the UT699 into a nominal mode whereby the processor is assumed to be in a typical state of operation, with all cores turned off except the IU and FTMCTRL. All clock inputs are turned off except SYSCLK, which is set to 66MHz. The FTMCTRL is set to HIGH READ mode, and caches are disabled. This would be representative of a state where the processor is executing integer code such as the Dhrystone benchmark, with no I/O accesses except to external memory. The Nominal Preset button can be used as a starting point to put the processor into a typical state before other core activities are selected.

4.0 Thermal Considerations

4.1 Determining Junction Temperature

The power calculator spreadsheet can be used to determine the operating junction temperature based upon the case temperature, power dissipation, and junction-to-case thermal impedance. The expression for this is:

$$TJ = TC + (PD * \Theta JC).$$

For example, suppose the case is set to the maximum allowable temperature of 105°C. Power dissipation is calculated at 1.5W, and QJC for the 352 CQFP package as indicated in the UT699 data sheet is 5°C/W. In this case, the junction temperature calculated by the spreadsheet and indicated in the Junction Temp field would be:

$$T_J = 105°C + (1.5W * 5°C/W) = 112.5°C.$$

4.2 Determining Case to Ambient Thermal Impedance

The spreadsheet can also be used to calculate the maximum case-to-ambient thermal impedance if the ambient temperature and power dissipation are known. The expression for case-to-ambient thermal impedance is:

$$\Theta_{CA} = (T_C - T_A) / P_D.$$

For example, if the ambient temperature is 85°C and power dissipation is 2.5W, the maximum value for QCA required to keep the case temperature at or below 105°C would be:

$$\Theta_{CA} = (105°C - 85°C) / 2.5W = 8°C/W.$$

Revision History

Date	Revision #	Author	Change Description	Page #
3/18/2020	1.0.0	N/A	Initial Release	