FRONTGRADE

APPLICATION NOTE

UT699-AN-06

UT699 Minimum System Design Example

9/9/2010
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Product Name:	Manufacturer Part Number	SMD #	Device Type	Internal PIC* Number:
UT699 32-bit Fault-Tolerant SPARC V8/LEON 3FT Processor	UT699	5962-08228	01, 02	WG07

Table 1: Cross Reference of Applicable Products

* PIC = Product Identification Code

1.0 Overview

The UT699 Leon 3FT microprocessor is a versatile system-on-chip device with a large feature set of core functionality and configuration options. For example, the device features four SpaceWire cores, a PCI and Ethernet core, and the ability to interface with different memory devices such as PROM, SRAM and SDRAM. In some instances, not all of the functionality of the UT699 is required. In these cases, the non-utilized cores can be disabled for power savings making the UT699 an ideal choice for systems that do not require the extensive built-in functionality of the device.

This application note presents a notional design example for a system based upon a reduced subset of the full feature set of the UT699 processor and shows how this system can be designed into a small form factor with minimum power dissipation.

2.0 Minimum System Design Requirements

The requirements for the minimum system are indicated in Table 2.

System Function	Design Requirements	Device
Operating frequency	10MHz	10MHz crystal oscillator
Supply voltages	3.3V, 2.5V, 1.8V	VRG8662 adjustable positive LDO regulator
SRAM	16MB with EDAC 32-bit data width	UT8R4M39 160Mbit SRAM with EDAC
Non-volatile memory	1MB with EDAC 8-bit data width	UT8MR8M8 64Mbit MRAM
SpaceWire	Two ports with a transmit clock of 10MHz	UT54LVDS-031 driver UT54LVDS-032 receiver
Software debug	DB-9 for GPIO DB-9 for DSU UART	Two DB-9 connectors RS232 quad transceiver

Table 2: System Requirements

2.1 Frequency and Power Requirements

Since both the UT699 core and SpaceWire cores will be operating at 10MHz, a single 10MHz crystal oscillator can be used. Three voltage sources are required: 2.5V for the UT699 core; 3.3V for I/O, PROM, and LVDS drivers; and 1.8V for the SRAM core.

2.2 Memory Requirements

SRAM and non-volatile memory both require EDAC check bits. Therefore, the effective capacity of the devices must be at least 20MB and 1.25MB, respectively. The device chosen for SRAM is a 160Mbit, multi-chip module that is configured with a 32-bit data width plus 7 bits for the EDAC check bits. Total memory capacity, including the check bits, is 20MB. The non- volatile memory is an MRAM device configured with an 8-bit data width. Total memory capacity is 2MB. In a x8 configuration, the upper 20% of memory is used to store the EDAC check bits. This leaves 1.25MB for data/instruction storage.

2.3 SpaceWire Requirements

Each SpaceWire channel requires two LVDS receivers and drivers. The devices chosen are quad receiver/transmitters and satisfy the SpaceWire physical interface requirements.

2.4 Debug Requirements

A Debug Support Unit (DSU) port is necessary for software development. The DSU port can interface over PCI, DSU UART, JTAG, or SpaceWire. The simplest debug interface uses the dedicated DSU UART port. The only requirement for debug in this case is a DB-9 connector, RS232 transceiver, and RS232 port on the system hardware that is used for software development. A general purpose UART can also facilitate software development. For this reason, a second DB-9 connector is used to provide access to this UART. A 16-pin header is used to allow access to the General Purpose I/O (GPIO) pins.

For flight, the two DB-9 RS232 connectors, the GPIO header, and the RS232 transceiver would not be populated.

3.0 System Block Diagram

The block diagram of the system is shown in Figure 1. The blocks for the individual devices and connectors include the required keep-out areas for manufacturing.

3.1 Power Requirements

Table 3 shows the required power from each of the three power supplies. Power dissipation assumes nominal voltage and 25C case operating temperature and does not include the power losses of the voltage regulators. Power dissipation for the memory devices is the rated power for memory read cycles. In order to achieve the lowest possible power dissipation, all unused cores, e.g., PCI and Ethernet are turned off using the Clock Gating Unit. Power dissipation of the UT699 microprocessor can be verified using the *UT699 Power Calculator Spreadsheet* available at http://www.frontgrade.com/.

Supply	UT699	MRAM	SRAM	LVDS DRV	LVDS RCV	Total
2.5V	0.342W					0.342W
3.3V	0.096W	0.330W	0.026W	0.059W	0.050W	0.561W
1.8V			0.405W			0.405W
Total						1.308W

Table 3: Power Requirements

3.2 Board Dimensions

The total size of the printed circuit board is 4.3” x 4.3” for a total area of 18.5 sq-in.

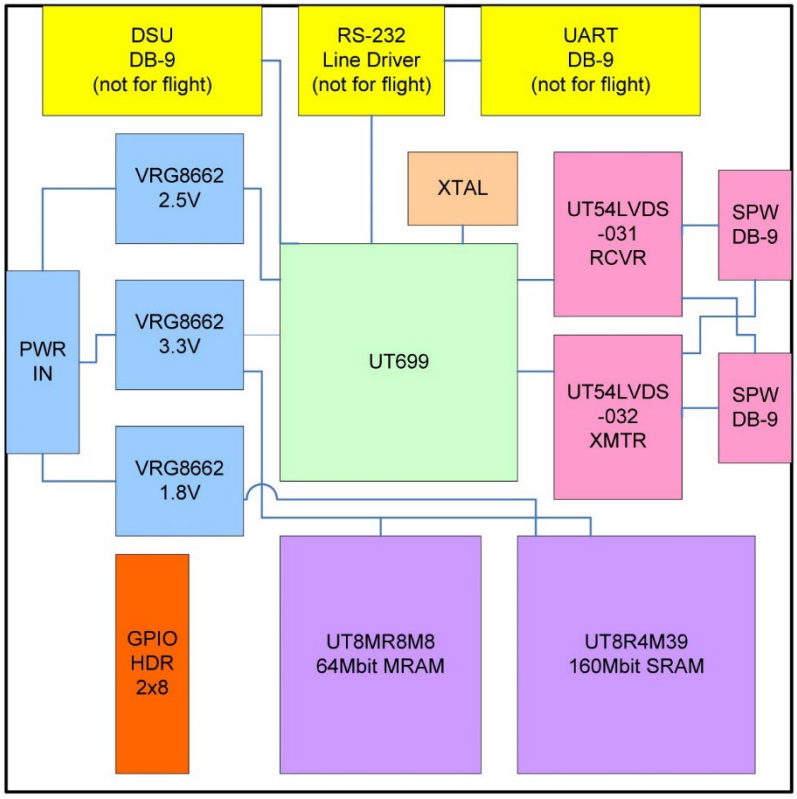

Figure 1. Block Diagram

4.0 Conclusion

This application note shows how to design an entire system based around the UT699 for minimal power dissipation and in a small form factor. The system in the preceding example has a total power dissipation of only 1.308W and in a form factor of only 18.5 sq-in. However, the system supports two SpaceWire ports operating at 10MHz, 16MB of data memory, and 1.25MB of instruction memory.

Revision History

Date	Revision #	Author	Change Description	Page #
9/9/2010	1.0.0	N/A	Initial release	