FRONTGRADE

APPLICATION NOTE

AN-LVDS-014-01

Calculating Power Dissipation for UT54LVDS217 and UT54LVDS218

6/5/2013

Version #: 1.0.0

Table 1: Cross Reference of Applicable Products

Product Name:	Manufacturer Part Number	SMD #	Device Type	Internal PIC
3.3V Serializer	UT54LVDS217	5962-01534	01, 02	WD11, WD13
3.3V Deserializer	UT54LVDS218	5962-01535	01, 02	WD12,WD14

Note:
*PIC = Product Identification Code

Overview

The UT54LVDS217 Serializer converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is propagated in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock (Tx CLK IN) 21 bits of input data are sampled and transmitted. The UT54LVDS218 Deserializer converts the three LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 75MHz, 21 bits of TTL data are transmitted at a rate of 525Mbps per LVDS data channel. Using a 75MHz clock, the data throughput is 1.575 Gbps.

Accurate power calculations are useful in estimating system power supply and thermal management requirements. The purpose of this application note is to review power consumption of Frontgrade Colorado Springs UT54LVDS217 Serializer and UT54LVDS218 Deserializer. This application note develops the components of LVDS power consumption and example power dissipation calculations for typical LVDS UT54LVDS217 and UT54LVDS218 applications.

A standard point-to-point configuration using the UT54LVDS217/UT54LVDS218 (SerDes) is shown in Figure 1. This configuration is terminated by a 100W resistor across each differential pair. A constant current source feeds the differential outputs of the driver. The direction of current flow through the termination resistor determines the logic state of the receiver output. Total power consumed by the standard point-to-point configuration is the device power minus the termination power. The LVDS output power consumption is a function of the output swing and the termination.

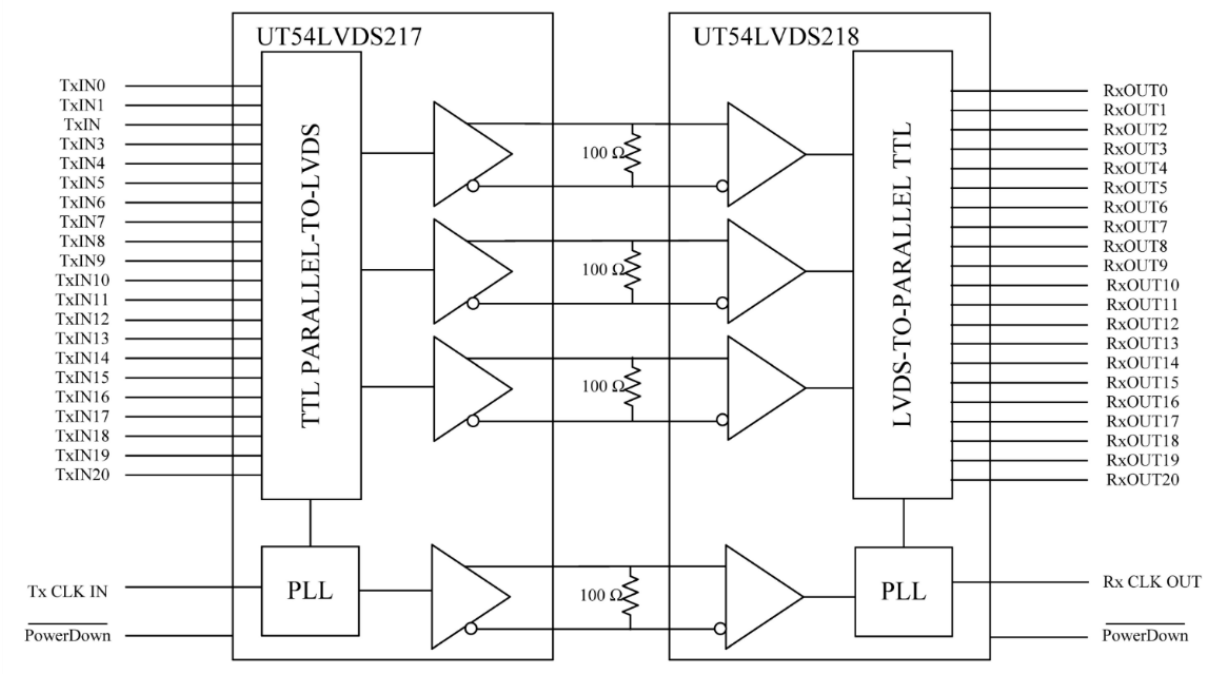

Figure 1. Standard UT54LVDS217 and UT54LVDS218 Configuration

Technical Figures and Data

The following plots show active current, or AIDD, measurements versus frequency and are used as input current for calculating power dissipation. The AIDD values are measurements taken during characterization of the SerDes devices configured under the following conditions.

Please note that the data contained in this application note was obtained in a lab. The test setup does not exactly match the test configurations shown for the AC and DC electrical characteristics described in the Frontgrade Datasheets and corresponding DSCC SMDs.

UT54LVDS217 and UT54LVDS218 Device Data

Temperature:	TC = 25°C, +125°C, -55°C,
Voltage:	VDD =3.0V, 3.3V, and 3.6V
Frequency:	ƒ =0MHz, 15MHz, 22.5MHz, 30MHz, 37.5MHz, 45MHz, 52.3MHz, 60MHz, 67.5MHz, and 75MHz
Capacitive Load:	CLT = 10pF, 32pF, and 49pF

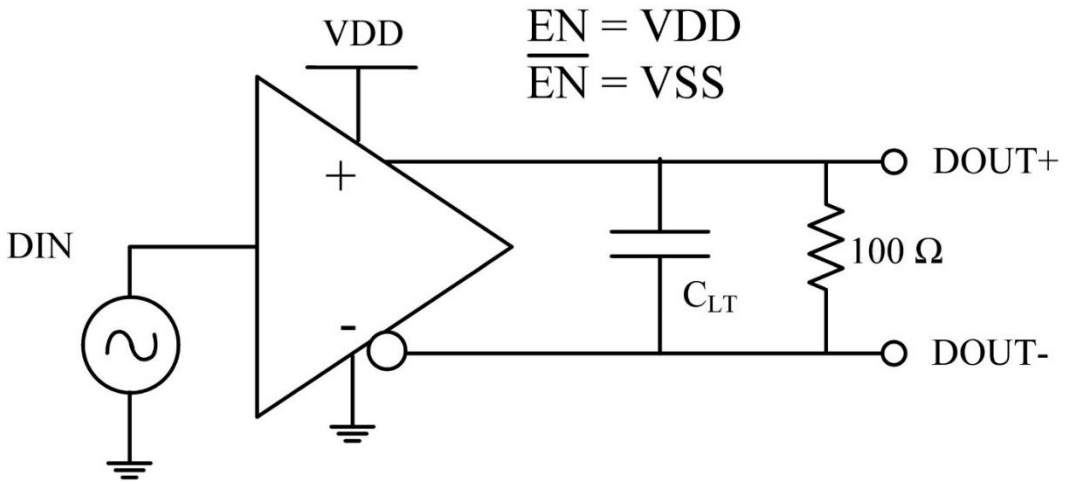

Figure 2A. LVDS Serializer Test Configuration.

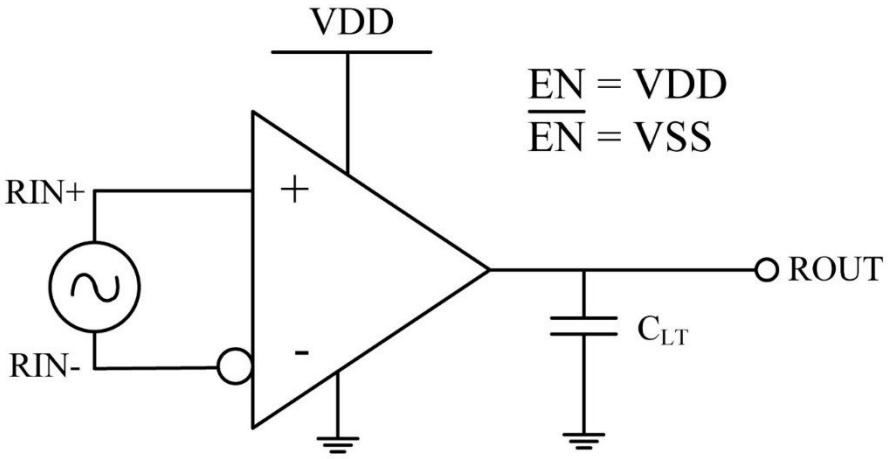

Figure 2B. LVDS Deserializer Test Configuration.

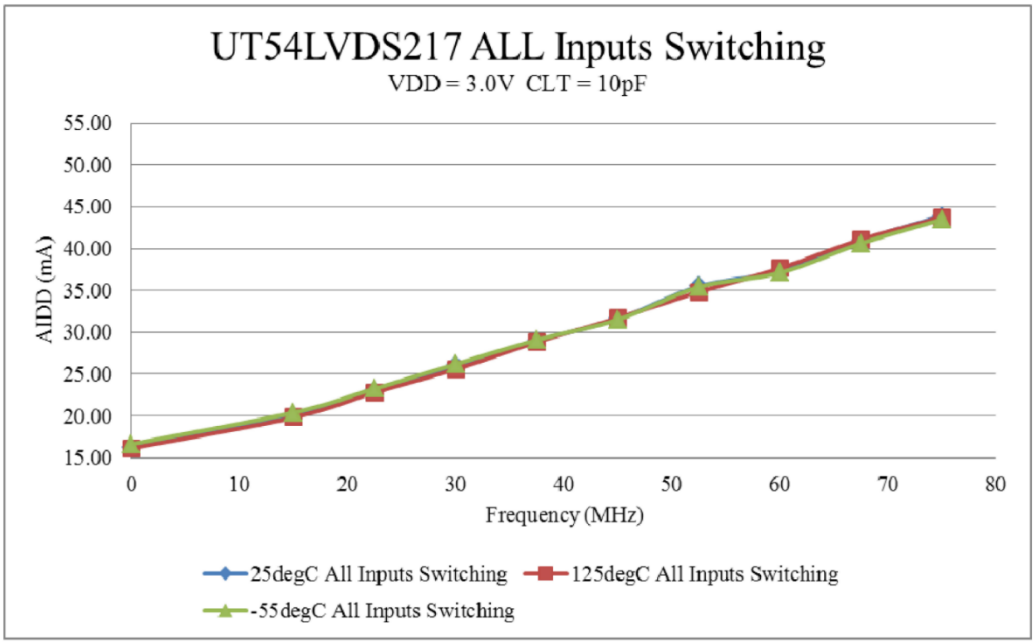

Figure 3. UT54LVDS217 Active current vs. Frequency for VDD = 3.0V, CLT = 10pF

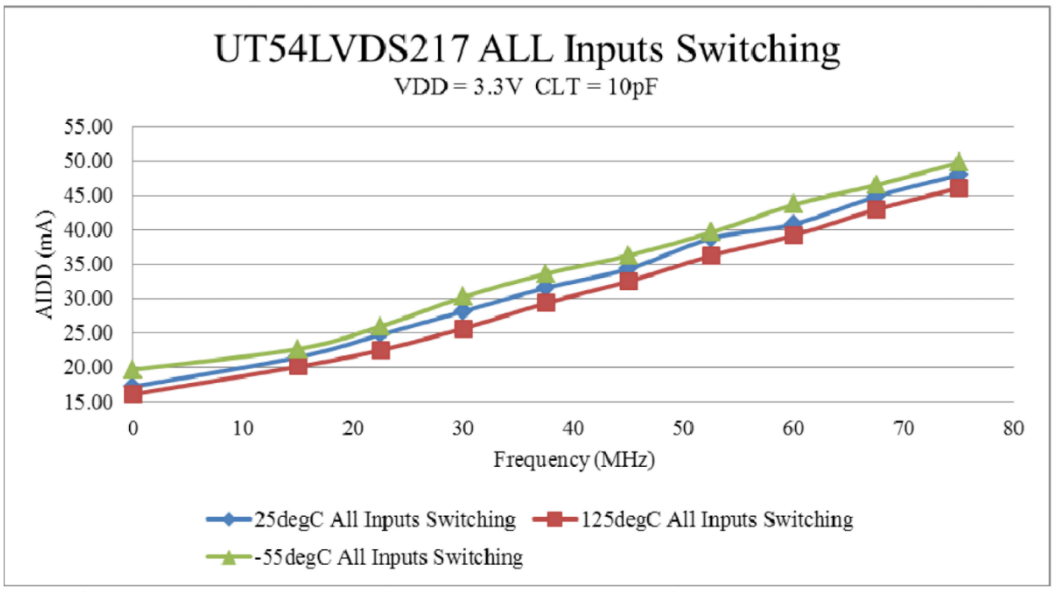

Figure 4. UT54LVDS217 Active current vs. Frequency for VDD = 3.3V, CLT = 10pF

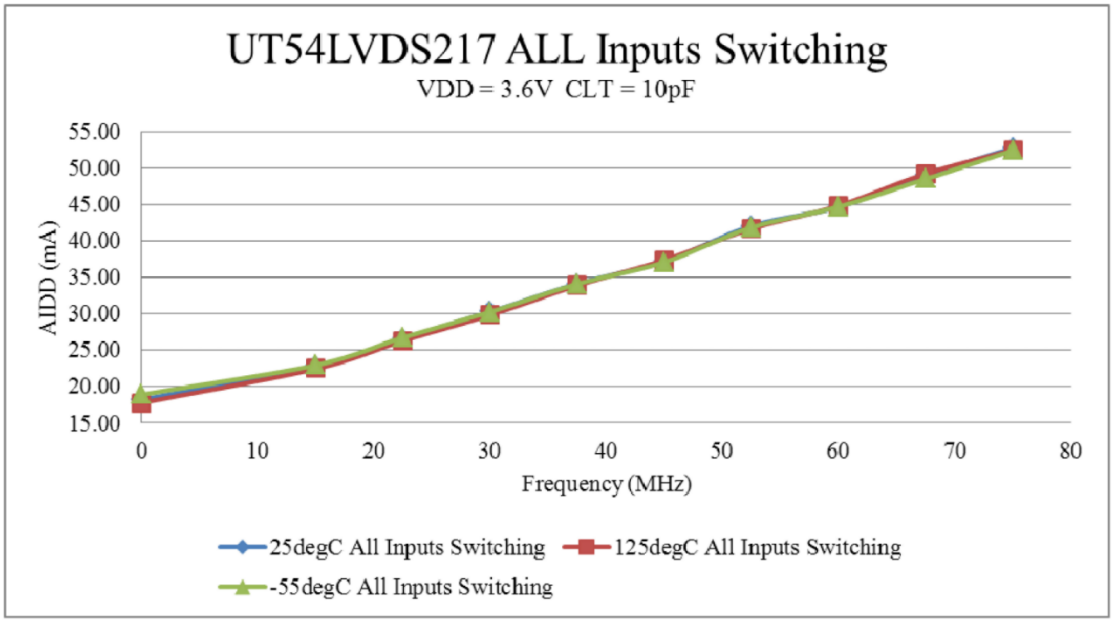

Figure 5. UT54LVDS217 Active current vs. Frequency for VDD = 3.6V, CLT = 10pF

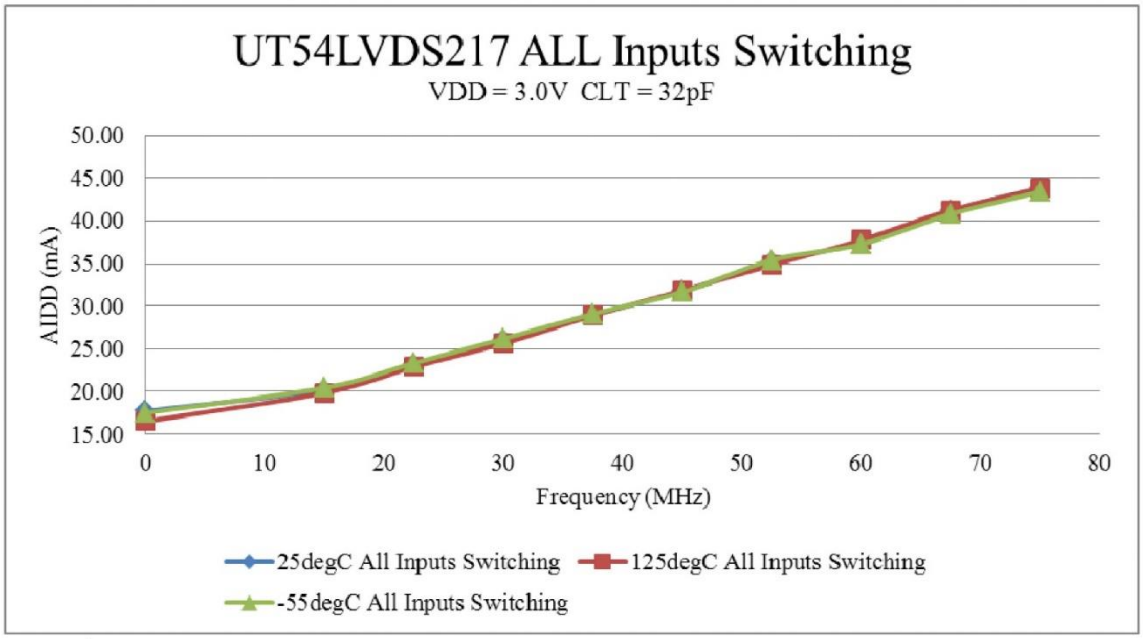

Figure 6. UT54LVDS217 Active current vs. Frequency for VDD = 3.0V, CLT = 32pF

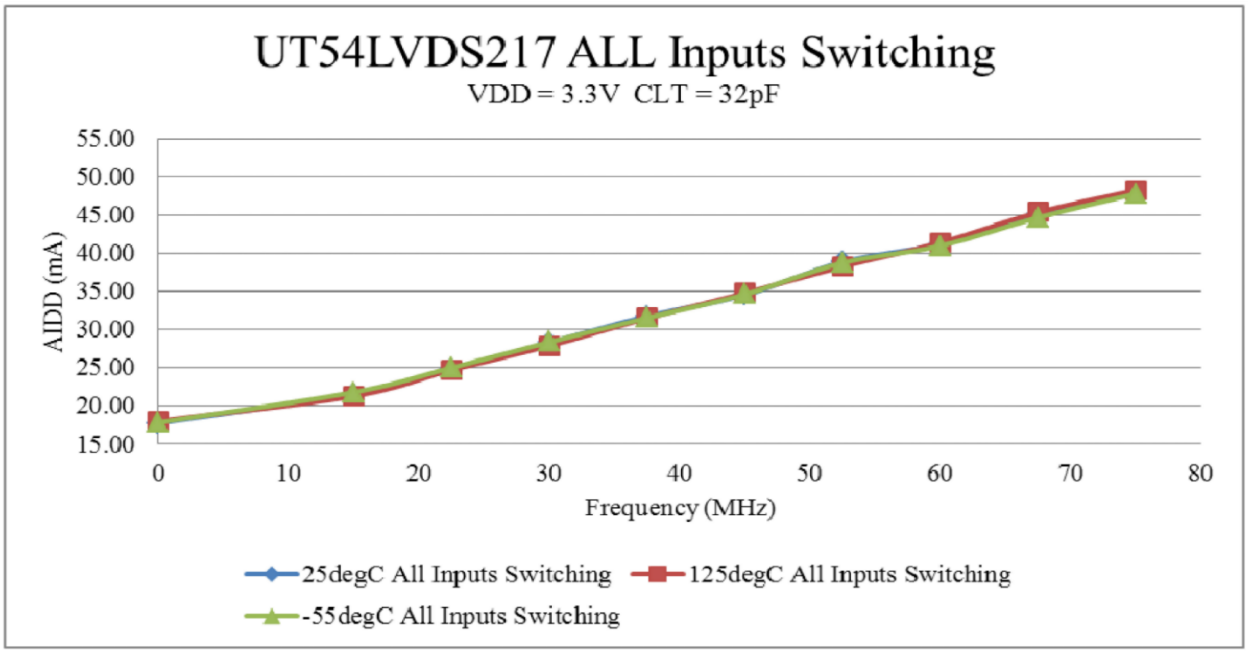

Figure 7. UT54LVDS217 Active current vs. Frequency for VDD = 3.3V, CLT = 32pF

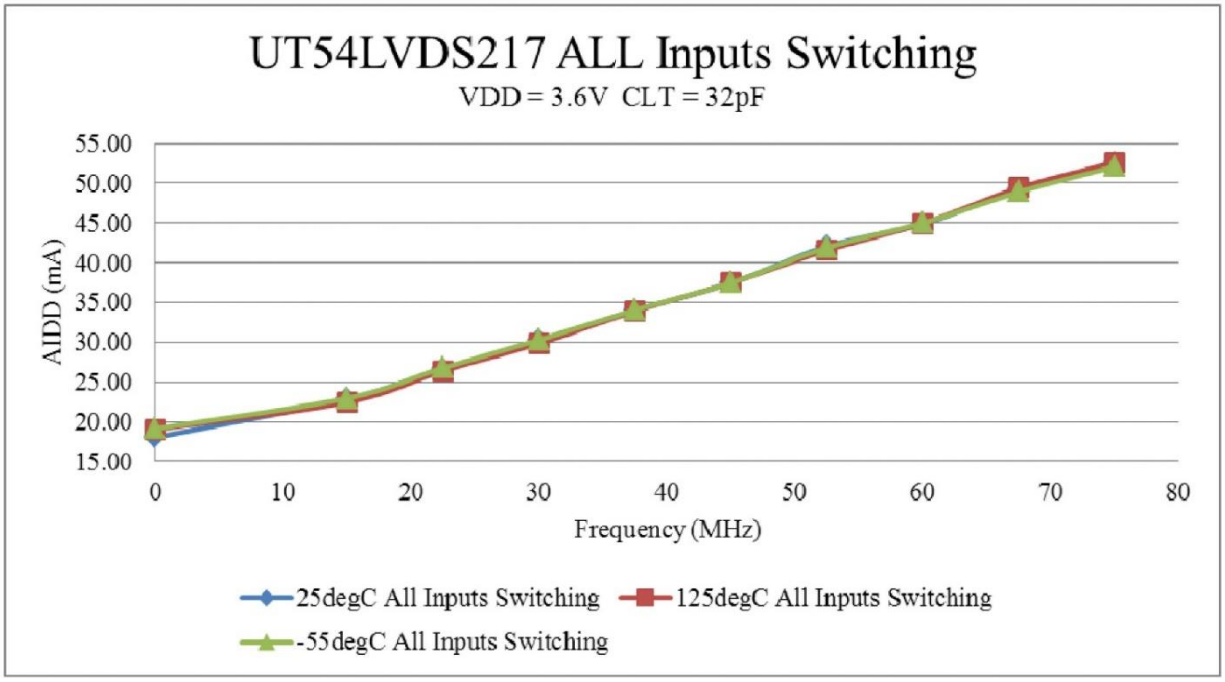

Figure 8. UT54LVDS217 Active current vs. Frequency for VDD = 3.6V, CLT = 32pF

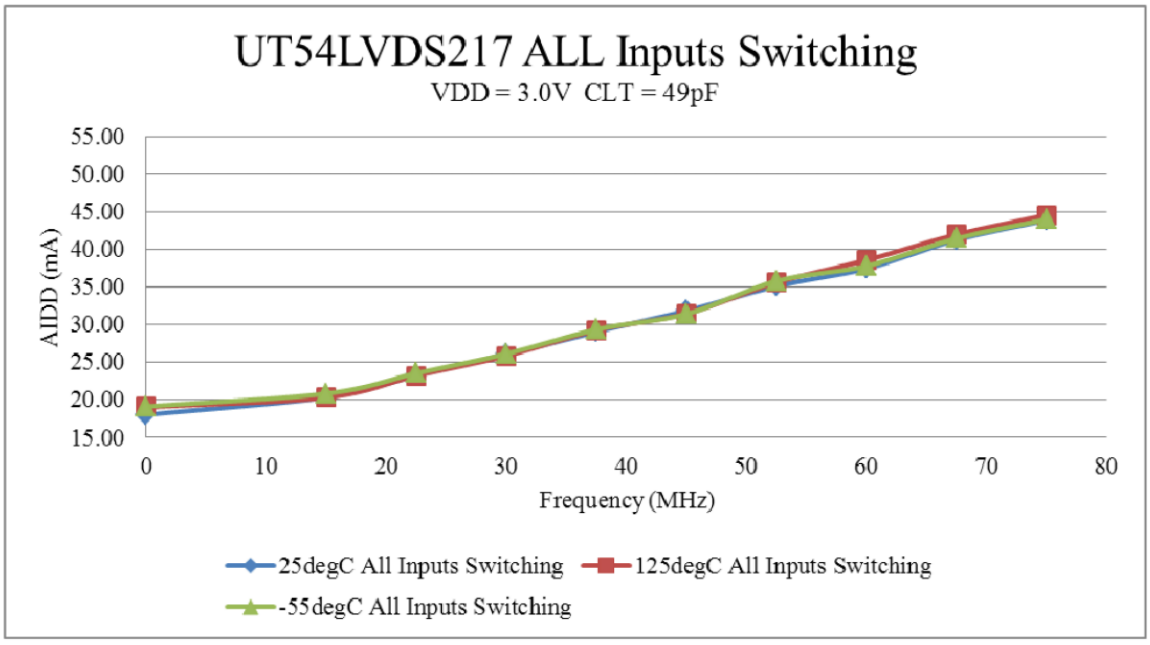

Figure 9. UT54LVDS217 Active current vs. Frequency for VDD = 3.0V, CLT = 49pF

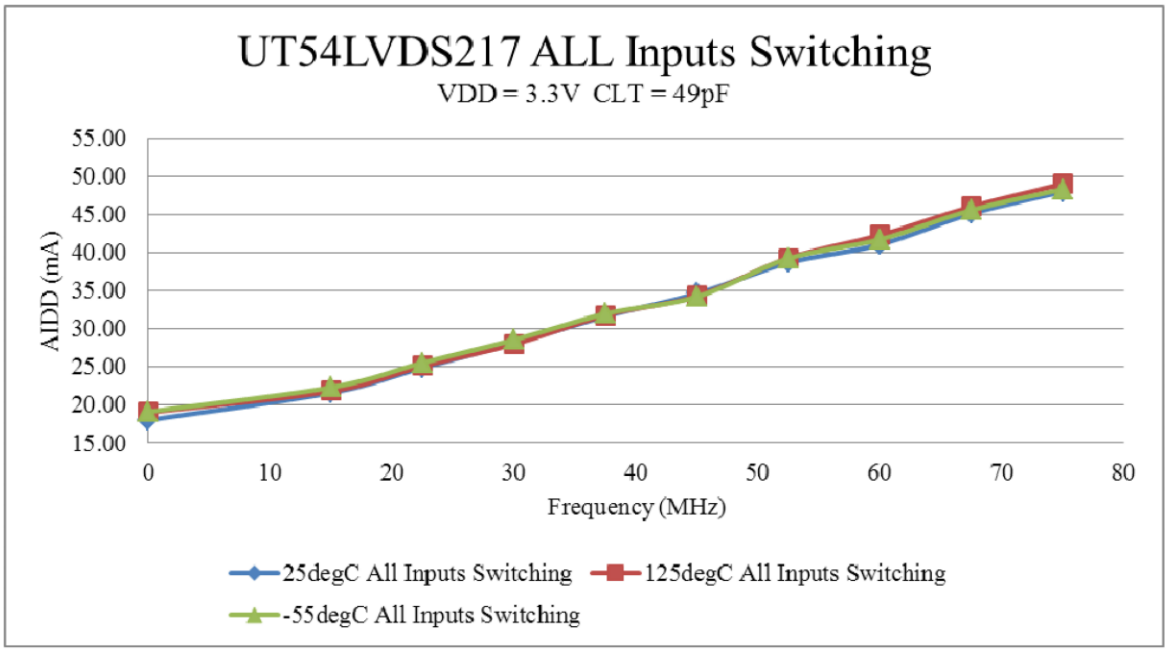

Figure 10. UT54LVDS217 Active current vs. Frequency for VDD = 3.3V, CLT = 49pF

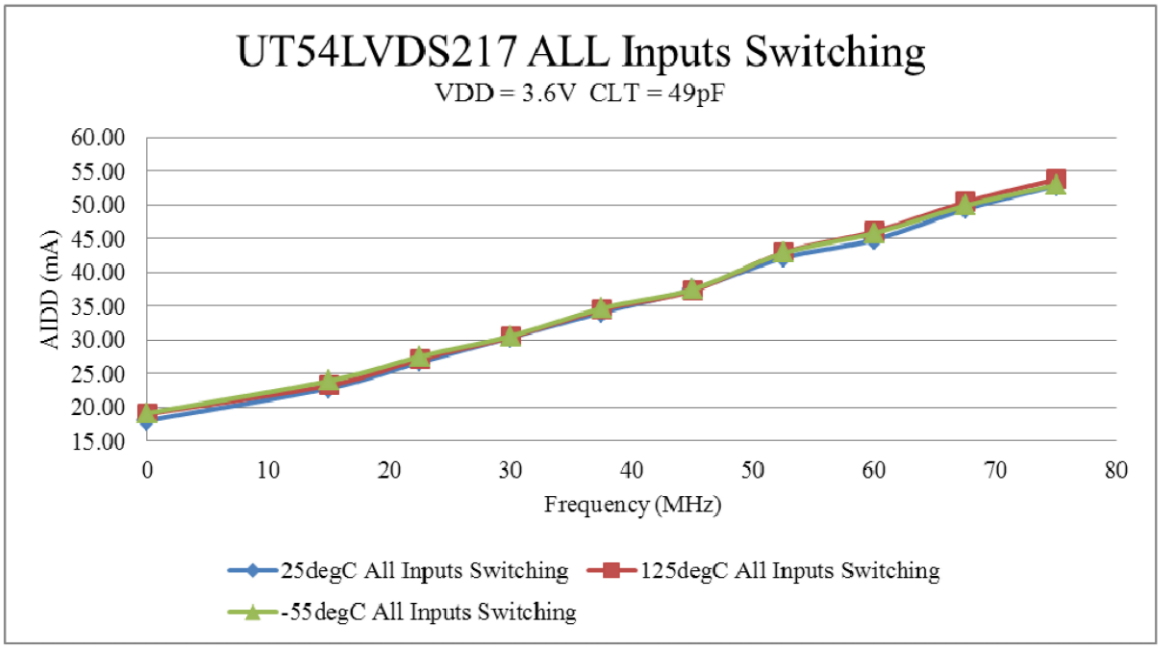

Figure 11. UT54LVDS217 Active current vs. Frequency for VDD = 3.6V, CLT = 49pF

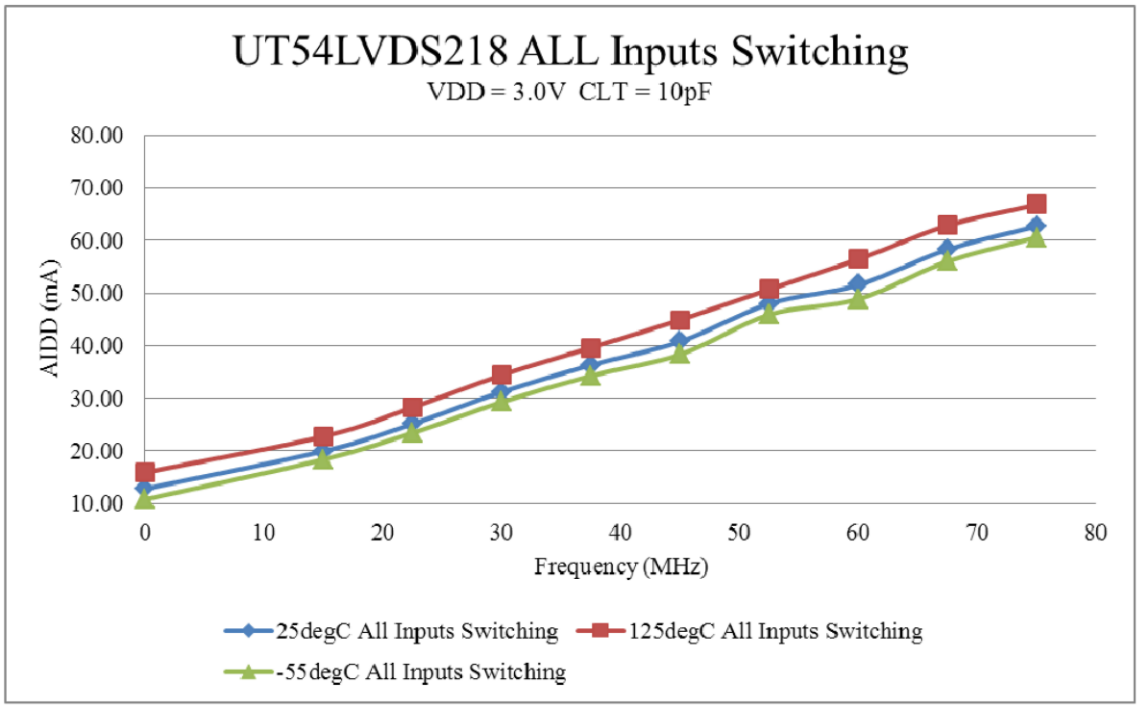

Figure 12. UT54LVDS217 Active current vs. Frequency for VDD = 3.6V, CLT = 49pF

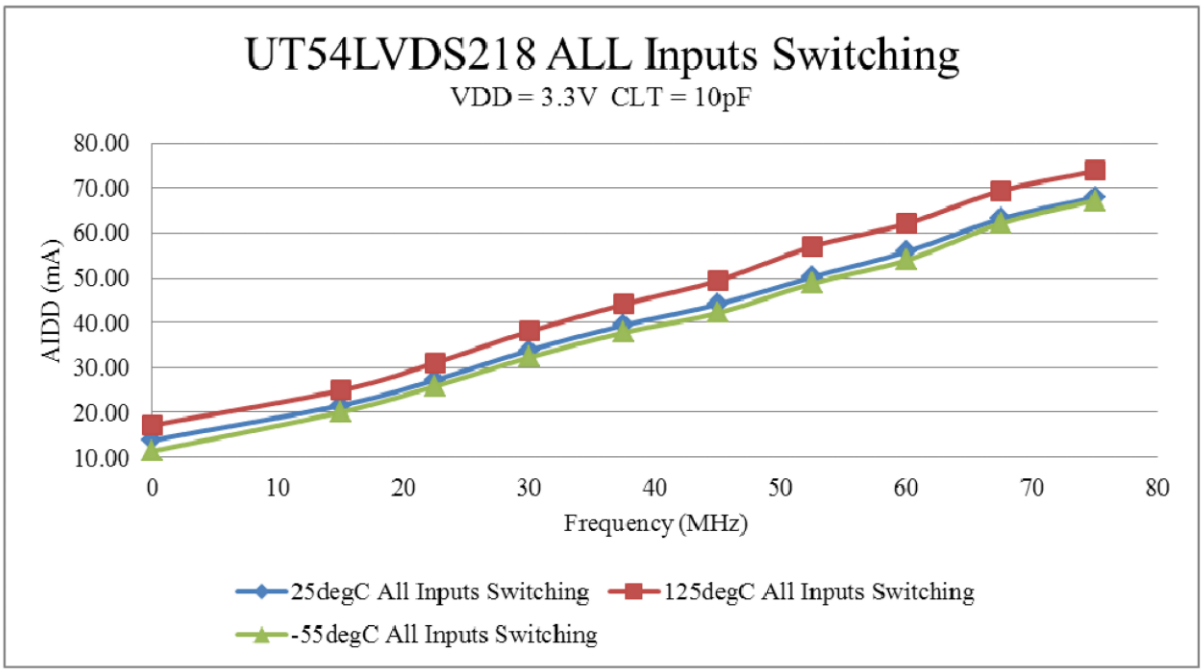

Figure 13. UT54LVDS218 Active current vs. Frequency for VDD = 3.3V, CLT = 10pF

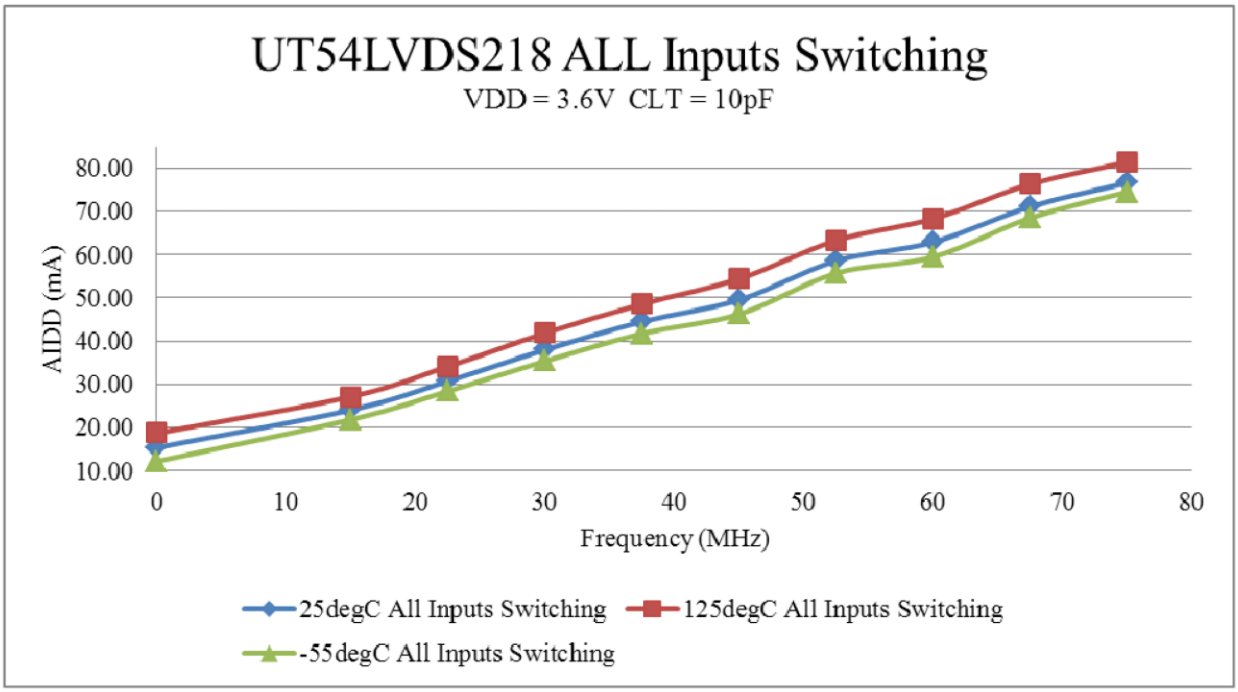

Figure 14. UT54LVDS218 Active current vs. Frequency for VDD = 3.6V, CLT = 10pF

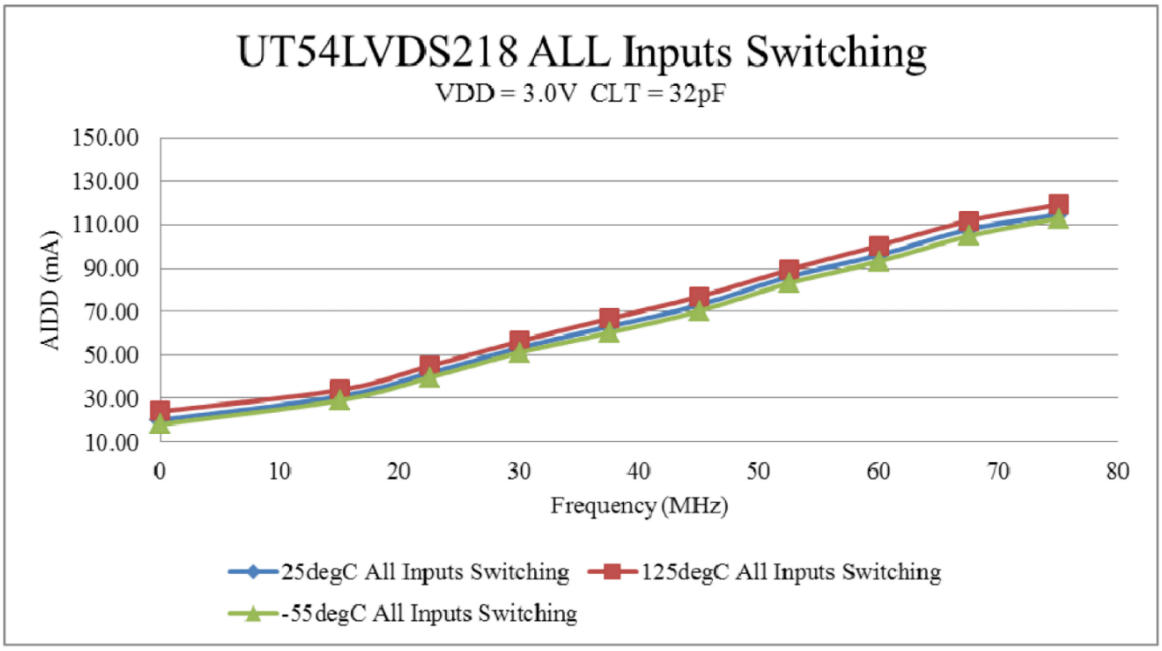

Figure 15. UT54LVDS218 Active current vs. Frequency for VDD = 3.0V, CLT = 32pF

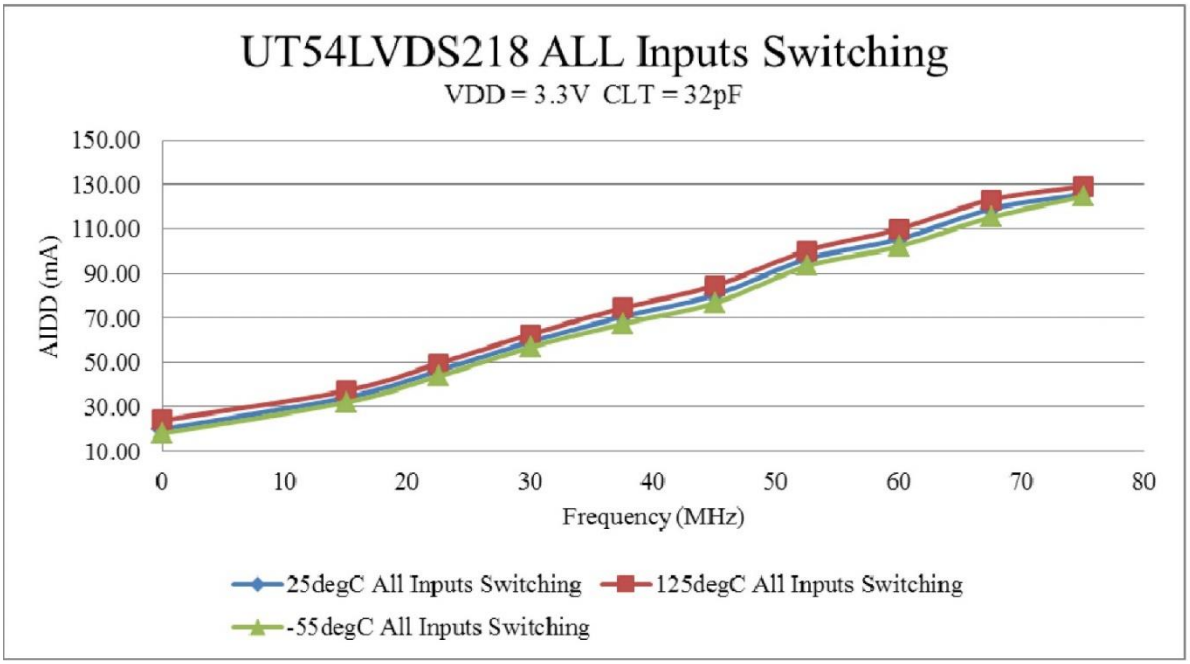

Figure 16. UT54LVDS218 Active current vs. Frequency for VDD 3.3V, CLT 32pF

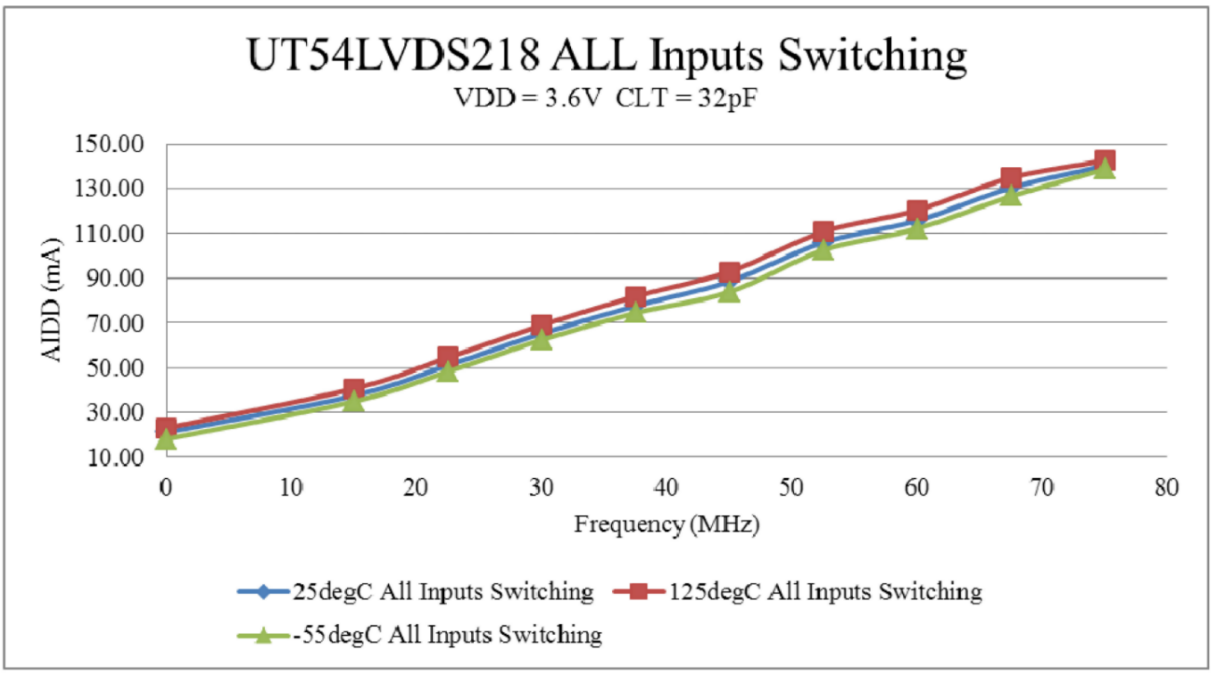

Figure 17. UT54LVDS218 Active current vs. Frequency for VDD = 3.6V, CLT = 32p

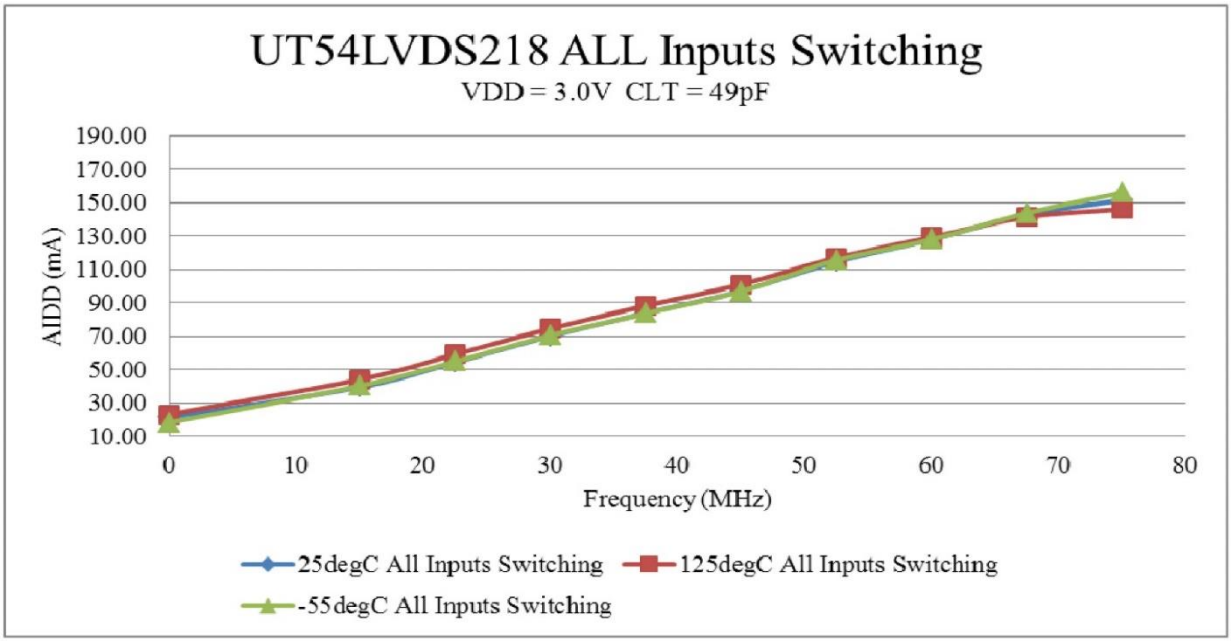

Figure 18. UT54LVDS218 Active current vs. Frequency for VDD = 3.0V, CLT = 49pF

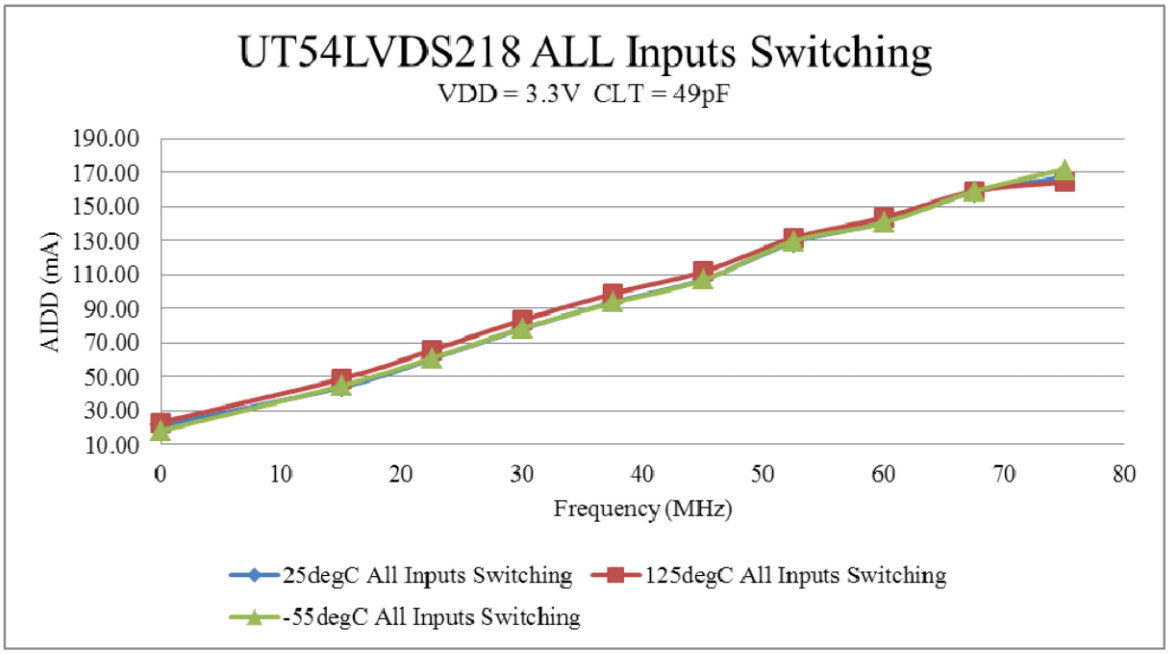

Figure 19. UT54LVDS218 Active current vs. Frequency for VDD = 3.3V, CLT = 49pF

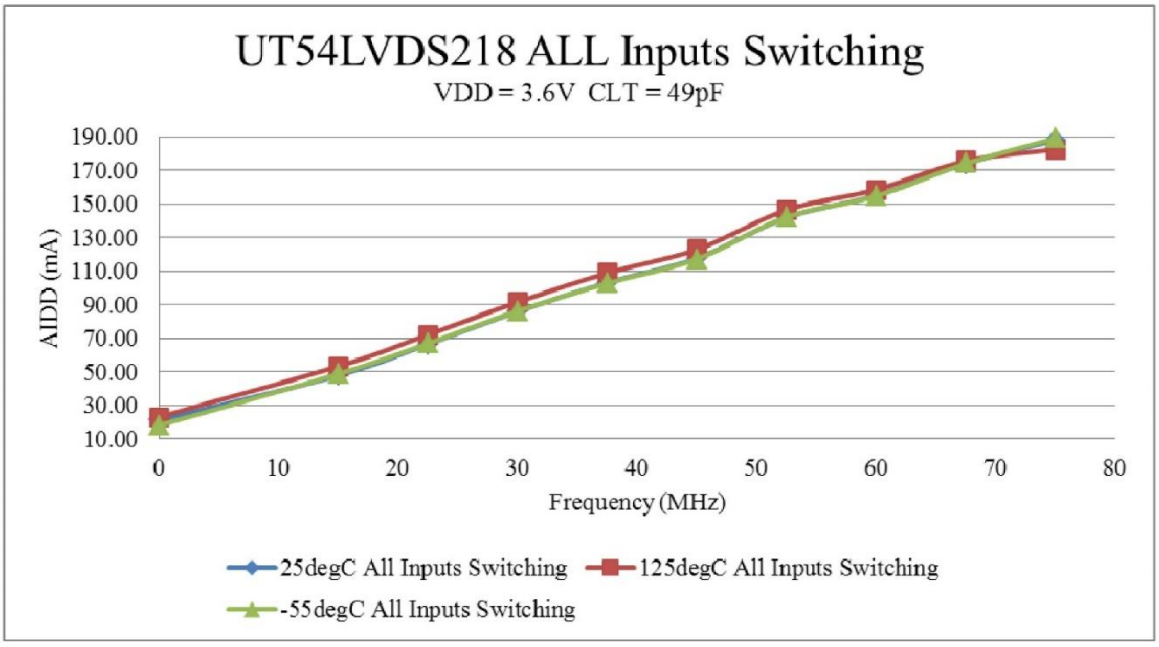

Figure 20. UT54LVDS218 Active current vs. Frequency for VDD 3.6V, CLT 49pF

Calculating of Power with Variable Load Capacitance

The structures of the UT54LVDS217 and UT54LVDS218 are such that there are three different clock domains. These clock domains make it difficult to accurately calculate power similar to AN-LVDS-002-NN. Therefore Frontgrade offers the active current (AIDD) characterization data to calculate power.

Device Power (P):

$P = AIDD*V_{DD}$

Example

Assume using the UT54LVDS217, switching all of the I/O, at a frequency of 60MHz, with a 10pF load, and with VDD set to nominal at a temperature of -55°C.

V_{DD} =3.3V Temp = -55°C

C_{LT} =10pF AIDD(estimate) = ~43mA

$P = AIDD*V_{DD}$ = 43.66mA*3.3V = 144.1mW

Conclusion

This application note empowers the designer to more accurately determine the power dissipation of Frontgrade LVDS SerDes products as implemented in the user's application. With accurate power dissipation improved power supply selection and thermal management schemes can be designed.

Additional Comments

Data contained in this application note is NOT GUARANTEED. The data is intended to provide system designers with better estimate of the UT54LVDS217 and UT54LVDS218 power dissipation.

To optimize power conservation tie unused driver inputs either high (VDD) or low (VSS), and leave unused outputs unconnected (no termination resistor connected, RT).

Leave unused receiver inputs floating, the unused input pins should be floated near the pin on the receiver device. There is a fail safe mode on the Frontgrade UT54LVDS218 Deserializer that forces the outputs to a high state. Unused inputs should not be connected to noise sources. Do not connect unused receiver input pins to a floating cable or trace because they will act as a noise antenna. Unused receiver outputs should be left unconnected to further power conservation.

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Revision History

Date	Revision #	Author	Change Description	Page #