FRONTGRADE

APPLICATION NOTE

1Gb/64Mb NOR Flash

Interfacing to GR740

09/1/2021

Version #: 1.0.0

Table 1: Cross Reference of Applicable Products

Product Name	Manufacturer Part Number	SMD #	Device Type
1 Gb SPI NOR Flash	UT81NFR1G1	5962-21210	All
1 Gb Parallel NOR Flash	UT81NFR128M8	5962-21209	All
64 Mb SPI NOR Flash	UT81NFR64M1	5962-21210	All
64 Mb Parallel NOR Flash	UT81NFR8M8	5962-21209	All

OVERVIEW

This Design Note provides the user with top-level information for interfacing the Frontgrade NOR Flash with the Frontgrade GR740 interfaces. This document includes the interface for booting the GR740 from the NOR Flash.

DESIGN IMPLEMENTATION (PARALLEL)

The UT81NFR128M8 and UT81NFR8M8 devices both have a single voltage supply that can operate at either 3.3 or 2.5 Volts. The GR740 I/O supply voltage recommended operating conditions for the PROM interface requires the use of 3.3 Volts.

2.1 Interface pin list

GR740 Pin Name	NOR Flash Pin Name	Functional Description
PROMIO_ADDR[26:0]	A[25:0], A-1	Address inputs (DQ[15] is A-1 in x8 mode)
PROMIO_OEN	OE#	Output enable
PROMIO_WEN	WE#	Write enable
PROM_CEN[0]	CE#	Chip enable
PROMIO_DATA[15:0]	DQ[15:0]	Data input/output
--	BYTE#	X16/x8 mode control
--	RESET#	Part Reset
--	RY/BY#	Device ready indicator
--	WP#	Write protect
--	PwrDN#	Part Power down (1Gb only)

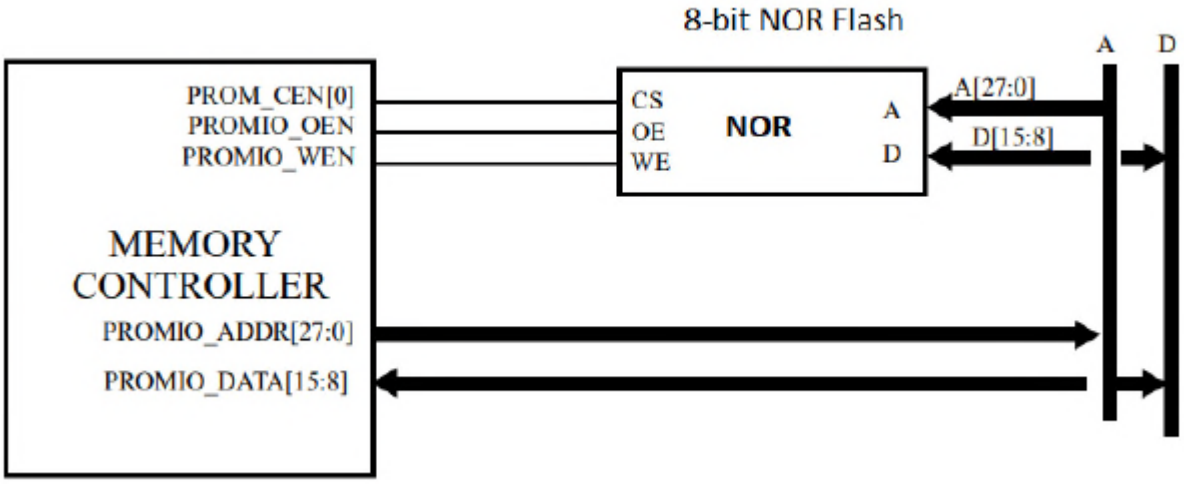

Figure 3: Basic Parallel NOR Flash to GR740 Connections (x8 interface)

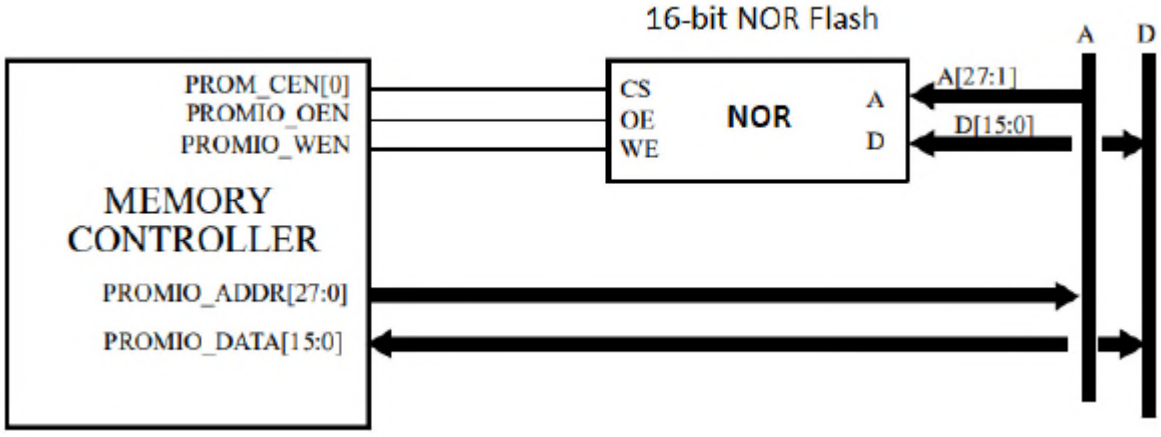

Figure 4: Basic Parallel NOR Flash to GR740 Connections (x16 interface)

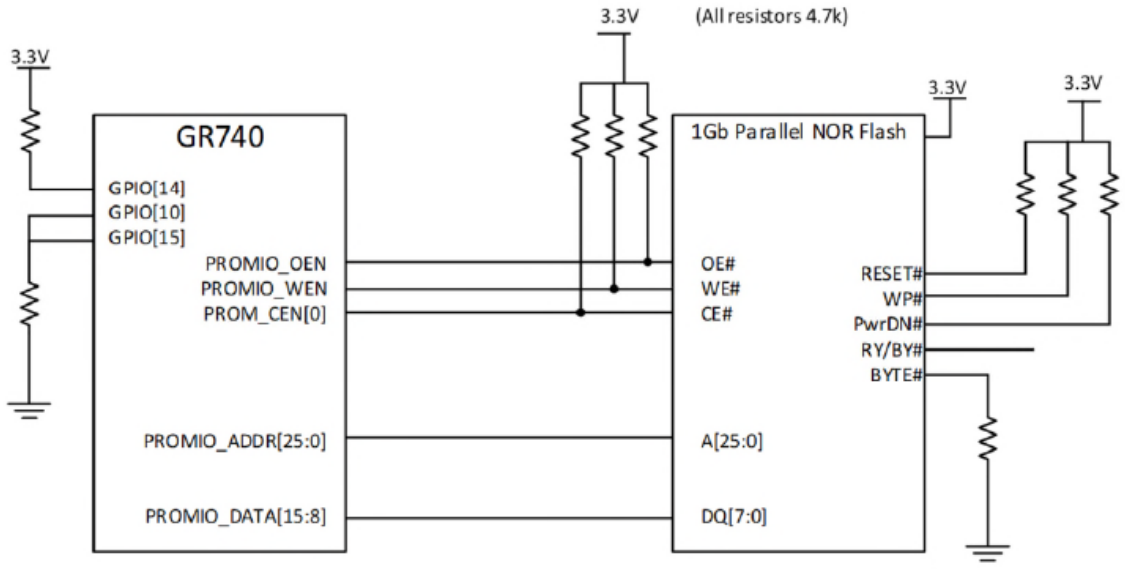

Figure 5: Boot Interface x8 Example

2.2 Setup

GR740 integrated EDAC protection is not available in 16-bit mode. GPIO[14] controls the reset value of the PROM/IO controller's PROM EDAC enable (PE) bit. When this input is '1' at reset, EDAC checking of the PROM area will be enabled. GPIO[15] selects if the PROM/IO interface should be enabled after reset. If this signal is LOW then the PROM/IO interface is enabled. Otherwise the PROM/IO interface pins are routed to their alternative functions per the GR740 datasheet.

It should be noted that checkbytes are stored at the upper 20% of the memory rendering only 80% of the memory useable in this mode. There is an application note about this EDAC mode referenced here: https://www.gaisler.com/doc/antn/GRLIB-AN-0003.pdf

A constraint on the number of available GPIO pins, it is preferred to leave the remaining control signals disconnected from the GR740. If the user wants to control the NOR flash further, it is recommended that an additional controller be included in the design such as the UT32M0R500 microcontroller.

DESIGN IMPLEMENTATION (SPI)

3.1 Interface pin list

GR716 Pin Name	NOR Flash Pin Name	Functional Description
SPI_MOSI	MOSI	NOR SPI Input
SPI_MISO	MISO	NOR SPI Output
SPI_SEL	SS#	Slave Select

GR716 Pin Name	NOR Flash Pin Name	Functional Description
SPI_SCK	SCLK	Serial Clock
--	WP#	Write Protect
--	RESET#	Part Reset
--	PwrDN#	Part Power Down

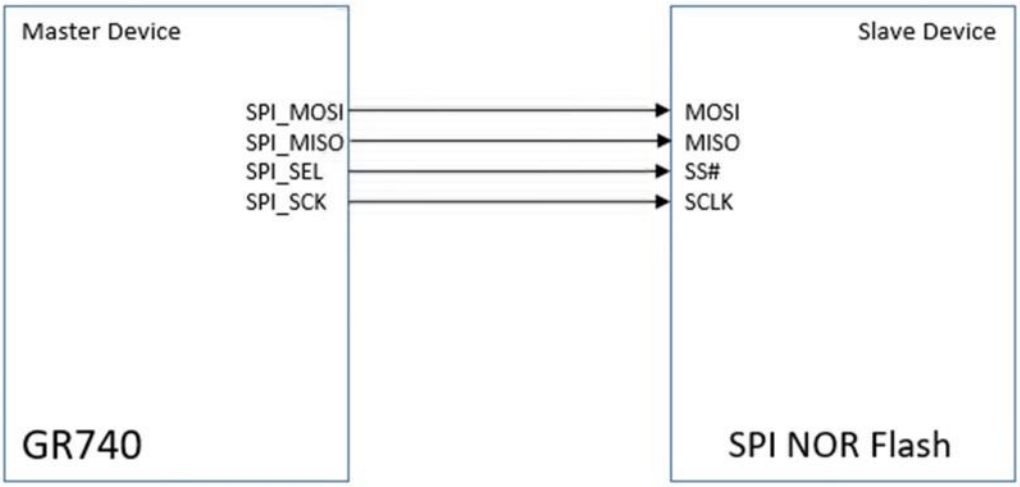

Figure 6: Basic SPI NOR Flash to GR740 Connections

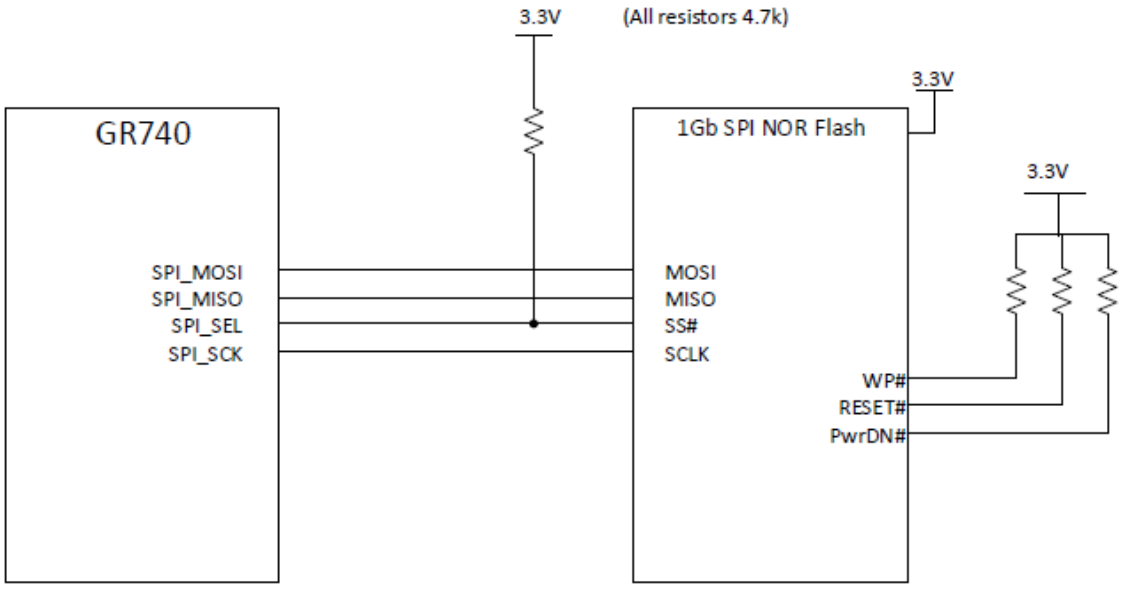

Figure 7: Master SPI Interface Mode Example

3.2 Setup

The SPI interface is not available for direct boot up operations on the GR740. Boot from SPI is available via the GRBOOT bootloader (https://www.gaisler.com/index.php/products/boot-loaders/grboot). This allows application software to be loaded from a SPI flash, but requires a parallel PROM to store the GRBOOT image. This small parallel PROM (typically EEPROM or MRAM) is used to store GRBOOT (only needs 24KiB of storage space), and the rest of the application image would be stored in the high-capacity SPI NOR-flash.

Reference the GR740 user manual for details on setting up the SPI operation. The SPI controller is clock gated at reset (section “4.9 Clock gating unit”) and must be enabled by software writing to the clock gating registers (chapter 25) before it can be used. The location of the SPI mode register is 0xFFA03020.

Revision History

Date	Revision #	Author	Change Description	Page #
09/2021			Initial Relase	