FRONTGRADE

APPLICATION NOTE

Calculating Power Dissipation for the 16-Bit Transceiver Family

3/1/2011

Version #: 1.0.0

Table 1: Cross Reference of Applicable Products

Product Name	Manufacturer Part Number	SMD #	Device Type	Internal PIC
MultiPurpose Transceiver with Cold Spare I/O	UT54ACS164245S/SE	5962-98580	01, 02, 03, 04, 05	JM01, JM03, JM04
MultiPurpose Transceiver with Cold/Warm Spare I/O	UT54ACS164245SEI	5962-98580	06, 07	JM06
MultiPurpose Registered Transceiver with Cold/Warm Spare I/O	UT54ACS164646S	5962-06234	01	KE01
MultiPurpose 3-Volt Transceiver with Cold/Warm Spare I/O	UT54ACS162245SLV	5962-02543	01	WA04,WA05

1.0 Overview

The Frontgrade 16-bit Logic family contains products such as the UT54ACS164245S/SE, UT54ACS164245SEI, UT54ACS164646S, and the UT54ACS162245SLV. These products perform functions such as: asynchronous two-way communication, Schmitt input buffering, voltage translation, multiplexed real-time and stored data, as well as cold and warm sparing.

This application note walks the designer through the calculations needed to determine power dissipation capacitance (C_{PD}) and power dissipation (PD) for the 16-bit Logic Family with user specific capacitive loads (CL).

2.0 Technical Figures and Data

Accurate power calculations are necessary to determine system power supply and thermal management requirements. The two primary components that determine the power consumption in a CMOS circuit are static and dynamic power. Static power is the power dissipated under DC conditions. Dynamic power consumption occurs when the device is switching capacitive loads.

Power consumption can be decreased by lowering supply voltage, reducing the capacitive load that the device has to drive, or lowering the devices operating frequency. Usually none of these reductions can be made without compromising system performance. It then becomes very important to be able to estimate the power requirements of the device.

From the device SMDs, power dissipation per switching output is offered as P_{total} = X mW/MHz with a tester load C_L = Y pF. SMD values enable the user to determine worst case power dissipation for the system. A power dissipation analysis can also determine the maximum reliable operating frequency of the device.

2.1 Characterization Data UT54ACS164245SEI

The following plots show active current, or AIDD, measurements versus frequency, over temperature and are used as input current for calculating power dissipation and power dissipation capacitance(C_{PD}). The AIDD values are from maximum measurements taken during characterization of numerous devices under the following conditions.

Temperature: T_C = 125°C, 25°C,-55°C

Voltage: VDD1 = VDD2 = 3.0V
VDD1 = VDD2 = 3.6V
VDD1 = VDD2 = 5.5V
VDD1 = 5.5V VDD2 = 3.6V

Frequency: ƒ = 10MHz, 25MHz, 50MHz

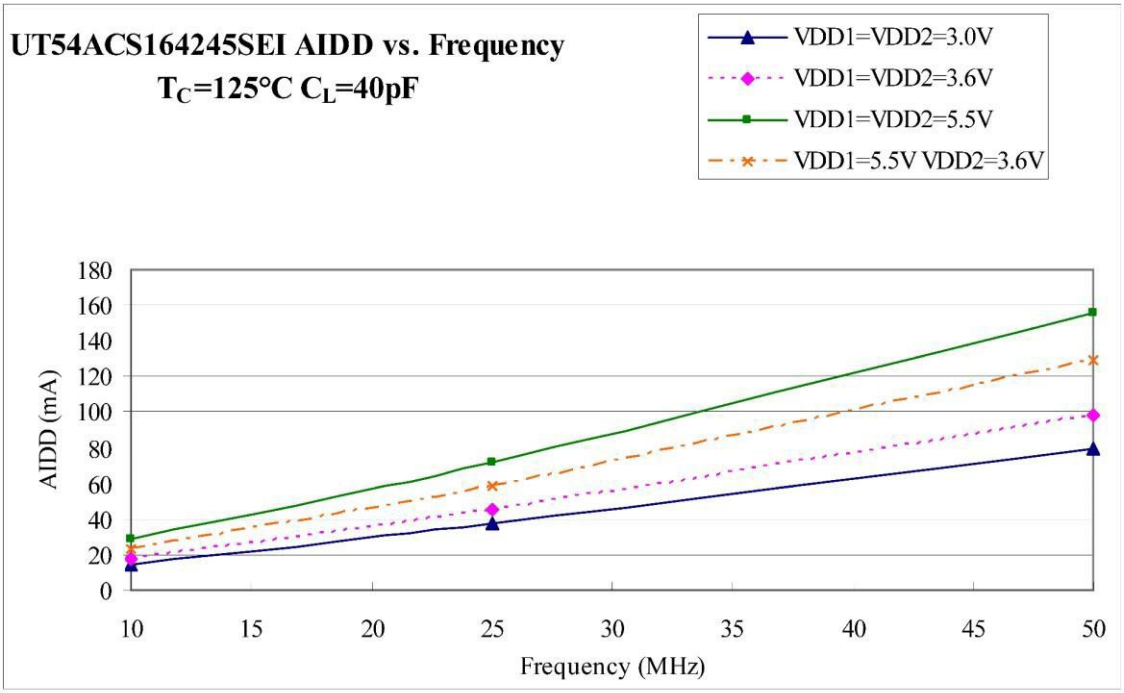

Figure 1. AIDD Values for 125°C with all 16 outputs switching

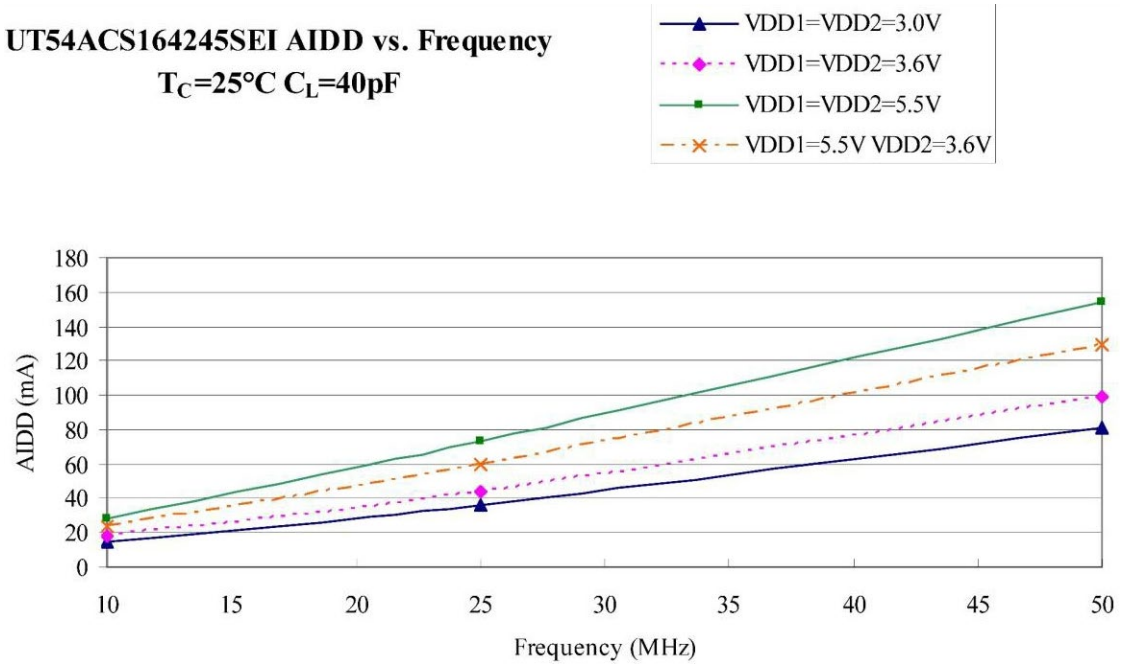

Figure 2. AIDD Values for 25°C with all 16 outputs switching

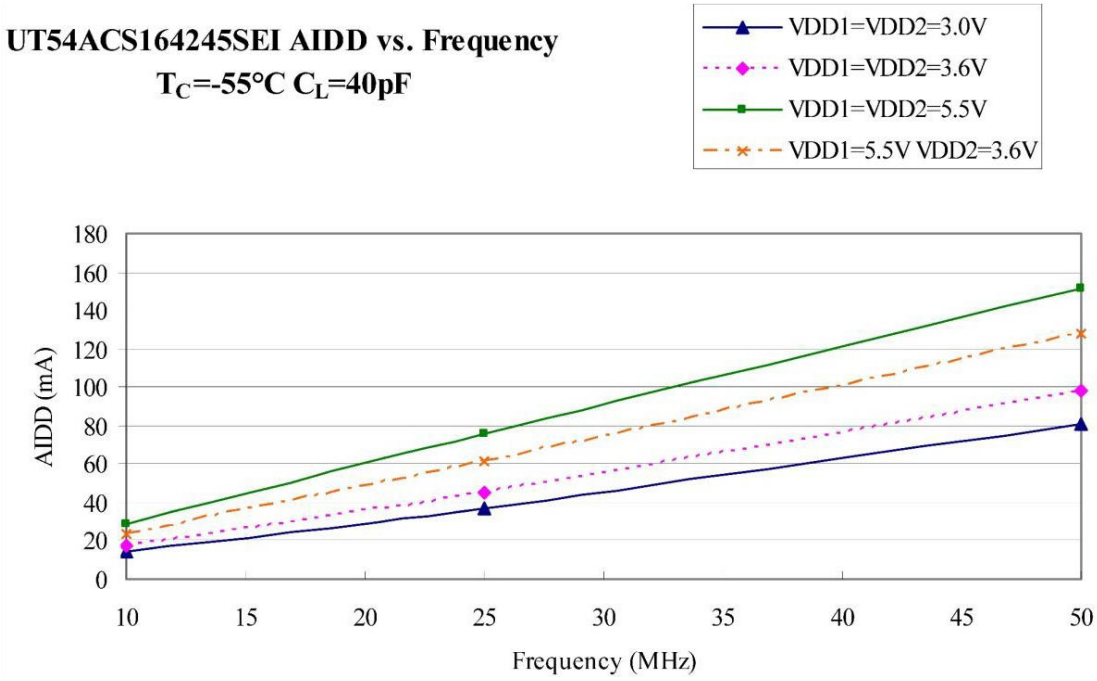

Figure 3. AIDD Values for -55°C with all 16 outputs switching

Using the AIDD graphs above (figures 1-3), or the data in tables 2 through 5 below, an estimate of the power supply current can be calculated by taking the slope of the line between two adjacent frequencies at a given temperature and multiplying by the designer's operating frequency. The values in the "Slope (mA/MHz)" column are the values for the power supply input current that will be used in determining the power dissipation and dynamic current consumption later in this application note.

Power dissipation capacitance or (C_{PD}) for the 16-Bit Logic Transceivers is calculated using equation 1 as follows. Since the outputs switch rail to rail V_{DD} = 3.3V or 5.0V, the capacitive load per switching output added by the automated tester (C_{LT}) must be accounted for. Calculations for C_{PD} are found in sections 3.0 and 4.0 of this application note.

Table 2. AIDD over frequency and temperature with VDD1 = VDD2 = 3.0V AIDD is listed for all 16 outputs switching, C_{PD} and C_{LT} are listed per switching output.

	T_C (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD1 = VDD2 = 3.0V C_{LT} = 40pF C_{PD} = 15.0pF	25	SIDD 0	12.62	
	25	10	14.41	
	25	25	36.08	1.45
	25	50	80.71	1.79
	-55	SIDD 0	12.71	
	-55	10	14.50	
	-55	25	36.45	1.46
	-55	50	81.29	1.79
	125	SIDD 0	13.21	
	125	10	14.89	
	125	25	37.11	1.48
	125	50	79.07	1.68

Table 3. AIDD over frequency and temperature with VDD1 = VDD2 = 3.6V AIDD is listed for all 16 outputs switching, C_{PD} and C_{LT} are listed per switching output.

	T_C (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD1 = VDD2 = 3.6V C_{LT} = 40pF C_{PD} = 15.0pF	25	SIDD 0	15.33	
	25	10	17.50	
	25	25	44.26	1.78
	25	50	98.55	2.17
	-55	SIDD 0	15.59	
	-55	10	17.71	
	-55	25	45.07	1.82
	-55	50	98.15	2.12
	125	SIDD 0	15.87	
	125	10	17.99	
	125	25	45.01	1.80
	125	50	97.99	2.12

Table 4. AIDD over frequency and temperature with VDD1 = 5.5V VDD2 = 3.6V AIDD is listed for all 16 outputs switching, C_{PD} and C_{LT} are listed per switching output.

	T_C (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD1 = 5.5V VDD2 = 3.6V C_{LT} = 40pF C_{PD} = 15.0pF	25	SIDD 0	20.49	
	25	10	23.29	
	25	25	59.12	2.39
	25	50	129.12	2.80
	-55	SIDD 0	21.04	
	-55	10	23.71	
	-55	25	60.97	2.48
	-55	50	127.58	2.66
	125	SIDD 0	20.92	
	125	10	23.71	
	125	25	58.95	2.35
	125	50	128.72	2.79

Table 5. AIDD over frequency and temperature with VDD1 = VDD2 = 5.5V AIDD is listed for all 16 outputs switching, C_{PD} and C_{LT} are listed per switching output.

	T_C (℃)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD1 = VDD2 = 5.5V C_{LT} = 40pF C_{PD} = 15.0pF	25	SIDD 0	25.18	
	25	10	28.43	
	25	25	72.74	2.95
	25	50	154.03	3.25
	-55	SIDD 0	26.06	
	-55	10	29.08	
	-55	25	75.42	3.09
	-55	50	150.94	3.02
	125	SIDD 0	25.36	
	125	10	28.74	
	125	25	71.78	2.87
	125	50	156.26	3.38

2.2 Characterization Data UT54ACS164245S/SE

Temperature: T_C = 125℃, 25℃,-55℃

Voltage: VDD1 = VDD2 = 3.0V

VDD1 = VDD2 = 3.6V

VDD1 = VDD2 = 5.5V

VDD1 = 5.5V VDD2 = 3.6V

Frequency: ƒ = 10MHz, 25MHz, 50MHz

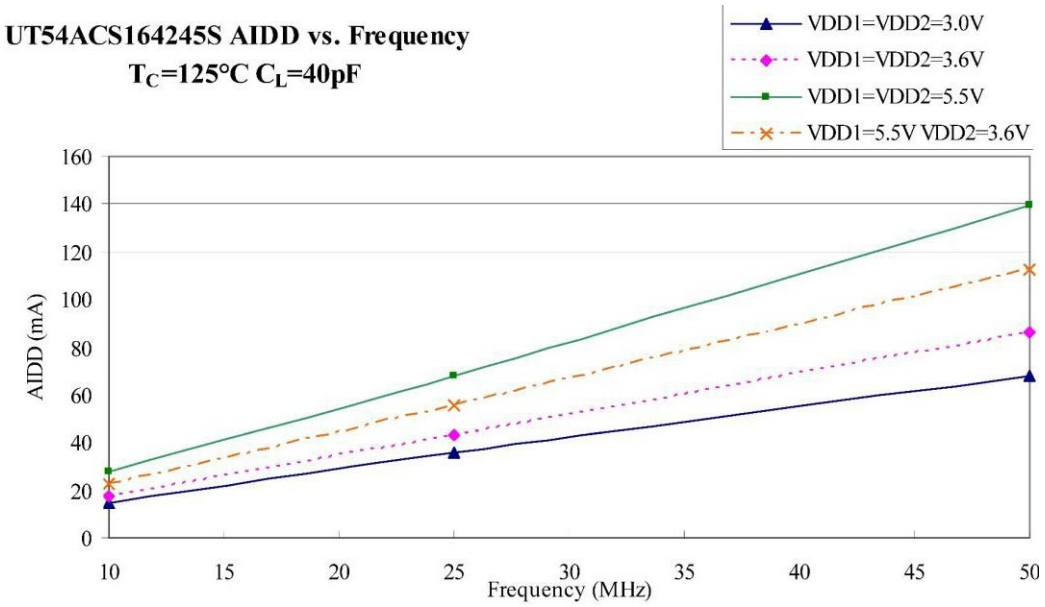

Figure 4. AIDD Values for 125°C with all 16 outputs switching

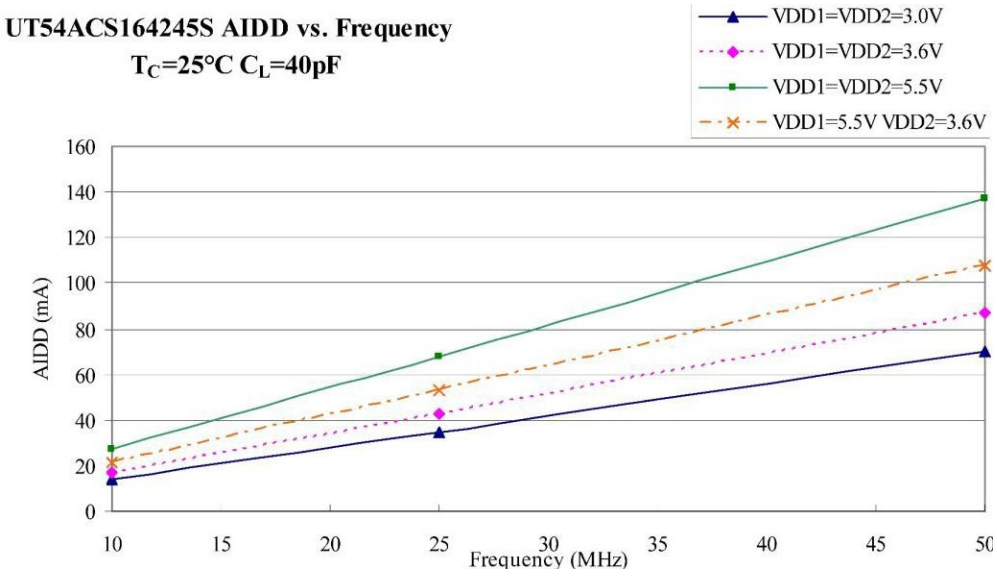

Figure 5. AIDD Values for 25°C with all 16 outputs switching

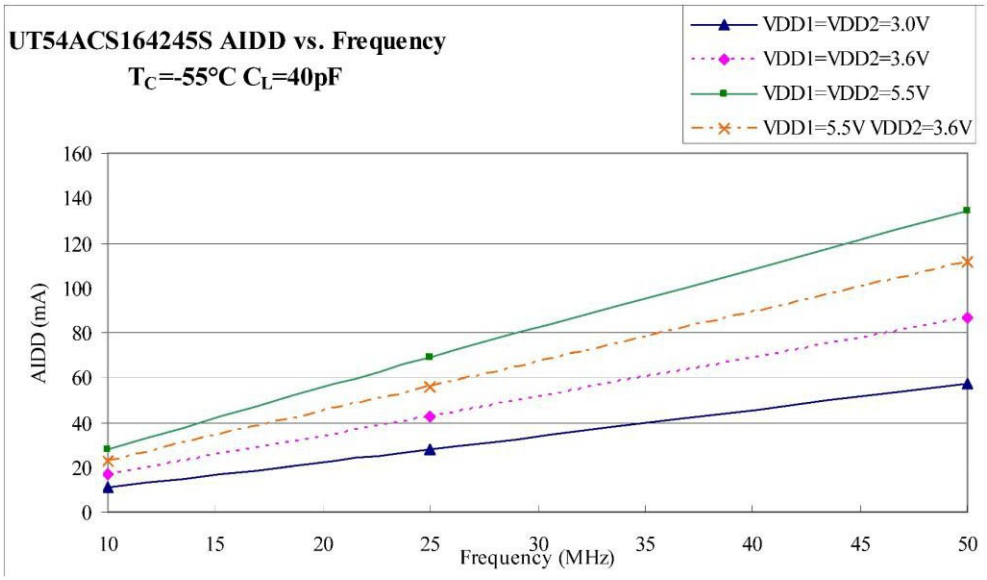

Figure 6. AIDD Values for -55°C with all 16 outputs switching

Table 6. AIDD over frequency and temperature with VDD1 = VDD2 = 3.0V AIDD is listed for all 16 outputs switching, C_{PD} and C_{LT} are listed per switching output.

	T_C (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD1 = VDD2 = 3.0V C_{LT} = 40pF C_{PD} = 15.0pF	25	SIDD 0	12.83	
	25	10	14.24	
	25	25	34.92	1.38
	25	50	70.29	1.41
	-55	SIDD 0	10.18	
	-55	10	11.36	
	-55	25	27.88	1.10
	-55	50	57.48	1.18
	125	SIDD 0	13.19	
	125	10	14.49	
	125	25	35.63	1.41
	125	50	67.95	1.29

Table 7. AIDD over frequency and temperature with VDD1 = VDD2 = 3.6V AIDD is listed for all 16 outputs switching, C_{PD} and C_{LT} are listed per switching output.

	T_C (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD1 = VDD2 = 3.6V C_{LT} = 40pF C_{PD} = 15.0pF	25	SIDD 0	15.52	
	25	10	17.30	
	25	25	42.48	1.67
	25	50	86.96	1.77
	25	SIDD 0	15.46	
	-55	10	17.24	
	-55	25	42.41	1.67
	-55	50	86.86	1.77
	125	SIDD 0	15.81	
	125	10	17.53	
	125	25	43.08	1.70
	125	50	86.11	1.72

Table 8. AIDD over frequency and temperature with VDD1 = 5.5V VDD2 = 3.6V AIDD is listed for all 16 outputs switching, C_{PD} and C_{LT} are listed per switching output.

	T_C (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD1 = 5.5V VDD2 = 3.6V C_{LT} = 40pF C_{PD} = 15.0pF	25	SIDD 0	19.38	
	25	10	21.56	
	25	25	52.96	2.09
	25	50	107.38	2.17
	-55	SIDD 0	20.32	
	-55	10	22.55	
	-55	25	55.52	2.19
	-55	50	111.36	2.23
	25	SIDD 0	20.25	
	125	10	22.54	
	125	25	55.31	2.18
	125	50	112.58	2.29

Table 9. AIDD over frequency and temperature with VDD1 = VDD2 = 3.0V AIDD is listed for all 16 outputs switching, C_{PD} and C_{LT} are listed per switching output.

	T_C (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD1 = VDD2 = 5.5V C_{LT} = 40pF C_{PD} = 15.0pF	25	SIDD 0	24.72	
	25	10	27.49	
	25	25	67.79	2.68
	25	50	136.92	2.76
	-55	SIDD 0	25.12	
	-55	10	27.74	
	-55	25	68.78	2.73
	-55	50	134.33	2.62
	25	SIDD 0	24.65	
	125	10	27.52	
	125	25	67.84	2.68
	125	50	139.5	2.86

2.1 Characterization Data UT54ACS164646S

Temperature: T_C = 125°C, 25°C,-55°C

Voltage: VDD1 = VDD2 = 3.0V

VDD1 = VDD2 = 3.6V

VDD1 = VDD2 = 5.5V

VDD1 = 5.5V VDD2 = 3.6V

Frequency: ƒ = 10MHz, 25MHz, 50MHz

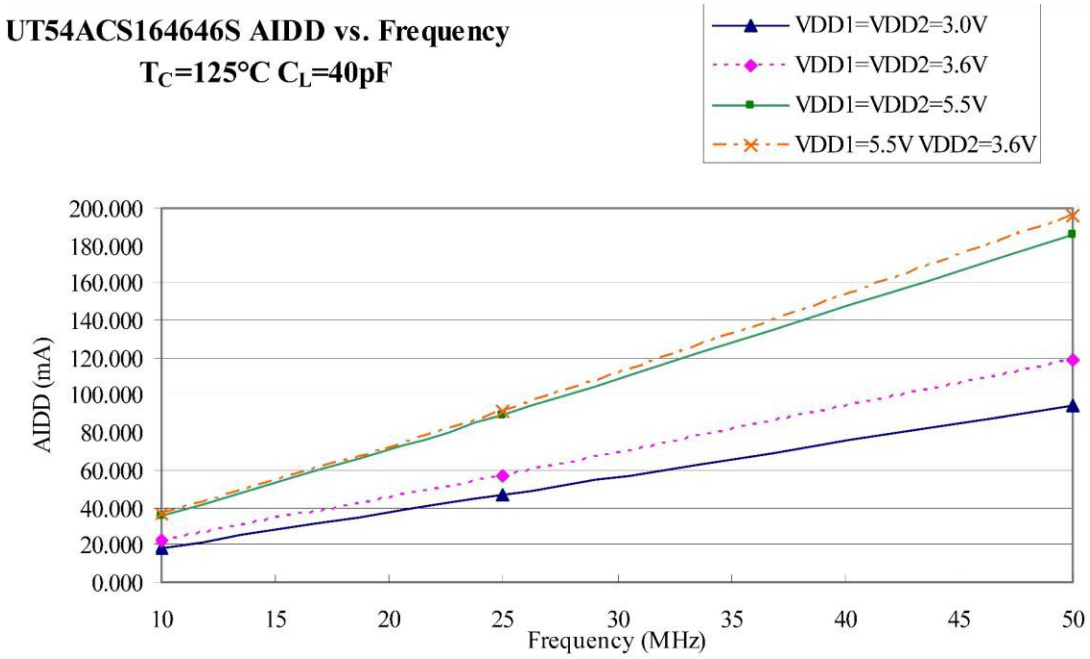

Figure 7. AIDD Values for 125°C with all 16 outputs switching

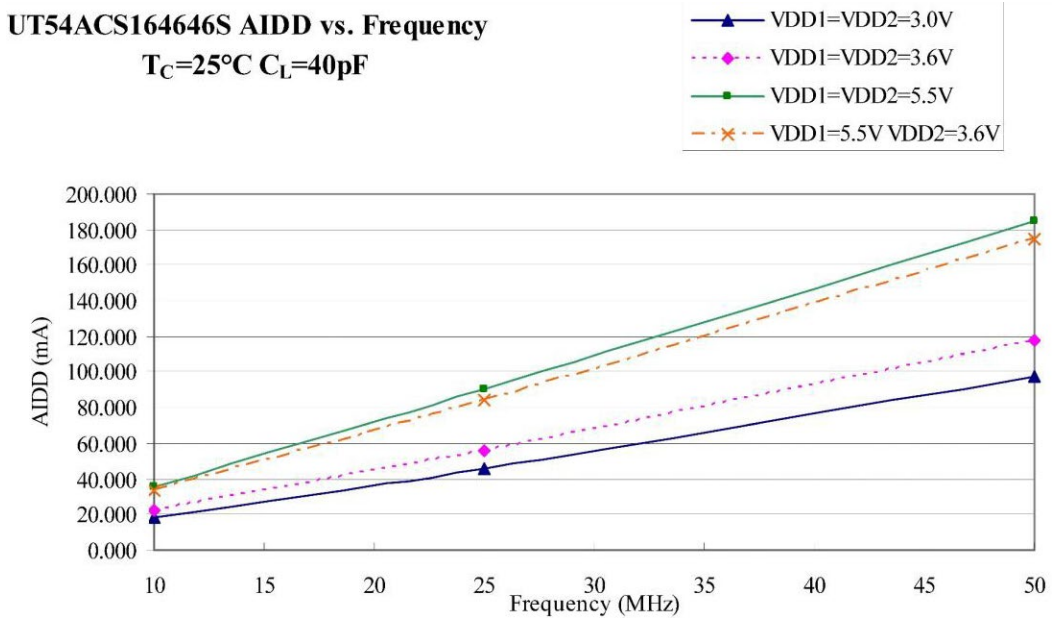

Figure 8. AIDD Values for 25°C with all 16 outputs switching

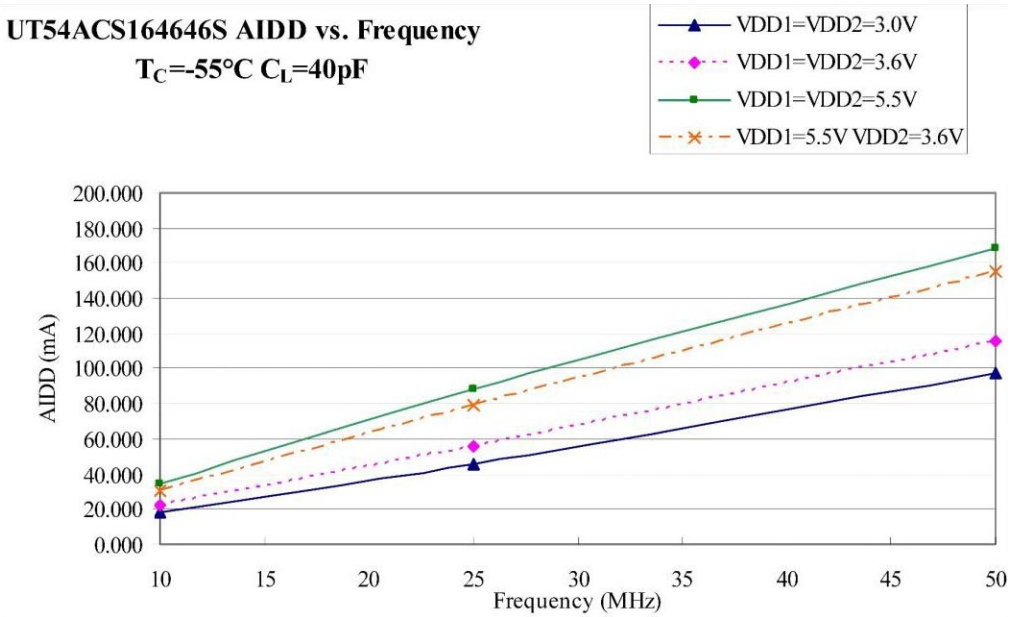

Figure 9. AIDD Values for -55°C with all 16 outputs switching

Table 10. AIDD over frequency and temperature with VDD1 = VDD2 = 3.0V AIDD is listed for all 16 outputs switching, C_{PD} and C_{LT} are listed per switching output.

	T_C (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD1 = VDD2 = 3.0V C_{LT} = 40pF C_{PD} = 15.0pF	25	SIDD 0	16.29	
	25	10	18.34	
	25	25	45.76	1.82
	25	50	97.10	2.05
	-55	SIDD 0	16.07	
	-55	10	18.13	
	-55	25	45.86	1.84
	-55	50	97.21	2.05
	125	SIDD 0	16.82	
	125	10	18.75	
	125	25	46.54	1.85
	125	50	94.73	1.92

Table 11. AIDD over frequency and temperature with VDD1 = VDD2 = 3.6V AIDD is listed for all 16 outputs switching, C_{PD} and C_{LT} are listed per switching output.

	T_C (℃)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD1 = VDD2 = 3.6V C_{LT} = 40pF C_{PD} = 15.0pF	25	SIDD 0	19.80	
	25	10	22.29	
	25	25	55.86	2.23
	25	50	118.14	2.49
	-55	SIDD 0	19.62	
	-55	10	22.01	
	-55	25	55.95	2.26
	-55	50	115.62	2.38
	125	SIDD 0	20.26	
	125	10	22.73	
	125	25	56.50	2.25
	125	50	118.41	2.47

Table 12. AIDD over frequency and temperature with VDD1 = 5.5V VDD2 = 3.6V AIDD is listed for all 16 outputs switching, C_{PD} and C_{LT} are listed per switching output.

	T_C (℃)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD1 = 5.5V VDD2 = 3.6V C_{LT} = 40pF C_{PD} = 15.0pF	25	SIDD 0	29.54	
	25	10	33.15	
	25	25	83.88	3.38
	25	50	174.21	3.61
	-55	SIDD 0	27.83	
	-55	10	30.92	
	-55	25	78.69	3.18
	-55	50	155.83	3.08
	125	SIDD 0	32.60	
	125	10	36.77	
	125	25	91.75	3.66
	125	50	195.92	4.16

Table 13. AIDD over frequency and temperature with VDD1 = VDD2 = 5.5V AIDD is listed for all 16 outputs switching, C_{PD} and C_{LT} are listed per switching output.

	T_C (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD1 = VDD2 = 5.5V C_{LT} = 40pF C_{PD} = 15.0pF	25	SIDD 0	31.80	
	25	10	35.59	
	25	25	90.03	3.62
	25	50	184.77	3.79
	-55	SIDD 0	31.74	
	-55	10	34.97	
	-55	25	88.15	3.54
	-55	50	168.99	3.23
	125	SIDD 0	31.85	
	125	10	35.72	
	125	25	88.98	3.55
	125	50	185.59	3.86

2.2 Characterization Data UT54ACS162245SLV

Temperature: T_C = 125°C, 25°C,-55°C

Voltage: VDD1 = VDD2 = 3.0V
VDD1 = VDD2 = 3.6V
VDD1 = VDD2 = 2.3V
VDD1 = 3.6V VDD2 = 2.7V

Frequency: ƒ = 10MHz, 25MHz, 50MHz

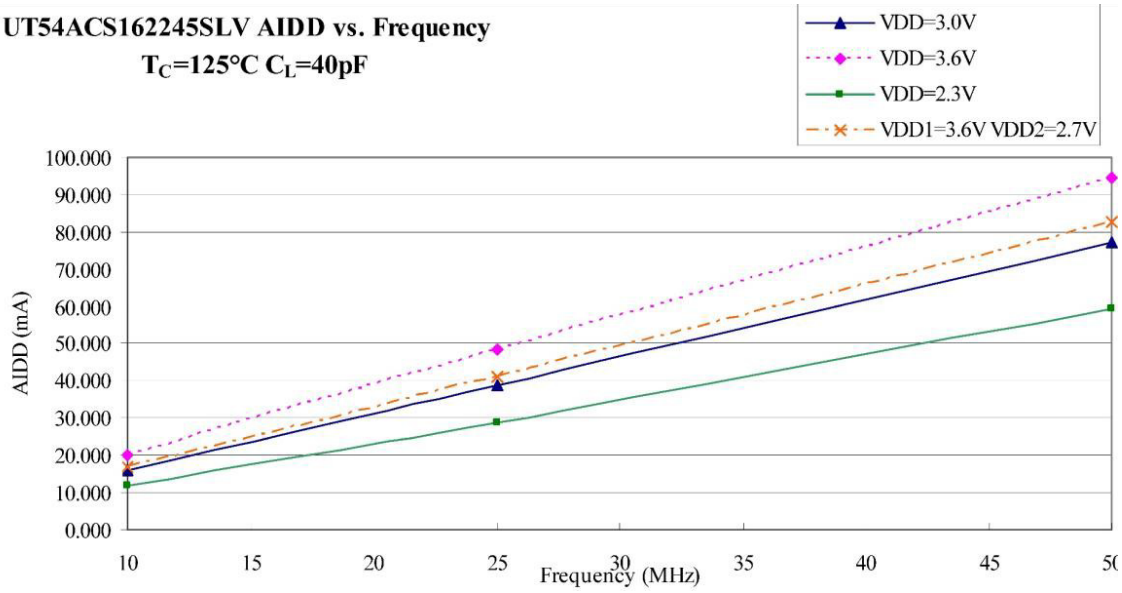

Figure 10. AIDD Values for 125°C with all 16 outputs switching

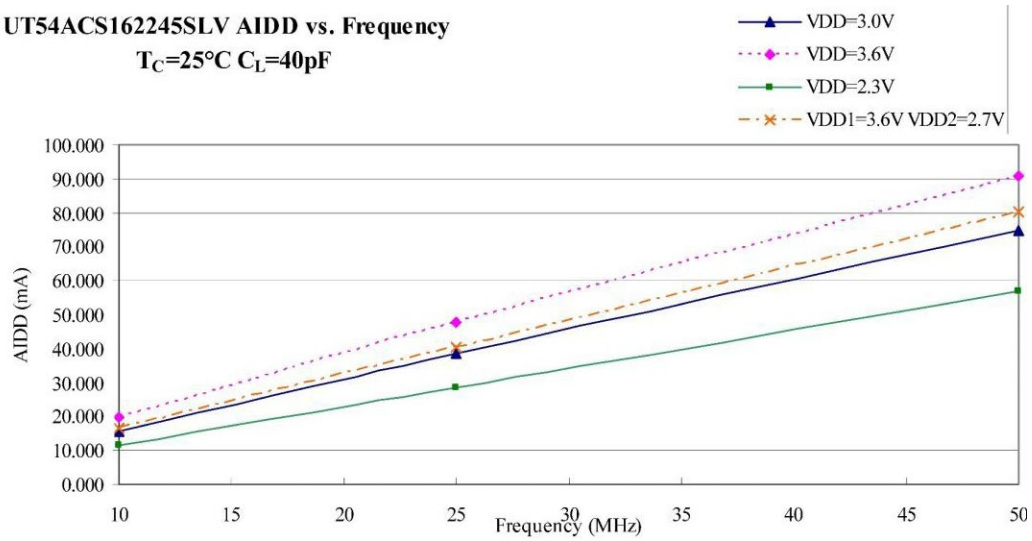

Figure 11. AIDD Values for 25°C with all 16 outputs switching

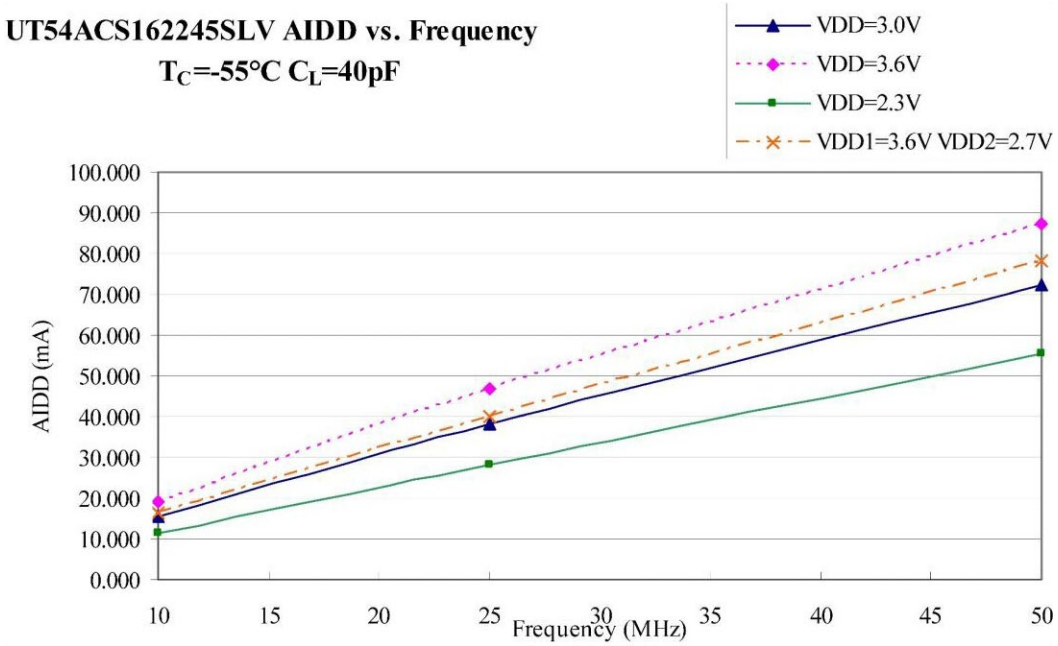

Figure 12. AIDD Values for -55°C with all 16 outputs switching

Table 14. AIDD over frequency and temperature with VDD1 = VDD2 = 3.0V AIDD is listed for all 16 outputs switching, C_{PD} and C_{LT} are listed per switching output.

	T_C (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD1 = VDD2 = 3.0V C_{LT} = 40pF C_{PD} = 15.0pF	25	SIDD 0	14.14	
	25	10	15.61	
	25	25	38.34	1.51
	25	50	74.97	1.46
	-55	SIDD 0	14.16	
	-55	10	15.53	
	-55	25	38.01	1.49
	-55	50	72.34	1.37
	125	SIDD 0	14.40	
	125	10	15.94	
	125	25	38.94	1.53
	125	50	77.29	1.53

Table 15. AIDD over frequency and temperature with VDD1 = VDD2 = 3.6V AIDD is listed for all 16 outputs switching, C_{PD} and C_{LT} are listed per switching output.

	T_C (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD1 = VDD2 = 3.6V C_{LT} = 40pF C_{PD} = 15.0pF	25	SIDD 0	17.82	
	25	10	19.54	
	25	25	47.72	1.87
	25	50	90.95	1.72
	-55	SIDD 0	17.64	
	-55	10	19.26	
	-55	25	46.98	1.84
	-55	50	87.46	1.61
	125	SIDD 0	18.15	
	125	10	19.99	
	125	25	48.52	1.90
	125	50	94.64	1.84

Table 16. AIDD over frequency and temperature with VDD1 = 3.6 VDD2 = 2.7V AIDD is listed for all 16 outputs switching, C_{PD} and C_{LT} are listed per switching output.

	T_C (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD1 = 3.6V VDD2 = 2.7V C_{LT} = 40pF C_{PD} = 15.0pF	25	SIDD 0	14.97	
	25	10	16.56	
	25	25	40.48	1.59
	25	50	80.20	1.58
	-55	SIDD 0	14.89	
	-55	10	16.42	
	-55	25	40.08	1.57
	-55	50	78.23	1.52
	125	SIDD 0	15.34	
	125	10	17.00	
	125	25	41.17	1.61
	125	50	82.82	1.66

Table 17. AIDD over frequency and temperature with VDD1 = VDD2 = 2.3V AIDD is listed for all 16 outputs switching, C_{PD} and C_{LT} are listed per switching output.

	T_C (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD1 = VDD2 = 2.3V C_{LT} = 40pF C_{PD} = 15.0pF	25	SIDD 0	10.45	
	25	10	11.58	
	25	25	28.49	1.12
	25	50	56.86	1.13
	-55	SIDD 0	10.34	
	-55	10	11.45	
	-55	25	28.21	1.11
	-55	50	55.43	1.08
	125	SIDD 0	10.53	
	125	10	11.76	
	125	25	28.82	1.13
	125	50	59.38	1.22

3.0 Calculating of Power with Variable Load Capacitance

The following equations and examples are provided as a guide for estimating power dissipation, power dissipation capacitance, and dynamic current consumption using various capacitive loads.

Definition of Terms:

V_{DD1} [1]	Port B Power Supply Voltage (V)
V_{DD2} [1]	Port A Power Supply Voltage (V)
V_{OL}	Low-level output voltage (V)
V_{OL}(actual)	Load Dependent Low-level output voltage (V) VOH High-level output voltage (V)
V_{OH}(actual)	Load Dependent High-level output voltage (V)
AIDD	Active Supply Current with all 16 Outputs Switching (mA)
AIDD(slope)	Slope of AIDD (mA/MHz) AIDD(frequency) Active current at given frequency (mA)
SIDD	Standby Current Device Enabled ƒ =0MHz (mA)
I_{OL}	Low level output current (mA)
I_{OH}	High level output current (mA)
I_{SD}	Dynamic Current Consumption (A)
P_{DCL}	Percent Duty Cycle Driving Logic Low (%)
P_{DCH}	Percent Duty Cycle Driving Logic High (%)
C_{PD}	Power Dissipation Capacitance (F)
C_L	Users Load Capacitance (F)
C_{LT}	Capacitive per switching output Tester Load (F)
ƒ	Input Frequency (Hz)
P_{SWO}	Power per Switching Output (W/MHz per output)
P_{ST}	Static Power Dissipation (W)
P_{DYN}	Dynamic Power Dissipation (W)
P_{RLOAD}	Resistive Load Output Power (W)
P_{TOTAL}	Total Power Dissipation (W)
N_O	Number of switching outputs
N_{16}	Number of outputs on the 16-bit Device

Notes:

1. The 16-bit transceiver devices are running at different supply voltages use the supply voltage that corresponds to the bidirect pins configured as outputs when using the equations provided in section 3.0.
   - Meaning if a calculation is being performed on the UT54ACS162245SLV device and VDD1=3.6V, VDD2 = 2.7V, and DIR1 = DIR2 = HIGH (meaning the device is in A data to B Bus), VDD1 = 3.6V would need to be used as the VDD terms in the section 3.0 equations
   - Another example if a calculation is being performed on the UT54ACS164245SEI device and VDD1=5.5V, VDD2 = 3.6V, and DIR1 = DIR2 = LOW (meaning the device is in B data to A Bus), VDD2 = 3.6V would need to be used as the VDD terms in the section 3.0 equations

Two methods are offered to calculate Power/MHz. The first method simply employs Joule's law(P = IV), the power supply current, and voltage measured under a specific test condition. Method 1 offers a validation to the values that are then calculated using method 2. Method 2 contains terms like C_{PD}, C_L, ƒ, and V_{DD}, all of which can be varied by the designer in predicting power for a specific application.

Power per Switching Output (P_{SWO}):

$$PSWO = \frac{VDD * AIDD\ (frequency)}{N_{16}} \quad (1)$$

Static Device Power (P_{ST}):

$$P_{ST} = SIDD * V_{DD} \quad (2)$$

Dynamic Device Power per Switching Output (P_{DYN}):

$$P_{DYN} = (C_{PD}(V_{DD}{}^2 * ƒ)) + (C_L(V_{OH}(actual) — V_{OL}(actual))^2 * ƒ) \quad (3)$$

Resistive Output Load Power (P_{LOAD})

$$P_{LOAD} = [(P_{DCL} * V_{OL} * I_{OL}) + (P_{DCH} * (V_{DD} — V_{OH}) * |I_{OH}|)] \quad (4)$$

Total Device Power (P_{TOTAL}):

$$P_{TOTAL} = P_{ST} + (N_O (P_{DYN} + P_{LOAD})) \quad (5)$$

Active Current at frequency (AIDD(frequency)):

$$AIDD(frequency) = [(ƒ — ƒ\ @known\ AIDD) * AIDD(slope)] + AIDD@known\ ƒ \quad (6)$$

$$C_{PD} = \frac{Average\ (AIDD\ (slope))}{VDD} — (N_{16} * C_{LT}) \quad (7)$$

4.0 Example Calculations

The following sections walk the designer through example calculations using data and equations presented in sections 2.0 and 3.0.

4.1 Example 1

The C_{PD} value in Table 2 calculates using equation (7).

$$C_{PD} = \frac{\text{Average (AIDD(slope))}}{V_{DD}} — (N_{16} * C_{LT})$$

Where:

V_{DD}	Maximum Users Power Supply Voltage (V)
AIDD(slope)	Slope of AIDD (mA/MHz)
C_{PD}	Power Dissipation Capacitance (F)
C_{LT}	Capacitive per switching output Tester Load (F)
N_{16}	Number of outputs on the 16-bit Device

$$C_{PD}(\text{total}) = \frac{\text{Average(AIDD (slope))}}{V_{DD}} — (N_{16}*C_{LT}) =$$

$$\frac{\text{Average(1.44,1.785,1.463,1.793,1.481.1.679)}}{3.0} — (16 * 40\text{ pF}) = 103.9\text{ pF}$$

Total power dissipation capacitance is not useful for further calculations. For meaningful calculations one must compute power dissipation capacitance per output.

$$C_{PD}\text{ (per switching output)} = \frac{\text{CPD (total)}}{\text{N16}} = \frac{103.9\text{ pF}}{16} = 6.49\text{ pF Per Switching Output}$$

4.5 Example 2

The UT54ACS164245SEI analysis assumes the following: utilization of 8 outputs switching at 20MHz with 80pF capacitive loads, VDD1 = VDD2 = 3.0V, 512.5Ω pull up to VDD on the output, at 25℃. A bias resistor is present on the output to pull up the outputs are in Z state. In practice, the bias resistor will be defined by the system designer.

Referencing tables 1-4, power supply current is found by estimating the slope of the line at various temperatures. The values in the "Slope (mA/MHz)" column are the values for the power supply input current that will be used in determining the power dissipation and dynamic current consumption.

$V_{DD1} = V_{DD2} = V_{DD} = 3.0V$
$T_C = 25°C$
$C_{LT} = 40pF$ / output
$C_{PD} = 6.49$ pF
$C_L = 80$ pF (users load)
AIDD(slope) = 1.45mA / MHz (Table 2)
SIDD = 12.62mA
$N_O = 8$outputs
ƒ = 20 MHz
$P_{DCL} = 0.5$
$P_{DCH} = 0.5$
$V_{OH} = V_{DD} = 0.2 = 3.0V — 0.2V = 2.8V$ at $I_{OH} = 100$ A
V_{OH}(actual) = 3.0V Assume no bias resistors output swinging rail to rail
V_{OL} =0.2V at $I_{OL} = 100\mu A$
V_{OL}(actual) = V_{DD} — (512.5Ω * I_{OL}) = 3.0V — 2.5V = 0.44V at I_{OL} = 5.0mA

4.2.1 Method 1:

For these conditions power per switching output (PSWO) calculates using equations (1) and (6):

To calculate the active current at 20MHz using Joule's law (P=IV):
See Table 2 T_C=25℃

$$I = \frac{((AIDD(slope)) * ƒ)}{N_{16}} = \frac{(1.45mA / MHz * 20MHz)}{16} = 1.81mA / output\ 16$$

$P_{Joule's} = N_O(I * V) + (SIDD * V) = 8outputs * (1.81\ mA * 3.0V) + (12.62 * 3.0V) = 81.36mW$ for 8 outputs switching

AIDD(frequency) = [(ƒ — ƒ @known AIDD) * AIDD(slope)] + AIDD@known ƒ = [(20MHz — 10MHz) * 1.45mA / MHz] + 14.41mA = [14.45] + 14.41 = 28.91mA

$$P_{SWO} = \frac{VDD * AIDD(frequency)}{N_{16}} = \frac{3.0V * 28.91mA}{16} = 5.42\ mW / per\ output$$

P_{TOTAL}(method1) = (SIDD * V_{DD}) + (P_{SWO} * N_O) = (12.62mA * 3.0V) + (5.42MW / output * 8 outputs) = 81.23mW

4.2.2 Method 2:

Using equation (2) for calculating Static Device Power (P_{ST}):

P_{ST} = SIDD * V_{DD} = 12.62mA * 3.0V = 37.86mW

Dynamic Device Power per Switching Output (P_{DYN}):

$P_{DYN} = (C_{PD} (V_{DD}{}^2 * f)) + (C_L(V_{OH}(actual) — V_{OL} (actual))^2 * f) = (6.49\ pF(3.0V^2 * 20MHz)) + (80pF((3.0V — 0.44V)^2 * 20MHz)) = 11.65mW$

Resistive Output Load Power (P_{LOAD}):

$P_{LOAD} = [(P_{DCL} * V_{OL} * I_{OL}) + (P_{DCH} * (V_{DD} — V_{OH}) * | IOH |)] = [(0.5 * 0.5V * 8.0mA) + (0.5 * (3.0V — 3.0V)* |100\mu A|)] = 2.0mW + 0mW = 2.0mW$

Total Device Power (P_{TOTAL}) for 8 switching outputs:

$P_{TOTAL} = P_{ST} + (N_O(P_{DYN} + P_{LOAD})) = 37.86mW + (8(11.65mW + 2.0mW)) = 147.06\ mW$

Summary and Conclusion

This application note empowers the designer to more accurately determine the power dissipation of the 16-bit logic products as implemented in the user's application. The calculations described in the above sections employ application specific variables such as load capacitance, frequency, DC loading contributes to overall power dissipation. Using accurate power dissipation calculations improved power supply selection and design of proper thermal management schemes is achieved.

SMD Ptotal Reference

Frontgrade Part Number	SMD Number	Power Dissipation	Test Conditions	CL (pF)	Limits (mW/MHz)
UT54ACS164245S	5962-98580	Ptotal1	A Port = 3.3V VDD1 = 4.5V and 5.5V VDD2 = 3.13V and 3.6V ---------- B Port = 3.3V VDD1 = 3.13V and 3.6V VDD2 = 3.13V and 3.6V	40	1.5
		Ptotal2	B Port = 5.0V VDD1 = 4.5V and 5.5V VDD2 = 3.13V and 3.6V	40	2.0
		Ptotal3	Port B = 5.0V VDD1 = 4.5V and 5.5V VDD2 = 4.5V and 5.5V	40	2.0
UT54ACS164245SE	5962-98580	Ptotal1	A Port = 3.3V VDD1 = 4.5V and 5.5V VDD2 = 3.0V and 3.6V ---------- B Port = 3.3V VDD1 = 3.0V and 3.6V VDD2 = 3.0V and 3.6V	40	1.5
		Ptotal2	Port B = 5.0V VDD1 = 4.5V and 5.5V VDD2 = 3.0V and 3.6V	40	2.0
		Ptotal3	Port B = 5.5V VDD1 = 4.5V and 5.5V VDD2 = 4.5V and 5.5V	40	2.0
UT54ACS164245SEI	5962-98580	Ptotal1	A Port = 3.3V VDD1 = 4.5V and 5.5V VDD2 = 3.0V and 3.6V ---------- B Port = 3.3V VDD1 = 3.0V and 3.6V VDD2 = 3.0V and 3.6V	40	1.5
		Ptotal2	Port B = 5.0V VDD1 = 4.5V and 5.5V VDD2 = 3.0V and 3.6V	40	2.0
		Ptotal3	Port B = 5.5V VDD1 = 4.5V and 5.5V VDD2 = 4.5V and 5.5V	40	2.0
UT54ACS164646S	5962-06234	Ptotal1	V_{DDA} = V_{DDB} = 4.5V and 5.5V	20	2.0
		Ptotal2	V_{DDA} = V_{DDB} = 3.0V and 3.6V	20	1.5
UT54ACS162245SLV	5962-02543	Ptotal1	VDD = 3.0V and 3.6V	40	6.2
		Ptotal2	VDD = 2.3V and 2.7V	40	3.0

Revision History

Date	Revision #	Author	Change Description	Page #