AEROSPACE DATA EXCHANGE PROGRAM TRANSMITTAL

FRONTGRADE

PROBLEM ADVISORY

1. TITLE	2. DOCUMENT NUMBER
NOTIFICATION OF DATASHEET (DS) UPDATE FOR ADDITIONAL INFORMATION ABOUT POWER APPLICATION AND WARM SPARE OPERATION AS APPLICABLE TO THE UT54ACS164245SEI SCHMITT TRIGGER INPUT CMOS 16-BIT BIDIRECTIONAL MULTIPURPOSE TRANSCEIVER	SPO-2024-PA-0003
	3. DATE *(Year, Month, Date)* 2024, AUGUST, 20
4. MANUFACTURER NAME AND ADDRESS FRONTGRADE TECHNOLOGIES 4350 CENTENNIAL BOULEVARD COLORADO SPRINGS, COLORADO 80907-3486	5. MANUFACTURER POINT OF CONTACT NAME BRUCE MASSEY
	6. MANUFACTURER POINT OF CONTACT TELEPHONE (719) 594-8466
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8. CAGE CODE	9. LDC START	10. LDC END	11. PRODUCT IDENTIFICATION CODE	12. BASE PART
65342	ALL	ALL	JM06	UT54ACS164245SEI

13. BLANK	14. SMD NUMBER	15. DEVICE TYPE DESIGNATOR
	5962-98580	06, 07
	16. RHA LEVELS	17. QML LEVEL
	ALL	ALL
	18. NON QML LEVEL	19. GIDEP NUMBER
	ALL	GB4-PA-2024-0002

20. PROBLEM DESCRIPTION / DISCUSSION / EFFECT

Some UT54ACS164245SEI customers have recently indicated that the instructions in the datasheet (DS) for Warm Spare operation lack sufficient detail in Power Application and related Warm Spare mode setup and operation. The affected part numbers are given in Table 1, and are from the product SMD BULLETIN pages.

Table 1 – Affected Part Numbers (PN)

AFFECTED PN	AFFECTED PN
5962R9858006QXC	UT54ACS164245SEIUCC
5962R9858006VXC	UT54ACS164245SEIUCCR
5962R9858006Q9A	UT54ACS164245SEI-QDIE
5962R9858006V9A	UT54ACS164245SEI-VDIE
5962R9858007QXC	UT54ACS164245SEIUCC
5962R9858007VXC	UT54ACS164245SEIUCCR
5962R9858007Q9A	UT54ACS164245SEI-QDIE
5962R9858007V9A	UT54ACS164245SEI-VDIE

21. ACTION TAKEN / PLANNED

In response to this customer feedback, Frontgrade Technologies has updated the DS under the following sections: Power Supply Application and Operating Requirements, Warm Spare, Cold Spare, pp.5-6. These updates include additional information to provide clarity for product use and will facilitate PCB, PWB, and system-level implementation of customer designs. A reference to the related Application Note (AN) is given below, and is also provided in this DS update.

22. DISPOSITIONARY RECOMMENDATION:	CHECK & USE AS IS ☐	CONTACT MANUFACTURER ☐	REMOVE & REPLACE ☐	CORRECT & USE AS SPECIFIED ☒

Reference Information:

https://www.frontgrade.com/sites/default/files/documents/datasheet-ut54acs164245sei_0.pdf
UT54ACS164245SEI Schmitt CMOS 16-bit Bidirectional MultiPurpose Transceiver

https://www.frontgrade.com/sites/default/files/documents/app-note-16bit-transceiver-coldandwarmspare.pdf
APPLICATION NOTE - Cold and Warm Spare Functionality of the 16-Bit Transceiver Product Family

https://landandmaritimeapps.dla.mil/Downloads/MilSpec/Smd/98580.pdf
MICROCIRCUIT, DIGITAL, RADIATION HARDENED, ADVANCED CMOS, SCHMITT 16-BIT BIDIRECTIONAL MULTI-PURPOSE TRANSCEIVER WITH THREE-STATE OUTPUTS, MONOLITHIC SILICON
5962-98580

DS editorial (text) changes:

Was (Existing):

Power Application Guidelines

For proper operation, connect power to all V_{DD} pins and ground all V_{SS} pins (i.e., no floating V_{DD} or V_{SS} input pins). By virtue of the UT54ACS164245SEI warm spare feature, power supplies V_{DD1} and V_{DD1} may be applied to the device in any order. To ensure the device is in cold spare mode, both supplies, V_{DD1} and V_{DD1} must be equal to V_{SS} +/- 0.3V. Warm spare operation is in effect when one power supply is >1V and the other power supply is equal to V_{SS} +/- 0.3V. If V_{DD1} has a power on ramp longer than 1 second, then V_{DD1} should be powered on first to ensure proper control of DIRx and $\overline{OE}$x. During normal operation of the part, after power-up, ensure $V_{DD1} \geq V_{DD1}$.

Warm Spare

By definition, warm sparing occurs when half of the chip receives its normal V_{DD} supply value while the V_{DD} supplying the other half of the chip is set to 0.0V. When the chip is "warm spared", the side that has V_{DD} set to a normal operational value is "actively" tri-stated because the chip's internal OE signal is forced low. The side of the chip that has V_{DD} set to 0.0V is "passively" tri-stated by the cold spare circuitry. In order to minimize transients and current consumption, the user is encouraged to first apply a high level to the $\overline{OE}$x pins and then power down the appropriate supply.

Cold Spare

The UT54ACS164245SEI places the device into "Cold Spare" mode when BOTH supplies are set to V_{SS} +/_0.25V with a maximum 1KΩ impedance between V_{DD}x and V_{SS}. While in Cold Spare, the device places all outputs into a high impedance state (see DC electrical parameters, Ics).

Is (Changed to):

Power Supply Application and Operating Requirements

The following are a list of power supply application and operating requirements for correct UT54ACS164245SEI operation:

Both V_{DD1} and V_{DD2} power supplies must be first powered-up, and then $\overline{OEx}$ set to a logic high before entering either Cold or Warm Spare modes of operation. These steps are required to initialize internal core logic functions and avoid potential high current operation.

Warm spare operation is in effect when $V_{DD1}(V_{DD2})$ >1V and $V_{DD2}(V_{DD1})$ = V_{SS} +/- 0.25V, with a maximum 1kΩimpedance between $V_{DD2}(V_{DD1})$ and V_{SS}.

The required initialization sequence for Warm Spare mode is: 1) Power up V_{DD1} and V_{DD2}, 2) Set $\overline{OEx}$ to a logic high level, 3) Power down $V_{DD1}(V_{DD2})$, with a maximum 1kΩ impedance between $V_{DD2}(V_{DD1})$ and V_{SS}. These steps are needed to minimize transients and prevent unintended current consumption.

Cold spare operation is in effect when both V_{DD1} and V_{DD2} power supplies are set to V_{SS} +/- 0.25V, with a maximum 1kΩ impedance between V_{DD1} and V_{DD2} and V_{SS}.

The required initialization sequence for Cold Spare mode is: 1) Power up V_{DD1} and V_{DD2}, 2) Set $\overline{OEx}$ to a logic high level, 3) Power down V_{DD1} and V_{DD2}, with a maximum 1kΩ impedance between V_{DD1}, V_{DD2} and V_{SS}. These steps are needed to minimize transients and prevent unintended current consumption.

All V_{DD1} and V_{DD2} power supply and V_{SS} ground pins must be connected. Floating or no-connect (N/C) V_{DD1}, V_{DD2}, V_{SS} pins are not allowed.

For warm spare mode, power supplies V_{DD1} and V_{DD2} may be applied to the device in any order, but simultaneous application is recommended.

If V_{DD1} has a power on ramp time longer than 1 second, then V_{DD2} should be powered on first to ensure proper control of DIRx and $\overline{OEx}$.

$V_{DD1} \geq V_{DD2}$ is a required a required condition following UT54ACS164245SEI device power-up, and also during the normal operation of the part.

For additional details and clarification, please see the referenced Application Note (AN): “Cold and Warm Spare Functionality of the 16-Bit Transceiver Product Family”, A link to this AN is available at the Frontgrade UT54ACS164245SEI product website.

Warm Spare

Warm spare operation is in effect when V_{DD1}(V_{DD2}) is within normal operating range and V_{DD2}(V_{DD1}) = V_{SS} +/- 0.25V, with a maximum 1kΩ impedance between V_{DD2}(V_{DD1}) and V_{SS}. While in Warm Spare mode, the device places all bi-directional I/O and control signals into a high impedance state (see DC electrical parameters, I_{ws}).

All requirements given under the “Power Supply Application and Operating Requirements” section of this datasheet pertaining to Warm Spare mode of operation are applicable.

Cold Spare

Cold Spare mode operation is in effect when both V_{DD1} and V_{DD2} power supplies are set to V_{SS} +/- 0.25V, with a maximum 1kΩ impedance between V_{DD1}, V_{DD2} and V_{SS}. While in Cold Spare mode, the device places all bi-directional I/O and control signals into a high impedance state (see DC electrical parameters, I_{cs}).

All requirements given under the “Power Supply Application and Operating Requirements” section of this datasheet pertaining to Cold Spare mode of operation are applicable.