DATASHEET

RELEASED 10/18

80 Megabit Flow-thru SSRAM

UT8SF2M40

Features

- Synchronous SRAM organized as 2Meg words x 40bit
- Continuous Data Transfer (CDT) architecture eliminates wait states between read and write operations
- Supports 40MHz to 80MHz bus operations
- Internally self-timed output buffer control eliminates the need for synchronous output enable
- Registered inputs for flow-thru operations
- Single 2.5V to 3.3V supply
- Clock-to-output time
  - Clk to Q =12ns
- Clock Enable ($\overline{CEN}$) pin to enable clock and suspend operation
- Synchronous self-timed writes
- Three Chip Enables($\overline{CS0}$,CS1,$\overline{CS2}$) for simple depth expansion
- "ZZ" Sleep Mode option for partial power-down
- "SHUTDOWN" Mode option for deep power-down
- Four Word Burst Capability--linear or interleaved
- Operational Environment
  - Total Dose: 100krad(Si)
  - SEL Immune: ≤100MeV-cm^2/mg
  - SEU error rate: 1.7x10^{-6}errors/bit-day
- Package options:
  - 288-lead CLGA, CCGA, and CBGA
- Standard Microelectronics Drawing (SMD)5962-15227
  - QML Q and Q+

Introduction

The UT8SF2M40 is a high performance 83,886,080-bit synchronous static random access memory (SSRAM) device that is organized as 2M words of 40 bits. This device is equipped with three chip selects ($\overline{CS0}$, CS1, and $\overline{CS2}$), a write enable ($\overline{WE}$), and an output enable ($\overline{OE}$) pin, allowing for significant design flexibility without bus contention. The device supports a four word burst function using (ADV_$\overline{LD}$).

All synchronous inputs are registered on the rising edge of the clock provided the Clock Enable ($\overline{CEN}$) input is enabled LOW. Operations are suspended when $\overline{CEN}$ is disabled HIGH and the previous operation is extended. Write operation control signals are $\overline{WE}$ and six byte write enables $\overline{BWE}$[4:0]. All write operations are performed by internal self-timed circuitry.

For easy bank selection, three synchronous Chip Enables ($\overline{CS0}$, CS1, $\overline{CS2}$) and an asynchronous Output Enable ($\overline{OE}$) provide for output tri-state control. The output drivers are synchronously tri-stated during the data portion of a write sequence to avoid bus contention.

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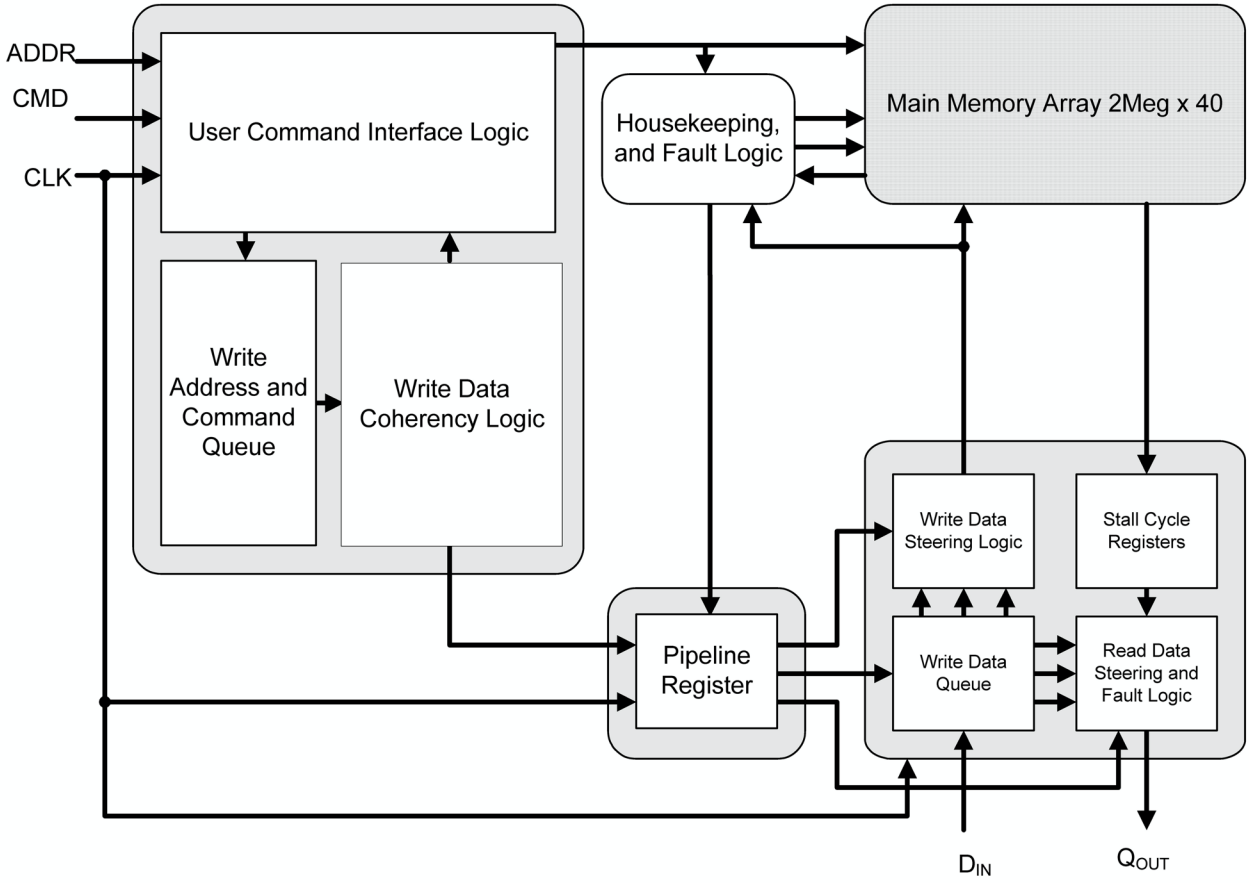

Figure 1. UT8SF2M40 Block Diagram

Table 1: Pin Definitions

Name	Description	Type
$\overline{CS0}$	**Chip Enable 0, Input, Active LOW:** Sampled on the rising edge of CLK. Used in conjunction with CS1 and $\overline{CS2}$ to select or deselect the device.	Input-Synchronous
CS1	**Chip Enable 1 Input, Active HIGH:** Sampled on the rising edge of CLK. Used in conjunction with $\overline{CS0}$ and $\overline{CS2}$ to select or deselect the device.	Input-Synchronous
$\overline{CS2}$	**Chip Enable 2 Input, Active LOW:** Sampled on the rising edge of CLK. Used in conjunction with $\overline{CS0}$ and CS1 to select or deselect the device.	Input-Synchronous
A[20:0]	**Address Inputs:** Sampled at the rising edge of the CLK. A[1:0] is fed to the two-bit burst counter.	Input-Synchronous
$\overline{BWE}$[4:0]	**Byte Write Enable, Active LOW:** Qualified with $\overline{WE}$, allows writes to each of six bytes of memory when active, and masks input data when disabled.	Input-Synchronous
$\overline{WE}$	**Write Enable Input, Active LOW:** Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be enabled LOW to initiate a write sequence.	Input-Synchronous
ADV_$\overline{LD}$	**Advance/Load Input:** Advances the on-chip address counter or loads a new address. When HIGH (and $\overline{CEN}$ is enabled LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After deselection, drive ADV_$\overline{LD}$ LOW to load a new address.	Input-Synchronous
CLK	**Clock Input:** Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.	Input-Clock
$\overline{OE}$	**Output Enable, Asynchronous Input, Active LOW:** Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are enabled to behave as outputs. When disabled HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state and when the device is deselected.	Input-Asynchronous
$\overline{CEN}$	**Clock Enable Input, Active LOW:** When enabled LOW, the clock signal is recognized by the SSRAM. When deasserted HIGH, the clock signal is masked. Because deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.	Input-Synchronous
DQ[47:0]	**Bidirectional Data I/Os:** As inputs, DQ[47:0] feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, DQ[47:0] delivers the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is enabled LOW, the pins behave as outputs. When HIGH, DQs are placed in a tri-state condition. The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$. CAES recommends connecting all DQ pins to either VDDQ or VSS through a ≥10kΩ resistor.	I/O-Synchronous
$\overline{RESET}$	**Reset Input, Active Low:** Resets device to known configuration. Reset is required at initial power-up, after exiting shutdown mode, or after any power interruption.	Input-ASynchronous

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Table 1: Pin Definitions

Name	Description	Type
ZZ	**ZZ "Sleep" Input, Active HIGH:** When HIGH, places the device in a non-time critical "sleep" condition with data integrity preserved. During normal operation, this pin must be LOW.	Input-Synchronous
SHUTDOWN	**Shutdown Input, Active HIGH**: When HIGH, places device in shutdown mode. System clock can be stopped. Memory contents are not retained.	Input-Asynchronous
READY[1]	**Device Ready Output:** READY outputs a HIGH when device is available for normal operations. READY outputs a LOW when requesting an idle cycle or during power up initialization. The READY output is a pseudo open-drain to support multiple device READY outputs connected to a single controller input with minimal contention. The READY pin drives high for one user clock cycle then tri-states. The READY pin requires an external pull-up connection to V_{DDQ} through a ≥10kΩ±10% resistor to maintain the high logic state.	Output-Synchronous
MODE[2]	**Mode Input:** Established at power up. Selects the burst order of the device. When tied to VSS selects linear burst sequence. When tied to VDDQ selects interleaved burst sequence.	Input-DC
EXTRES[2]	**Input Current Reference:** Provided for external precision current reference resister connection.	Input-DC
V_{DD}	Power supply inputs to the Core of the Device.	Power Supply
V_{DDQ}	Power supply for the I/O Circuitry.	I/O Power Supply
V_{SS}	Ground inputs to the core of the device.	Ground
V_{SSQ}	Ground for I/O circuitry	I/O Ground
NUIL	**Not used Input Low:** Pins designated as NUIL need to be externally connected by user to V_{SSQ} through a ≥10kΩ±10% resistor.	--
NUIH	**Not used Input High:** Pins designated as NUIH need to be externally connected by user to V_{DDQ} through a ≥10kΩ±10% resistor.	--
NC	**No Connects**. Not internally connected to the die.	---
TDO[3]	**JTAG circuit serial data output:** Package pin requires a pull-up through ≥10kΩ±10% resistor to V_{DDQ}.	JTAG Serial Output Synchronous
TDI[3]	**JTAG circuit serial data input:** Device pin internally connected through a 75kΩ±10% resistor to V_{DDQ}.	JTAG Serial Input Synchronous
TMS[3]	**JTAG controller Test Mode Select:** Device pin internally connected through a 75kΩ±10% resistor to V_{DDQ}.	Test Mode Select Synchronous
TCK[3]	**JTAG circuit Clock input:** Package pin requires a pull-up through ≥10kΩ±10% resistor to V_{DDQ}.	JTAG Clock

Notes:

1) Reference application note AN-MEM-004 for additional READY signal information.
2) DC inputs are established at power up and cannot be switched while power is applied to the device.
3) Reference application note AN-MEM-005 for JTAG operations. JTAG operations are intended for terrestrial use and not guaranteed in radiation environment.

Device Operation

The UT8SF2M40 is synchronous flow-thru SSRAM designed specifically to eliminate wait states during Write/Read or Read/ Write transitions. All synchronous inputs and outputs are registered on the rising edge of clock. The clock signal is enabled by the Clock Enable input ($\overline{CEN}$). When $\overline{CEN}$ is HIGH, the clock signal is disregarded and all internal states are maintained. All synchronous operations are qualified by $\overline{CEN}$. Once power-up requirements have been satisfied, the input clock may only be stopped during sleep (ZZ is HIGH) or shutdown mode (SHUTDOWN is HIGH). Maximum access delay from the rising edge of clock (t_{CQV}) is 12ns (80MHz device).

Access is initiated by asserting all three Chip Enables ($\overline{CS0}$, CS1, $\overline{CS2}$) active at the rising edge of the clock with Clock Enable ($\overline{CEN}$) and ADV_$\overline{LD}$ asserted LOW. The address presented to the device will be registered. Access can be either a Read or Write operation, depending on the status of the Write Enable ($\overline{WE}$).

Write operations are initiated by the Write Enable ($\overline{WE}$) input. All write commands are controlled by built in synchronous self-timed circuitry.

Three synchronous Chip Enables ($\overline{CS0}$, CS1, $\overline{CS2}$) and an asynchronous Output Enable ($\overline{OE}$) simplify memory depth expansion. All operations (Reads, Writes, and Deselects) are pipelined. ADV_$\overline{LD}$ must be driven LOW once the device has been deselected in order to load a new address and command for the next operation.

Single Read Accesses

A read access is initiated when the following device inputs are present at rising clock edge: $\overline{CEN}$ is enabled LOW, $\overline{CS0}$, CS1, and $\overline{CS2}$ are all enabled, the Write Enable input signal $\overline{WE}$ is disabled HIGH and ADV_$\overline{LD}$ is asserted LOW. The addresses present at the address inputs A[20:0] are registered and presented to the memory. Data propagates to the input of the output register. Data will be available to the bus 12ns after the next rising clock edge provided $\overline{OE}$ is enabled LOW. After the first clock of the read access, the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be enabled LOW to drive requested data. During the next rising clock, any operation (Read/Write/Deselect) may be initiated.

Burst Read Accesses

The UT8SF2M40 has an internal burst counter allowing up to four reads to be performed from a single address input. A new address can only be loaded when ADV_$\overline{LD}$ is driven LOW. New addresses are loaded into the SSRAM, as described by the Single Read Access section. The burst counter operates in either linear or interleave and is controlled by the MODE input at power up. When MODE pin is LOW, the burst sequence is linear. The burst sequence is interleaved when MODE is HIGH. A0 and A1 are controlled by the burst counter. The burst counter will wrap around when needed. The burst counter increments anytime ADV_$\overline{LD}$ is HIGH and $\overline{CEN}$ is low. The operation selected by the state of $\overline{WE}$ is latched at the beginning of the sequence and maintained throughout.

Single Write Accesses

A write access is initiated when the following device inputs are present at rising clock edge: $\overline{CEN}$ is enabled LOW, $\overline{CS0}$, CS1, and $\overline{CS2}$ are all enabled, the Write Enable input signal $\overline{WE}$ is enabled LOW and ADV_$\overline{LD}$ is asserted LOW. The addresses present at the address inputs A[20:0] are registered and presented to the memory core. Data I/Os are tri-stated at the next rising edge of clock regardless of state of $\overline{OE}$. The write is completed after the next rising clock edge using data present on DQ pins. Each byte of data is individually qualified by its applicable byte write enable input (see Table 2). When the input low, the applicable DQ inputs are registered to memory. When the input is high, the applicable DQ pins are ignored.

To avoid bus contention data should not be driven to DQs when outputs are active. The Output Enable ($\overline{OE}$) may be disabled HIGH before applying data to the DQ lines. This will tri-state the DQ output drivers. As an additional feature DQ lines are automatically tri-stated during the data portion of a Write cycle, regardless of the state of $\overline{OE}$.

Burst Write Accesses

The UT8SF2M40 has an internal burst counter allowing up to four writes to be performed from a single address input. A new address can only be loaded when ADV_$\overline{LD}$ is driven LOW. New addresses are loaded into the SSRAM, as described in the Single Write Access section. When ADV_$\overline{LD}$ is driven HIGH on the subsequent clock rise, where $\overline{CEN}$ is LOW, the Chip Enables ($\overline{CS0}$, CS1, $\overline{CS2}$) and $\overline{WE}$ inputs are ignored and the burst counter is incremented. The $\overline{BWE}$[4:0] inputs must be LOW in each cycle of the burst write in order to qualify each respective byte of data.

Ready Status

The UT8SF2M40 device operates as a Synchronous SRAM device. Data integrity housekeeping activities are performed in the background during normal user activity. These housekeeping activities are performed on a regular basis. However, when a housekeeping activity sequence cannot be completed due to user conflict for memory space, the READY pin asserts signifying to the user that an idle cycle is required. Please reference applications note AN-MEM-004 for more information.

Byte Write Enables $\overline{BWE}$[4:0]

The UT8SF2M40 device employs six byte write enable inputs to be used in conjunction with $\overline{WE}$ to qualify each associated byte of data into the memory. When $\overline{WE}$ is HIGH, the device is in read mode where all $\overline{BWE}$[4:0] are don't cares. When $\overline{WE}$ is LOW, each $\overline{BWE}$[4:0] must also be low to write the associated data input pins into memory. Data input pins whose associated byte write enable pin is HIGH, will be masked.

Table 2. Byte Write Enable to Data Input Pins

Byte Write Enable Input	Data Input Pins
$\overline{BWE0}$	DQ[7:0]
$\overline{BWE1}$	DQ[15:8]
$\overline{BWE2}$	DQ[23:16]
$\overline{BWE3}$	DQ[31:24]
$\overline{BWE4}$	DQ[39:32]

Sleep Mode

The ZZ input lead is a synchronous input. Asserting the ZZ pin HIGH places the SSRAM into a power conservative "sleep" mode. To assure the completion of previous commands through the pipeline prior to entering sleep mode, a minimum of two full clock cycles (t_{ZZS}) are required between the last operation command and asserting the ZZ input. While in sleep mode, data integrity is guaranteed. Changing the input clock frequency or halting the input clock may be executed during sleep mode. The device must be deselected prior to entering sleep mode and remain deselected for the duration of t_{ZZREC} after the ZZ input returns LOW.

Shutdown Mode

The SHUTDOWN input pin is an asynchronous input. Asserting SHUTDOWN places the device in a power saving shutdown mode. The system clock can be stopped. Memory contents are not maintained in shutdown mode. The SSRAM requires a reset upon exiting shutdown mode.

Table 3. Linear Burst Address Table (MODE=V_{SS})

Starting Address	Second Address	Third Address	Fourth Address
A1, A0	**A1, A0**	**A1, A0**	**A1, A0**
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Table 4. Interleaved Burst Address Table (MODE=V_{DDQ})

Starting Address	Second Address	Third Address	Fourth Address
A1, A0	**A1, A0**	**A1, A0**	**A1, A0**
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Power Up/ Down Requirements

The SSRAM requires that $V_{DD} \leq V_{DDQ}$ at all times. The SSRAM does require the user to provide an external reset after initial power application, exiting shutdown mode, or any power interruption to the device input voltage outside the specified limit. Performing a reset requires the assertion of the $\overline{\text{RESET}}$ device input lead (LOW) for a minimum of 1 us (t_{RLRH}). After the $\overline{\text{RESET}}$ input is returned HIGH, the device requires 50us ($t_{SHTDWNREC}$) to complete the reset operation. Once the reset operation is complete, the device requires an additional 20us (t_{CR}) to synchronize the clock input providing a stable input clock is present. The device READY output lead asserts HIGH once t_{CR} is satisfied at the next rising clock. The READY out lead HIGH indicates the device is available for normal operations. For power down it is required that V_{DD} and V_{DDQ} be powered down to ≤0.5V for a minimum of100ms.

Clock Conditioning Requirements

The CLK signal input requirements are given in the Clock section of the AC Characterizations. AC Characterization performances listed herein are based on providing a clock input signal meeting these requirements.

Changing Clock Frequencies

The CLK input frequency should be established at a power on, and may only be changed while in SLEEP mode (reference Table 6).

External Connections

A precision 25kohm ≤±0.2% low TCR ≤25ppm/°C resistor is required to be connected between device pin EXTRES (R15) and V_{SS}.

In order to ensure proper operation in conjunction with JTAG boundary scan (reference applications note MEM-AN-005), CAES requires that specific package pins be biased through soft connections to either V_{DDQ} or V_{SSQ}. Table 5 is a list of these required external biases.

Table 5. External Bias Conditions

Signal Name	Package Pin	Bias Condition
NUIL[1]	H1, H20, N1, N2, N19, N20, P13, R7, R8, R10, R12, R13, R14, R16	≥10kΩ to V_{SSQ}
NUIH[2]	P16, R8	≥10kΩ to V_{DDQ}
TDO	R5	≥10kΩ to V_{DDQ}
TCK	R9	≥10kΩ to V_{SSQ}
DQ[47:0][3]	ref Table 7	≥10kΩ to V_{DDQ} or V_{SSQ}
READY	C4	≥10kΩ to V_{DDQ}

Notes:

1) NUIL = Not Used Input Low.
2) NUIH = Not Used Input High
3) CAES recommends connecting all DQ[47:0] to either V_{DDQ} or V_{SSQ} through ≥10kΩ resistors.

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Table 6: Truth Table for UT8SF2M40[1,2,3,4,5,6,7]

Operation	Address Used	$\overline{CSx}$*	ZZ	SHUT DOWN	ADV_$\overline{LD}$	$\overline{WE}$	$\overline{BWEx}$	$\overline{OE}$	$\overline{CEN}$	CLK	DQs
Standby Mode	None	H	L	L	L	X	X	X	L	L-H	3-State
Continue Deselect	None	X	L	L	H	X	X	X	L	L-H	3-State
Read Cycle (Start Burst)	External	L	L	L	L	H	X	L	L	L-H	Data Out
Read Cycle (Cont. Burst)	Next	X	L	L	H	X	X	L	L	L-H	Data Out
NOP/Dummy Read (Start)	External	L	L	L	L	H	X	H	L	L-H	3-State
NOP/Dummy Read (Cont.)	Next	X	L	L	H	X	X	H	L	L-H	3-State
Write Cycle (Start Burst)	External	L	L	L	L	L	L	X	L	L-H	Data In
Write Cycle (Cont. Burst)	Next	X	L	L	H	X	L	X	L	L-H	Data In
Dummy Write (Start)	None	L	L	L	L	L	H	X	L	L-H	3-State
Dummy Write (Cont. Burst)	Next	X	L	L	H	X	H	X	L	L-H	3-State
Clock Inhibit (Stall)	N/A	X	L	L	X	X	X	X	H	L-H	N/A
Sleep Mode	N/A	H	H	L	X	X	X	X	X	X	3-State
Shutdown Mode	None	X	X	H	X	X	X	X	X	X	3-State

Notes:

*All chip selects active when L, at least one chip selects inactive when H

1) X = "Don't Care", H = Logic HIGH, L = Logic LOW.
2) Write is defined by $\overline{WE}$ and $\overline{BWEx}$.
3) When a Write cycle is detected, all I/Os are tri-stated.
4) The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal.
5) $\overline{CEN}$ = H inserts wait states.
6) Device will power-up deselected and the I/Os in a tri-state condition, regardless of $\overline{OE}$.
7) $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during Write cycles. During a Read cycle DQs = tri-state when $\overline{OE}$ is inactive or when the device is deselected and DQs= data when $\overline{OE}$ is active.

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Table 7. 288-Lead Pipelined Signal Locations

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A			VDDQ	$\overline{CS2}$	$\overline{WE}$	VSS	A10	A8	A4	A18	A19	A14	A15	A2	A0	$\overline{CS0}$	VSS	$\overline{BWE1}$		
B		VSS	VSS	$\overline{OE}$	$\overline{BWE2}$	A11	A9	A6	A17	VSS	A20	A16	A13	A12	A1	ZZ	$\overline{BWE3}$	SHUT DOWN	VSS	
C	VDDQ	VSSQ	VSS	READY[1]	$\overline{BWE0}$	$\overline{BWE4}$	A7	A5	VSS	VDD	VSS	VSSQ	VDD	VDD	A3	ADV_$\overline{LD}$	CS1	VSS	VSSQ	VDD
D	DQ33	DQ35	VDD	VSS	VSS	VDDQ	VSSQ	VDD	VDD	VSS	VDD	VDD	VSSQ	VDDQ	VDD	VSS	VSS	VDD	VDDQ	DQ32
E	DQ37	DQ1	DQ39	VDD	VSSQ	VSS	VSSQ	VDDQ	VSS	VSS	VSS	VSSQ	VDDQ	VSS	VSS	VSSQ	VDD	DQ38	DQ36	DQ34
F	DQ3	DQ5	DQ7	VDDQ	VDDQ	VSSQ	VSS	VSS	VDD	VSS	VDD	VSS	VSS	VDDQ	VSSQ	VDDQ	VDDQ	DQ4	DQ0	DQ2
G	DQ9	DQ11	DQ13	VDD	VSSQ	VDD	VDDQ	VDD	VSS	VDD	VSS	VDD	VDDQ	VSSQ	VDD	VSSQ	VDD	DQ10	DQ6	DQ8
H	NUIL[3]	DQ15	$\overline{CEN}$	VSS	VSS	VDD	VDD	VDD	VSS	VSS	VSS	VDD	VDD	VSS	VSS	VSS	VSS	CLK	DQ12	NUIL
J	DQ19	DQ17	DQ21	VDD	VSSQ	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VSSQ	VDD	VSSQ	VDD	DQ14	DQ16	DQ18
K	DQ27	DQ25	DQ23	VDDQ	VDDQ	VSSQ	VSS	VDDQ	VDD	VSS	VDD	VDDQ	VSS	VDDQ	VSSQ	VDDQ	VDDQ	DQ20	DQ24	DQ22
L	DQ31	DQ41	DQ29	VDD	VSSQ	VSS	VSSQ	VDDQ	VSS	VSS	VSS	VSSQ	VDDQ	VSS	VSS	VSSQ	VDD	DQ26	DQ30	DQ28
M	DQ45	DQ47	DQ43	VDD	VSS	VSSQ	VDDQ	VSSQ	VDD	VSS	VDD	VDD	VSSQ	VDDQ	VSSQ	VSS	VDD	DQ40	DQ44	DQ42
N	NUIL[3]	NUIL[3]	VSS	VSS	VDD	VDDQ	VSSQ	VDD	VSS	VDD	VSS	VSS	VDD	VSSQ	VSSQ	VDD	VSS	DQ46	NUIL[3]	NUIL[3]
P		VSS	VSS	VDD	VDDQ	VSSQ	VSSQ	VSSQ	VSS	VSS	VDDQ	MODE	NUIL[3]	VDDQ	TMS	NUIH[4]	VSSQ	VSS	VSS	
R			VDD	TDI	TDO[1]	VDD	NUIL[3]	NUIH[4]	TCK[2]	NUIL[3]	$\overline{RESET}$	NUIL[3]	NUIL[3]	NUIL[3]	EXTRES	NUIL[3]	VDDQ	VDD		

Notes:

1) Pin requires pull-up to V_{DDQ} of ≥10kΩ±10%.
2) Pin requires pull-down to V_{SS} of ≥10kΩ±10%.
3) NUIL = Not used Input Low. NUIL pins requires ≥10kΩ±10% pull-down to V_{SSQ}.
4) NUIH = Not Used Input High. NUIH pins requires ≥10kΩ ±10% pull-up to V_{DDQ}.

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Absolute Maximum Ratings[1]

(Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}/V_{DDQ}	Supply Voltage[2]	-0.5 to 4.0	V
V_{IN}	Voltage on any pin[2]	-0.3 to V_{DDQ}+0.3	V
I_{IO}	DC I/O current per pin @ T_J = 135° for 15 years	±10	mA
P_D	Package power dissipation permitted @ T_C = 105°C[3]	15	W
T_J	Maximum junction temperature	+150	°C
Θ_{JC}	Thermal resistance junction to case	3	°C/W
T_{STG}	Storage temperature	-65 to +150	°C

Notes:

1) Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions.
2) All voltages are referenced to V_{SS}.
3) Per MIL-STD-883, Method 1012, Section 3.4.1 $P_D = \frac{(T_J(max)-T_C(max))}{\Theta_{JC}}$

Operational Environments

Parameter	Limits	Units
Total Ionizing Dose (TID)	100	krad(Si)
Heavy Ion Error Rate[1]	$1.7x10^{-6}$	Errors/Bit-Day
Single Event Latchup (SEL) Immune[2]	≤ 100	MeV-cm²/mg

Notes:

1) Adams 90% worst case environment, Geosynchronous orbit, 100mils of aluminum.
2) Temperature = 105°C; V_{DD} and V_{DDQ} = 3.6V.

Recommended Operating Conditions

Symbol	Parameter	Limit
V_{DD}	Core supply voltage	2.3V to V_{DDQ}
V_{DDQ}	I/O power supply voltage	2.3V to 3.6V
T_C	Case temperature range	-55°C to +105°C
V_{IN}	DC input voltage	0V to V_{DDQ}
T_J	Junction Temperature	-55°C to +125°C

DC Electrical Characteristics (Pre and Post-Radiation)*

(V_{DD}= 2.3V to V_{DDQ}, V_{DDQ}= 2.3 to 3.6V; Unless otherwise noted, Tc is per the temperature range ordered)

Parameter	Description	Condition		MIN	MAX	Unit
V_{DD}	Core Power Supply Voltage			2.3	V_{DDQ}	V
V_{DDQ}	I/O Power Supply Voltage			2.3	3.6	V
V_{OH}	Output HIGH Voltage	For 3.0V I/O, I_{OH}=-4mA I_{OH}		0.8 * V_{DDQ}		V
		For 2.3V I/O, I_{OH} =-1mA		2.0		V
V_{OL}	Output LOW Voltage	For 3.0V I/O, I_{OL}=8mA			0.4	V
		For 2.3V I/O, I_{OL} =1mA			0.4	V
V_{IH}	Input HIGH Voltage	For 3.0V I/O		2.0		V
		For 2.3V I/O		1.7		V
V_{IL}	Input LOW Voltage	For 3.0V I/O			0.8	V
		For 2.3V I/O			0.7	V
I_{IN1}	Input Leakage Current	V_{IN} = V_{DDQ} and V_{SS} Except device pins TDI and TMS		-2	2	µA
I_{IN2}	Input Leakage Current	V_{IN} = V_{DDQ} Device pins TDI and TMS			2	µA
		V_{IN} = V_{SS} Device pins TDI and TMS		-100		µA
I_{OZ}	Three-State Output Leakage Current	V_{DD}, V_{DDQ} = (Max), V_O= V_{DDQ} and V_{SS}, $\overline{OE}$ = V_{DDQ} (Max)		-2	2	µA
I_{OS}[1,2]	Short-Circuit Output Current	V_{DD}, V_{DDQ} = (Max), V_O = V_{DDQ} and V_{SS}		-100	100	mA
I_{DD}[3]	V_{DD} Supply Current in Active Mode	V_{DD}, V_{DDQ} = (Max), I_{OUT} = 0mA, f = f_{max}	105°C		900	mA
			-55°C and 25°C		750	mA
I_{DDQ}[3]	V_{DDQ} Supply Current in Active Mode	V_{DD}, V_{DDQ} = (Max), I_{OUT} = 0mA, f = f_{max}	105°C		100	mA
			-55°C and 25°C		100	mA
I_{SHTDWN}[3]	V_{DD} Supply Current in Shutdown Mode	V_{DD}, V_{DDQ} = (Max), V_{IN}≥ V_{IH} or V_{IN}≤ V_{IL}, SHUTDOWN ≥ V_{IH}	105°C		250	mA
			-55°C and 25°C		200	mA
$I_{SHTDWNQ}$[3]	V_{DDQ} Supply Current in Shutdown Mode	V_{DD}, V_{DDQ} = (Max), V_{IN}≥ V_{IH} or V_{IN}≤ V_{IL}, SHUTDOWN ≥ V_{IH}	105°C		15	mA
			-55°C and 25°C		15	mA
I_{STBY}[3]	V_{DD} Supply Current in Standby Mode	V_{DD}, V_{DDQ} = (Max) V_{IN}≥ V_{IH} or V_{IN}≤ V_{IL}, f = fmax, device deselected	105°C		650	mA
			-55°C and 25°C		500	mA
I_{STBYQ}[3]	V_{DDQ} Supply Current in Standby Mode	V_{DD}, V_{DDQ} = (Max) V_{IN}≥ V_{IH} or V_{IN}≤ V_{IL}, f = fmax, device deselected	105°C		100	mA
			-55°C and 25°C		100	mA

Parameter	Description	Condition		MIN	MAX	Unit
I_{ZZ}[3]	V_{DD} Supply Current in Sleep Mode	V_{DD}, V_{DDQ} = (Max), $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, ZZ ≥ VIH, SHUTDOWN ≤ V_{IL}	105°C		500	mA
			-55°C and 25°C		350	mA
I_{ZZQ}[3]	V_{DDQ} Supply Current in Sleep Mode	V_{DD}, V_{DDQ} = (Max), $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, ZZ ≥ V_{IH}, SHUTDOWN ≤ V_{IL}	105°C		85	mA
			-55°C and 25°C		85	mA

Capacitance

Symbol	Parameter	MIN	MAX	Unit
C_{IN}[4]	Input Capacitance		15	pF
$C_{I/O}$[4]	I/O Capacitance		15	pF

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) Supplied as a design limit but not guaranteed nor tested.
2) Not more than one output may be shorted at a time for maximum duration of one second.
3) Post-irradiation limits are the 105°C limits when specified.
4) Measured only for initial qualification and after process or design changes that could affect this parameter.

AC Characteristics (Pre and Post-Radiation)*

(V_{DD}= 2.3V to V_{DDQ}, V_{DDQ} = 2.3 to 3.6V; Unless otherwise noted, Tc is per the temperature range ordered.)[1]

Parameter	Description	MIN	MAX	Unit
$t_{Powerup}$[2]	V_{DD} to first valid command (READ or WRITE)	100		ms
CLOCK				
t_{CYC}[6]	Clock (CLK) cycle time	12.5	25.0	ns
t_{CH}	CLK HIGH time	0.4 * t_{CYC}	0.6 * t_{CYC}	ns
t_{CL}	CLK LOW time	0.4 * t_{CYC}	0.6 * t_{CYC}	ns
t_r,t_f[2]	Input clock rise/fall time (10-90%)	2.25		V/ns
t_{clkPJ}[3,5]	Input clock period jitter	-100	100	ps
t_{clkCCJ}[3,5]	Input clock cycle to cycle jitter		150	ps
Setup Times				
t_{AS}	Address setup time prior to CLK	2.5		ns
t_{DS}	Data setup time prior to CLK	1.5		ns
t_{CENS}	Clock enable ($\overline{CEN}$) setup time prior to CLK	3		ns
t_{WES}	Write enable ($\overline{WE}$) setup time prior to CLK	3		ns
t_{BWES}	Byte Write enable ($\overline{BWE}$[4:0]) setup time prior to CLK	3		ns
t_{ADVLDS}	Advance load (ADV_$\overline{LD}$) setup time prior to CLK	2.5		ns
t_{CSS}	Chip select (CSx) setup time prior to CLK	3		ns
Hold Times				
t_{AH}	Address hold time after CLK	1.2		ns
t_{DH}	Data hold time after CLK	1.4		ns
t_{CENH}	$\overline{CEN}$ hold time after CLK	1.2		ns
t_{WEH}	$\overline{WE}$ hold time after CLK	1.5		ns
t_{BWEH}	Byte Write enable ($\overline{BWE}$[4:0]) hold time after CLK	1.5		ns
t_{ADVLDH}	ADV_$\overline{LD}$ hold time after CLK	0.9		ns
t_{CSH}	CSx hold time after CLK	1.8		ns
Output Times				
t_{CQV}[4]	Data valid after rising CLK		12	ns
t_{OEQV}[4]	Output enable ($\overline{OE}$) active to data valid		4.0	ns
t_{CQOH}	Data output hold time after rising CLK	2.0		ns
t_{CQZ}[5]	Rising CLK to output three-state time		5.0	ns
t_{CQX}[5]	Rising CLK to output enable time	1.3		ns
t_{OEQZ}[5]	$\overline{OE}$ inactive to output three-state time		4.5	ns
t_{OEQX}[5]	$\overline{OE}$ active to output enable time	0		ns

Notes:
*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) AC Characteristics based on compliance with CLOCK input specifications
2) Supplied as a design guideline, not tested or guaranteed.
3) Period and Cycle to Cycle jitter is defined by JEDEC Standard 65B
4) Maximum data output valid times guaranteed up to 25pf load capacitance. For loads >25pf, a derating factor of parameter = [specification max(ns) + (C_{Load} - 25pF)(44.2ps/pF].
5) Guaranteed by design.
6) Maximum Cycle Time is tested functionally.

Shutdown and Sleep Mode Characteristics (Pre and Post-Radiation)*

(V_{DD}= 2.3V to V_{DDQ}, V_{DDQ} = 2.3 to 3.6V; Unless otherwise noted T_C is for temperature range ordered.)

Parameter	Description	Condition	MIN	MAX	Unit
t_{ZZS}[3]	Device operation to SLEEP mode	ZZ ≥ V_{IH}	1 t_{CYC}		ns
t_{ZZH}[3]	SLEEP high pulse width	ZZ ≥ V_{IH}	100		µs
t_{ZZL}[3]	SLEEP low pulse width	ZZ ≤ V_{IH}	100		µs
$t_{SHTDWNS}$[3]	Device operation to SHUTDOWN	SHUTDOWN ≥ V_{IH}	2 t_{CYC}		ns
t_{ZZREC}[3]	SLEEP recovery time	STANDBY ≤ V_{IL}	100 + (3*t_{CYC})		ns
$t_{SHTDWNREC}$[1,3]	SHUTDOWN recovery time	SHUTDOWN ≤ V_{IL}		50	us
t_{ZZI}[4]	Active to SLEEP current	ZZ ≥ V_{IH}		100 + (3*t_{CYC})	ns
$t_{SHTDWNI}$[4]	Active to SHUTDOWN current	SHUTDOWN ≥ V_{IH}		250	ns
t_{RZZI}[4]	Time to exit SLEEP current mode	STANDBY ≤ V_{IL}	0		ns
$t_{RSHTDWNI}$[4]	Time to exit SHUDOWN current mode	SHUTDOWN ≤ V_{IL}	0		ns
t_{CR}[1,2,3]	Clock recovery prior to exiting ZZ	ZZ ≥ V_{IH}		20	µs
t_{RLRH}	$\overline{\text{RESET}}$ low to high time	Shutdown ≤ V_{IL}	1		µs
t_{PDS}[3]	SLEEP setup time prior to CLK		2.0		ns
t_{PDH}[3]	SLEEP hold time after CLK		0.5		ns

Notes:
*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured

1) The clock must start up prior to exiting sleep or shutdown modes. Parameter is guaranteed by design.
2) T_{CR} is necessary anytime the clock is stopped, after initial power on, or exiting shutdown mode.
3) Tested functionally.
4) Guaranteed by design.

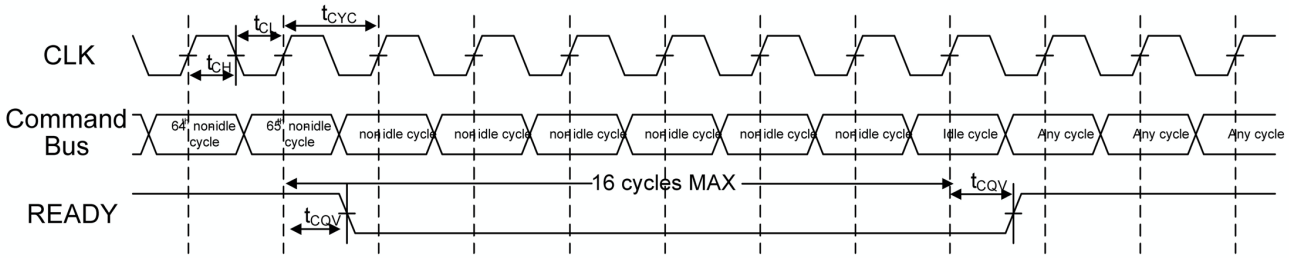

Figure 3. Switching Waveform for Internal Housekeeping

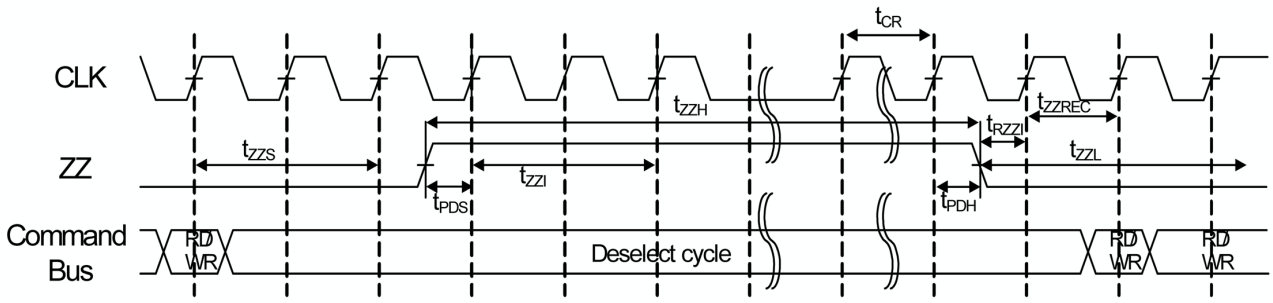

Figure 4. Switching Waveform for SLEEP Mode

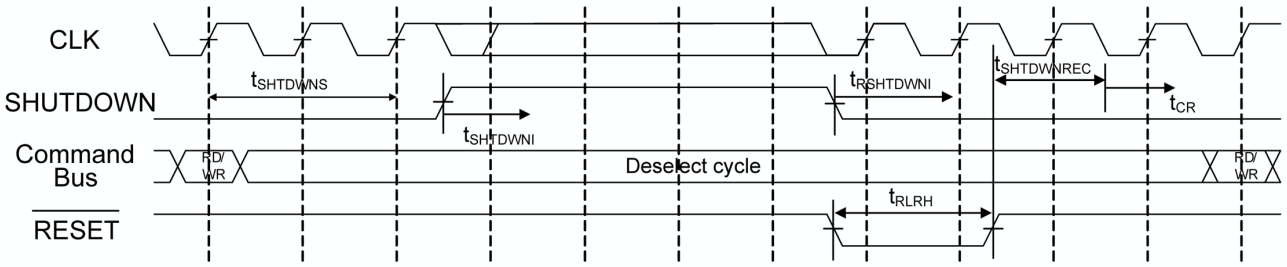

Figure 5. Switching Waveform for SHUTDOWN Mode

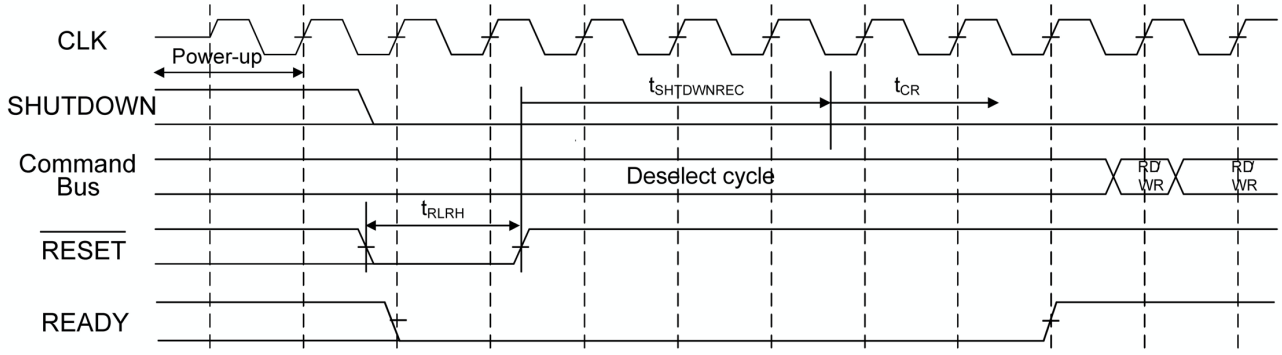

Figure 6. Switching Waveform for Power-Up

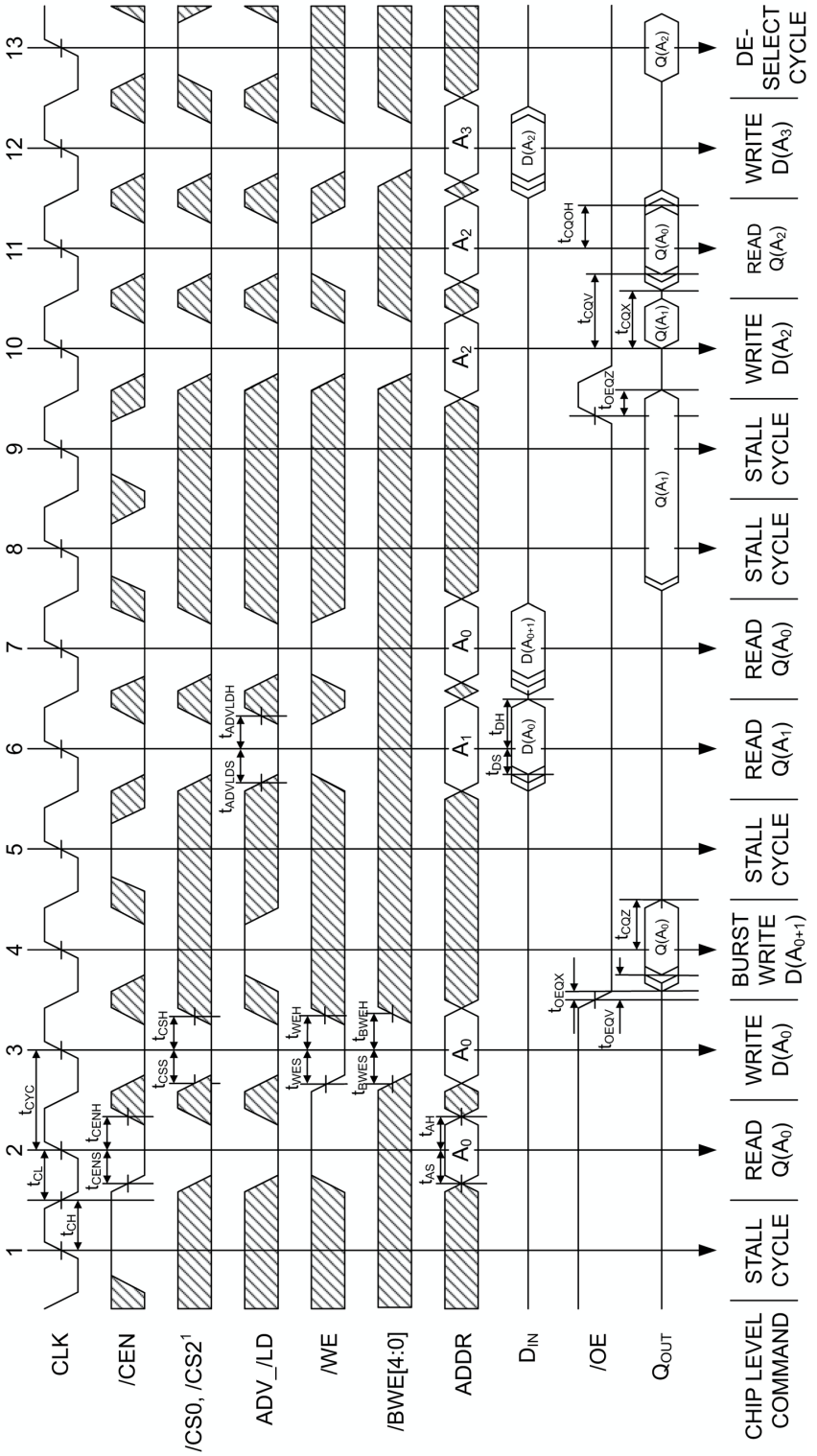

Figure 7. Switching Waveforms for Pipelined Cycle Operations

Note:

1) CS1 has timing transitions identical to /CS0 and /CS2 but is inverted logically. For example, when /CS0 and /CS2 are LOW CS1 is High.

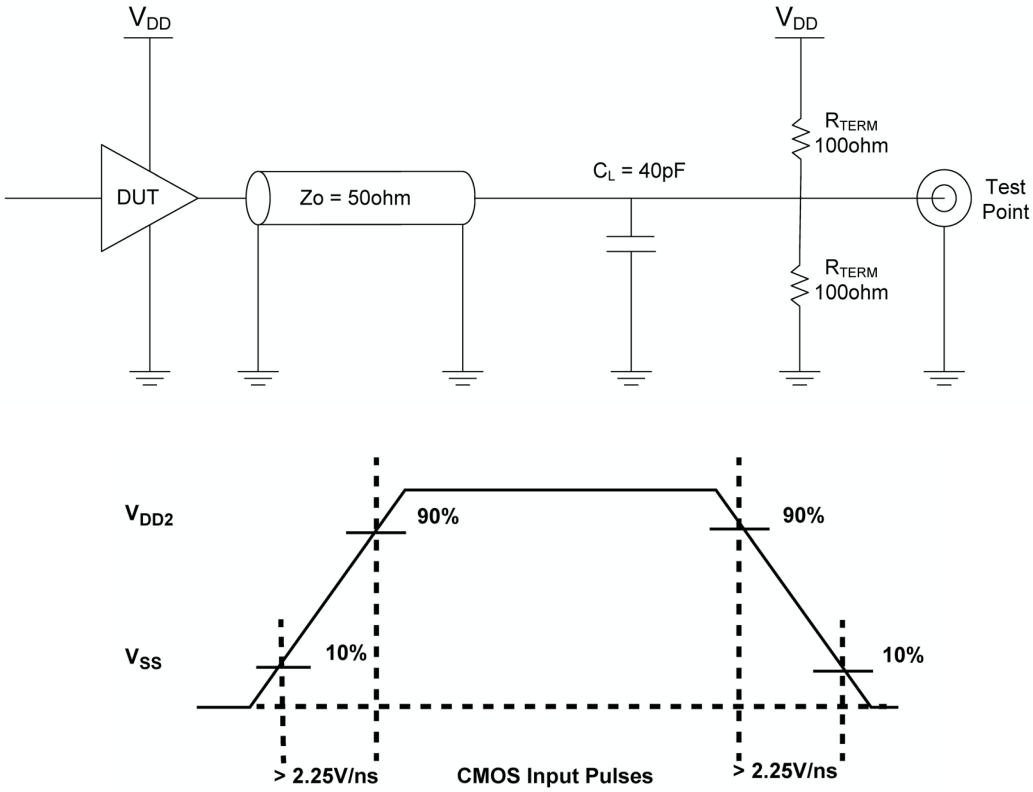

Figure 8. AC Test Loads and Input Waveforms

Note:

1) Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = $V_{DD2}/2$.

Packaging

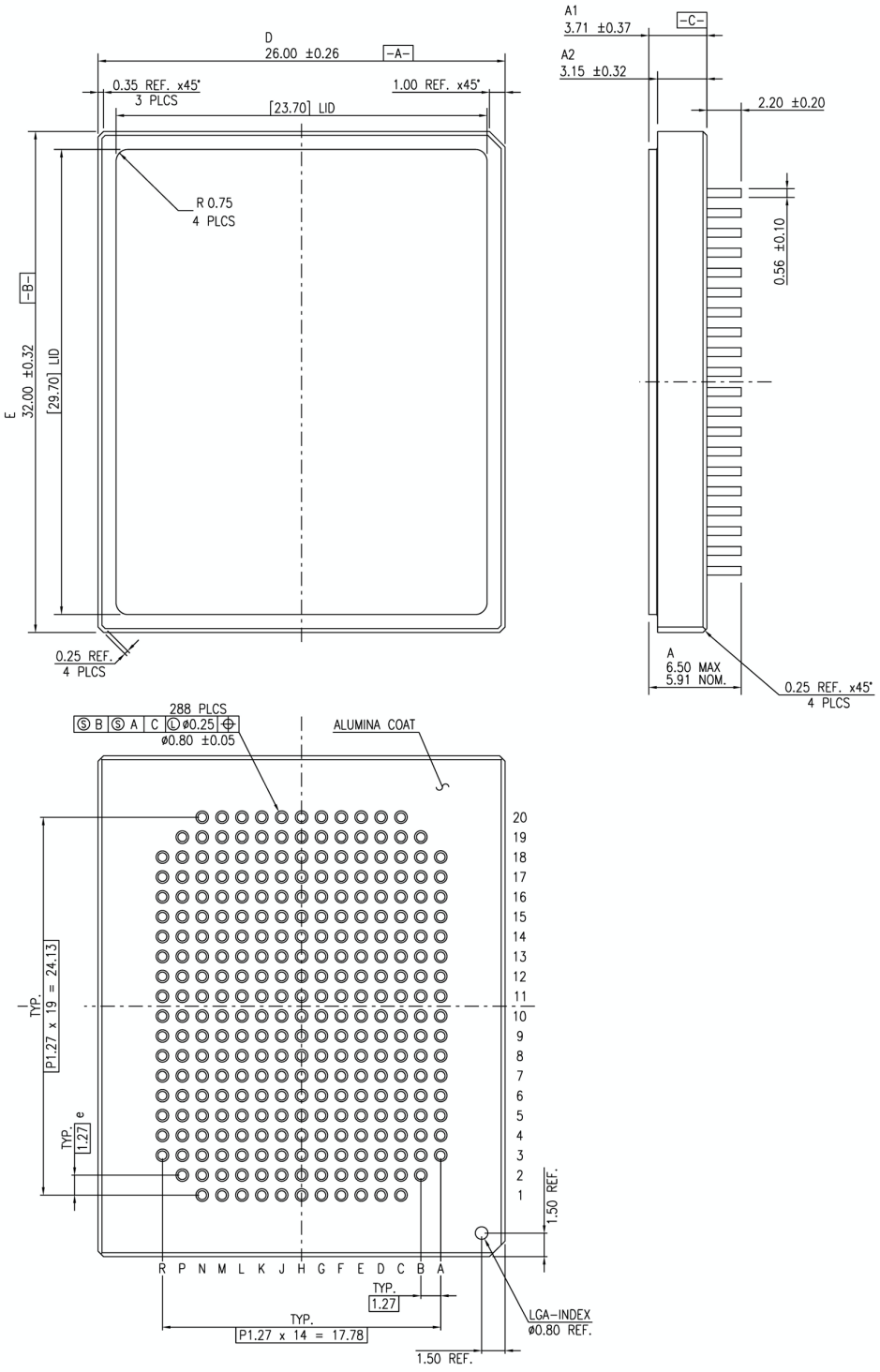

Figure 9. 288-Lead CCGA

Notes:

1) Package material: opaque 90% minimum alumina ceramic.
2) All exposed metal areas are gold plated over electroplated nickel undercoating per MIL-PRF-38535.
3) Lid is connected to VSS.

Packaging

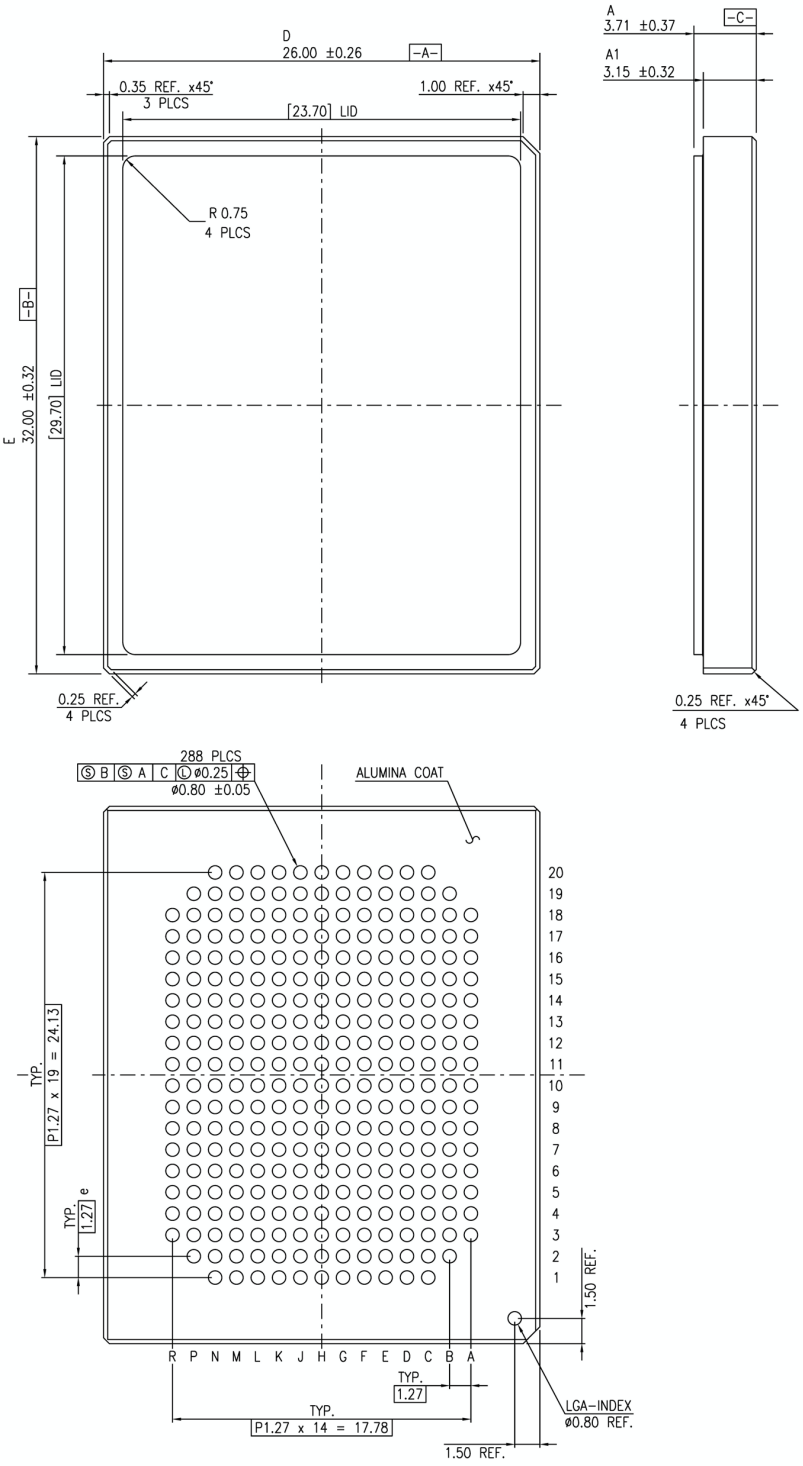

Figure 10. 288-Lead CLGA

Notes:

1) Package material: opaque 90% minimum alumina ceramic.
2) All exposed metal areas are gold plated over electroplated nickel undercoating per MIL-PRF-38535.
3) Lid is connected to VSS.

80 Megabit Flow-thru SSRAM

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Packaging

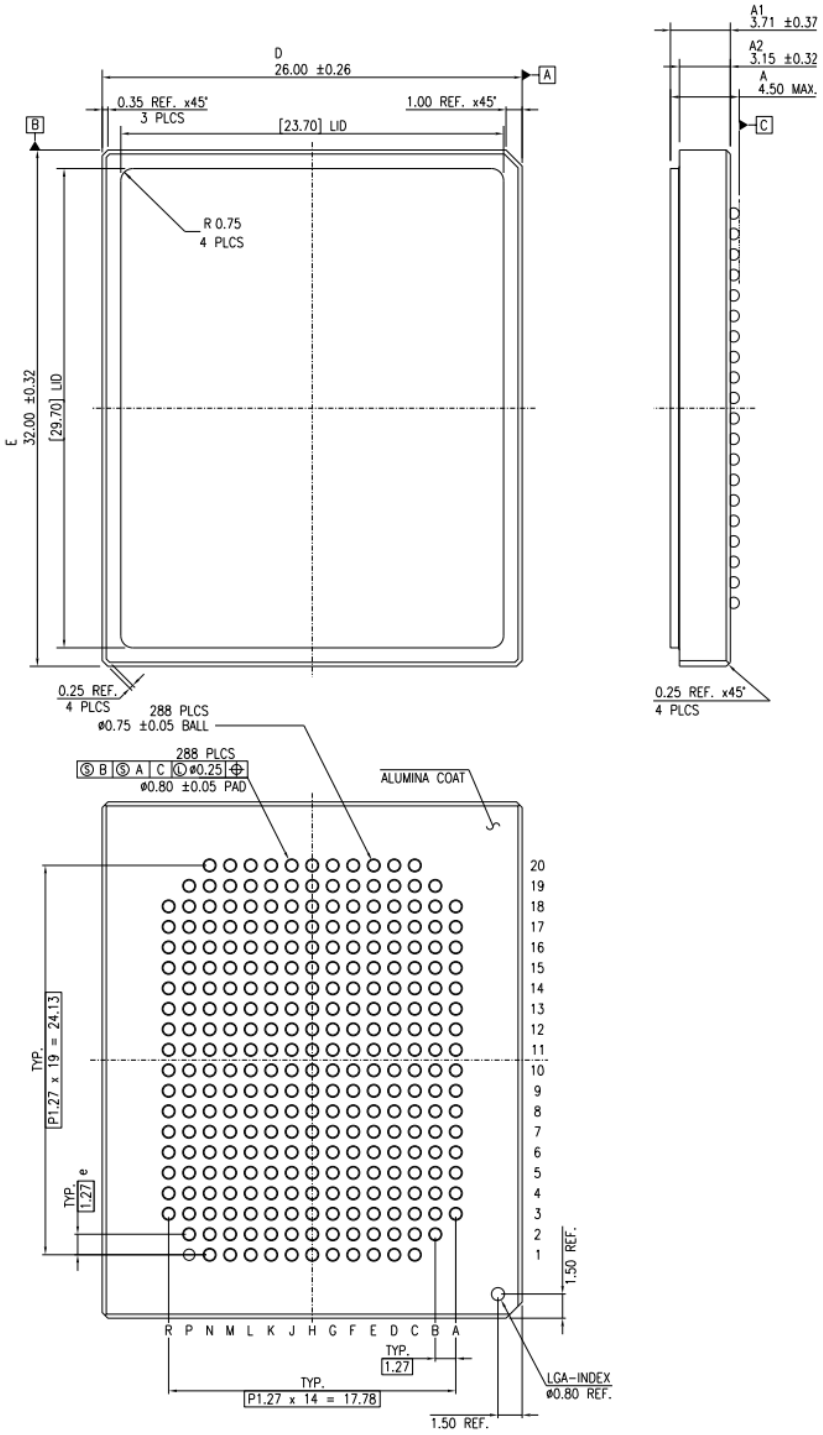

Figure 11. Advanced 288-lead CBGA, Ball dimensions (A, A1, A2) are subject to change

Notes:

1) Package material: opaque 90% minimum alumina ceramic.
2) All exposed metal areas are gold plated over electroplated nickel undercoating per MIL-PRF-38535.
3) Lid is connected to VSS.
4) Ball drop size is 0.75mm.

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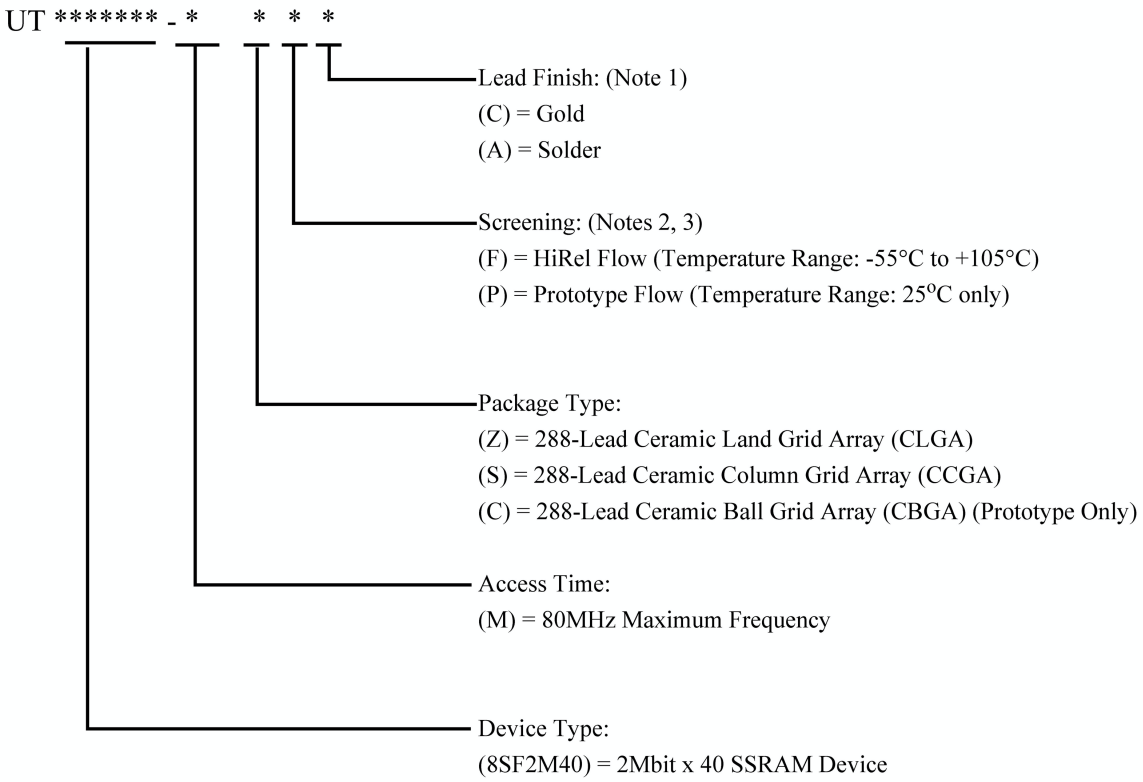
Ordering Information

2M x 40 SSRAM



Notes:

1) Lead finish is per the table below.
2) Prototype Flow per CAES Manufacturing Flows Document. Devices are tested at 25°C only. Radiation is neither tested nor guaranteed.
3) HiRel flow per CAES Manufacturing Flows Document. Radiation is neither tested nor guaranteed.

Package Option	Associated Lead Finish Option
(Z) 288-CLGA	(C) Gold
(S) 288-CCGA	(A) Hot Solder Dipped
(C) 288-CBGA	(A) Hot Solder Dipped

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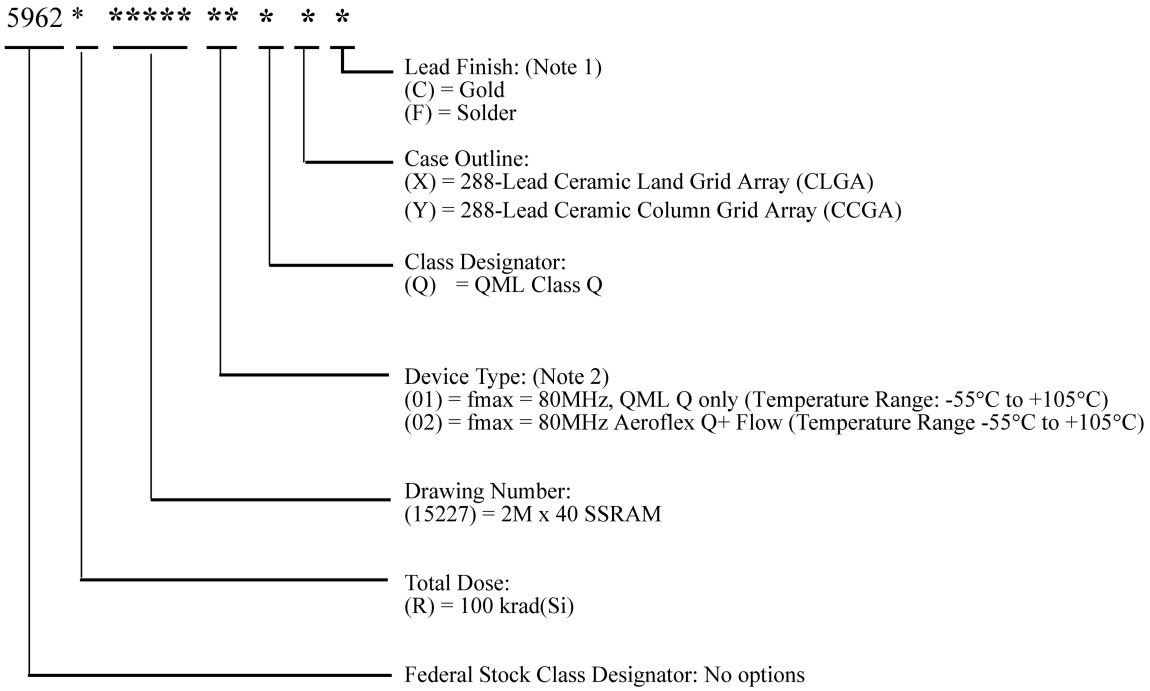
2M x 40 SSRAM: SMD



Notes:

1) Lead finish is per the table below.
2) CAES Q+ assembly flow, as defined in section 4.2.2.d of the SMD, provides QML-Q product through the SMD that is manufactured with CAES QML-V flow.

Package Option	Associated Lead Finish Option
(X) 288-CLGA	(C) Gold
(F) 288-CCGA	(F) Hot Solder Dipped

DATASHEET

RELEASED 10/18

Data Sheet Revision History

Revision Date	Description of Change	Author
1-15	Release of Preliminary Datasheet	ML
6-15	**Page 1 & 23: Updated the SMD number**	ML
9-17	Page 1: Datasheet Released Page 4 and 10: READY pin 10K ohm pull-up requirement added to datasheet	ML
11-17	Page 22-23: Updated Order Information	ML
10-18	Page 12: Corrected Condition for I_{STBYQ} $V_{IN} \leq V_{IL}$	ML

DATASHEET

RELEASED 10/18

80 Megabit Flow-thru SSRAM

UT8SF2M40

Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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