

Octal D-Flip-Flops with Clear

# UT54ACS273E

## Features

- Contains eight flip-flops with single-rail outputs
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
  - Buffer/storage registers, shift registers, and pattern generators
- 0.6μm CRH CMOS process
  - Latchup immune
- High speed
- Low power consumption
- Wide power supply operating range from 3.0V to 5.5V
- Available QML Q or V processes
- 20-lead flatpack
- UT54ACS273E - SMD 5962-96578

## Description

The UT54ACS273E is a performance and voltage enhanced version of the UT54ACS273 positive-edge-triggered D-type flip-flop with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

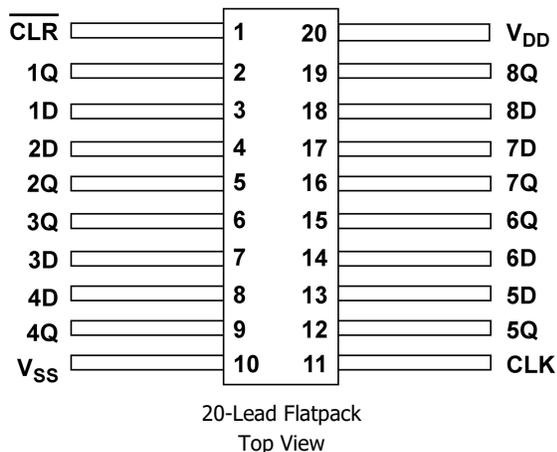
The device is characterized over full HiRel temperature range of -55°C to +125°C.

## Function Table

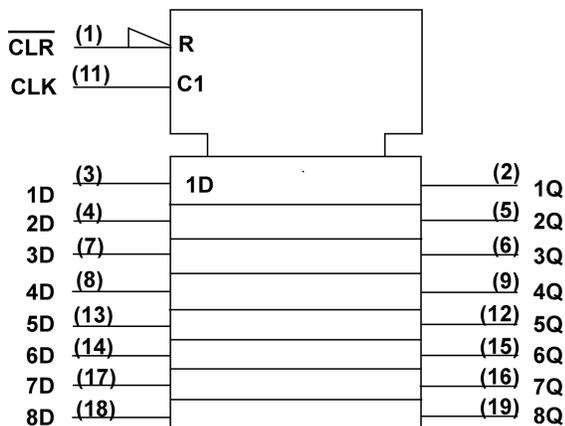
$\overline{\text{CLR}}$	Inputs		Output
	CLK	D <sub>x</sub>	Q <sub>x</sub>
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	No change

# UT54ACS273E

## Pinout



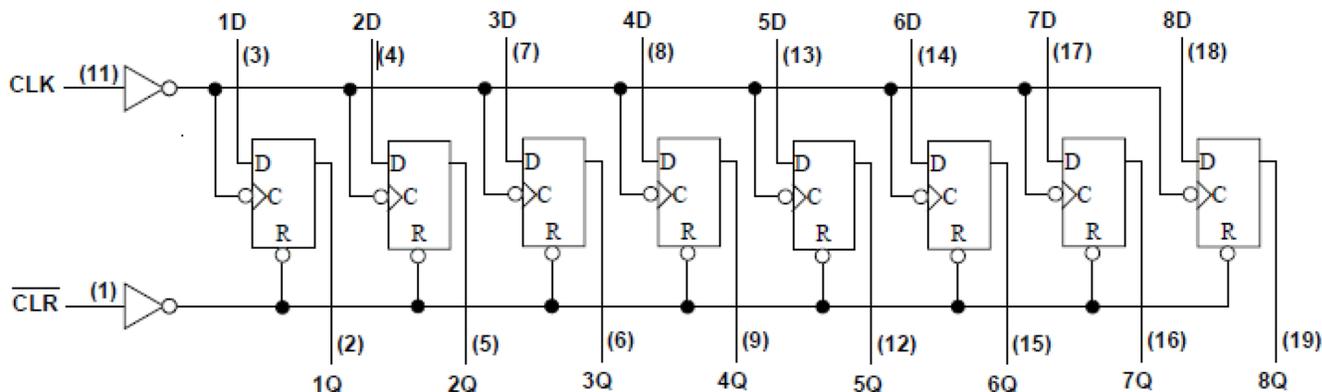
## Logic Symbol



**Note:**

1) Logic symbol in accordance with ANSI/IEEE standard 91-1984 and IEC Publication 617-12.

## Logic Diagram



Octal D-Flip-Flops with Clear

# UT54ACS273E

## Operational Environment <sup>1</sup>

Parameter	Limit	Units
Total Dose	1.0E6	rads(Si)
SEU Threshold <sup>2</sup>	108	MeV-cm <sup>2</sup> /mg
SEL Threshold	120	MeV-cm <sup>2</sup> /mg
Neutron Fluence	1.0E14	n/cm <sup>2</sup>

**Notes:**

- 1) Logic will not latch up during radiation exposure within the limits defined in the table.
- 2) Device storage elements are immune to SEU affects.

## Absolute Maximum Ratings <sup>1</sup>

Symbol	Parameter	Limit	Units
V <sub>DD</sub>	Supply voltage	-0.3 to 7.0	V
V <sub>I/O</sub>	Voltage any pin	-0.3 to V <sub>DD</sub> +0.3	V
T <sub>STG</sub>	Storage Temperature range	-65 to +150	°C
T <sub>J</sub>	Maximum junction temperature	+175	°C
T <sub>LS</sub>	Lead temperature (soldering 5 seconds)	+300	°C
Θ <sub>JC</sub>	Thermal resistance junction to case	15	°C/W
I <sub>I</sub>	DC input current	±10	mA
P <sub>D</sub> <sup>2</sup>	Maximum power dissipation permitted @ T <sub>C</sub> = +125°C	3.2	W

**Notes:**

- 1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other condition beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- 2) Per MIL-STD-883, method 1012.1, Section 3.4.1,  $P_D = (T_{J(max)} - T_{C(max)}) / \Theta_{JC}$

## Recommended Operating Conditions

Symbol	Parameter	Limit	Units
V <sub>DD</sub>	Supply voltage	3.0 to 5.5	V
V <sub>IN</sub>	Input voltage any pin	0 to V <sub>DD</sub>	V
T <sub>C</sub>	Temperature range	-55 to + 125	°C

# UT54ACS273E

## DC Electrical Characteristics for the UT54ACS273E <sup>7</sup>

( $V_{DD} = 3.0V$  to  $5.5V$ ;  $V_{SS} = 0V$ <sup>6</sup>;  $-55^{\circ}C < T_C < +125^{\circ}C$ )

Symbol	Parameter	Condition	MIN	MAX	Unit
$V_{IL}$	Low-level input voltage <sup>1</sup>	$V_{DD}$ from 3.0V to 5.5V		$0.3V_{DD}$	V
$V_{IH}$	High-level input voltage <sup>1</sup>	$V_{DD}$ from 3.0V to 5.5V	$0.7V_{DD}$		V
$I_{IN}$	Input leakage current	$V_{IN} = V_{DD}$ or $V_{SS}$	-1	+1	$\mu A$
$V_{OL}$	Low-level output voltage <sup>3</sup>	$I_{OL} = 100\mu A$		0.25	V
$V_{OH}$	High-level output voltage <sup>3</sup>	$I_{OH} = -100\mu A$	$V_{DD}-0.25$		V
$I_{OS1}$	Short-circuit output current <sup>2, 4</sup>	$V_O = V_{DD}$ and $V_{SS}$ $V_{DD}$ from 4.5V to 5.5V	-200	+200	mA
$I_{OS2}$	Short-circuit output current <sup>2, 4</sup>	$V_O = V_{DD}$ and $V_{SS}$ $V_{DD}$ from 3.0V to 3.6V	-100	+100	mA
$I_{OL1}$	Low level output current <sup>9</sup>	$V_{IN} = V_{DD}$ or $V_{SS}$ $V_{OL} = 0.4V$ $V_{DD}$ from 4.5V to 5.5V	+8		mA
$I_{OL2}$	Low level output current <sup>9</sup>	$V_{IN} = V_{DD}$ or $V_{SS}$ $V_{OL} = 0.4V$ $V_{DD}$ from 3.0V to 3.6V	+6		mA
$I_{OH1}$	High level output current <sup>9</sup>	$V_{IN} = V_{DD}$ or $V_{SS}$ $V_{OH} = V_{DD}-0.4V$ $V_{DD}$ from 4.5V to 5.5V	-8		mA
$I_{OH2}$	High level output current <sup>9</sup>	$V_{IN} = V_{DD}$ or $V_{SS}$ $V_{OH} = V_{DD}-0.4V$ $V_{DD}$ from 3.0V to 3.6V	-6		mA
$P_{total1}$	Power dissipation <sup>2, 8, 10</sup>	$C_L = 50pF$ $V_{DD} = 4.5V$ to $5.5V$		1.5	mW/MHz
$P_{total2}$	Power dissipation <sup>2, 8, 10</sup>	$C_L = 50pF$ $V_{DD} = 3.0V$ to $3.6V$		0.7	mW/MHz
$I_{DDQ}$	Quiescent Supply Current	$V_{IN} = V_{DD}$ or $V_{SS}$ $V_{DD}$ from 3.0V to 5.5V		25	$\mu A$
$C_{IN}$	Input capacitance <sup>5</sup>	$f = 1MHz$ $V_{DD} = 0V$		15	pF
$C_{OUT}$	Output capacitance <sup>5</sup>	$f = 1MHz$ $V_{DD} = 0V$		15	pF

# UT54ACS273E

**Notes:**

- 1) Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions:  $V_{IH} = V_{IH(min)} + 20\%$ ,  $- 0\%$ ;  $V_{IL} = V_{IL(max)} + 0\%$ ,  $- 50\%$ , as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to  $V_{IH(min)}$  and  $V_{IL(max)}$ .
- 2) Supplied as a design limit but not guaranteed or tested.
- 3) Per MIL-PRF-38535, for current density  $\leq 5.0E5$  amps/cm<sup>2</sup>, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
- 4) Not more than one output may be shorted at a time for maximum duration of one second.
- 5) Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and  $V_{SS}$  at frequency of 1MHz and signal amplitude of 50mV rms maximum.
- 6) Maximum allowable relative shift equals 50mV.
- 7) For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 method 1019 condition A up to the maximum TID level procured.
- 8) Power dissipation specified per switching output.
- 9) Guaranteed by characterization, but not tested.
- 10) Power does not include power contribution of any TTL output sink current.

## AC Electrical Characteristics for the UT54ACS273E <sup>2</sup>

( $V_{DD} = 3.0V$  to  $5.5V$ ;  $V_{SS} = 0V$  <sup>1</sup>;  $-55^\circ C < T_c < +125^\circ C$ )

Symbol	Parameter	Condition	$V_{DD}$	Minimum	Maximum	Unit
$t_{PLH1}$	CLK to Q	$C_L = 50pF$	4.5V to 5.5V	4	10.5	ns
			3.0V to 3.6V	4	15.5	
$t_{PHL1}$	CLK to Q	$C_L = 50pF$	4.5V to 5.5V	4	11	ns
			3.0V to 3.6V	4	16.5	
$t_{PHL2}$	$\overline{CLR}$ to Q	$C_L = 50pF$	4.5V to 5.5V	5	12	ns
			3.0V to 3.6V	5	17	
$f_{MAX}$	Maximum clock frequency	$C_L = 50pF$	4.5V to 5.5V		83	MHz
			3.0V to 5.5V		63	
$t_{SU1}$	Data setup time before CLK $\uparrow$	$C_L = 50pF$	3.0V to 5.5V	2		ns
$t_{SU2}$	$\overline{CLR}$ inactive setup time before CLK $\uparrow$	$C_L = 50pF$	3.0V to 5.5V	1		ns
$t_H$	Data hold time after CLK $\uparrow$	$C_L = 50pF$	3.0V to 5.5V	2		ns
$t_{W1}$	Minimum pulse width CLK high or low	$C_L = 50pF$	4.5V to 5.5V	4.5		ns
			3.0V to 5.5V	6.5		
$t_{W2}$	Minimum pulse width $\overline{CLR}$ low	$C_L = 50pF$	3.0V to 5.5V	4.5		ns

**Notes:**

- 1) Maximum allowable relative shift equals 50mV.
- 2) For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 method 1019 condition A up to the maximum TID level procured.

# UT54ACS273E

## Packaging

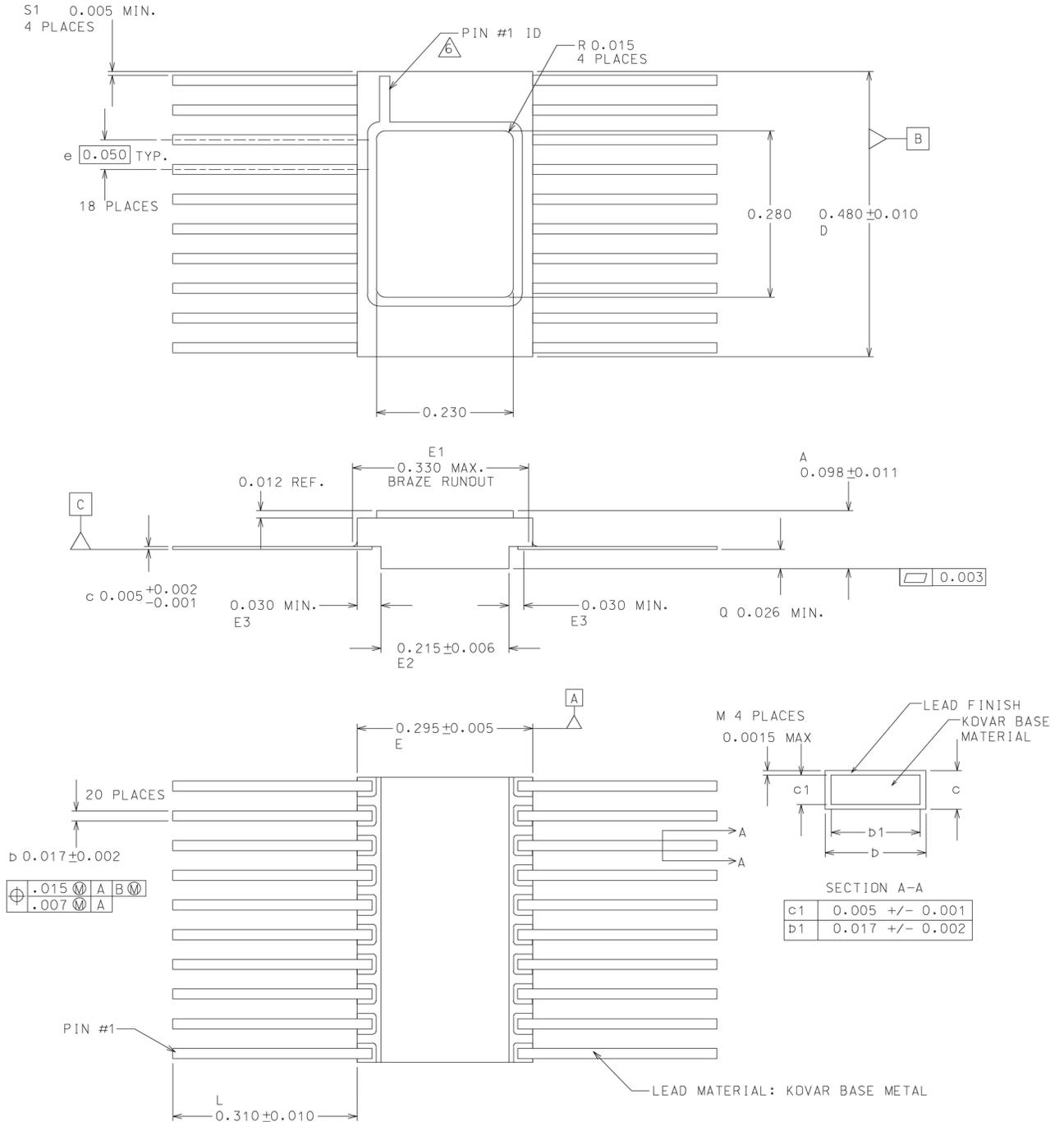


Figure 1. 20-lead Flatpack

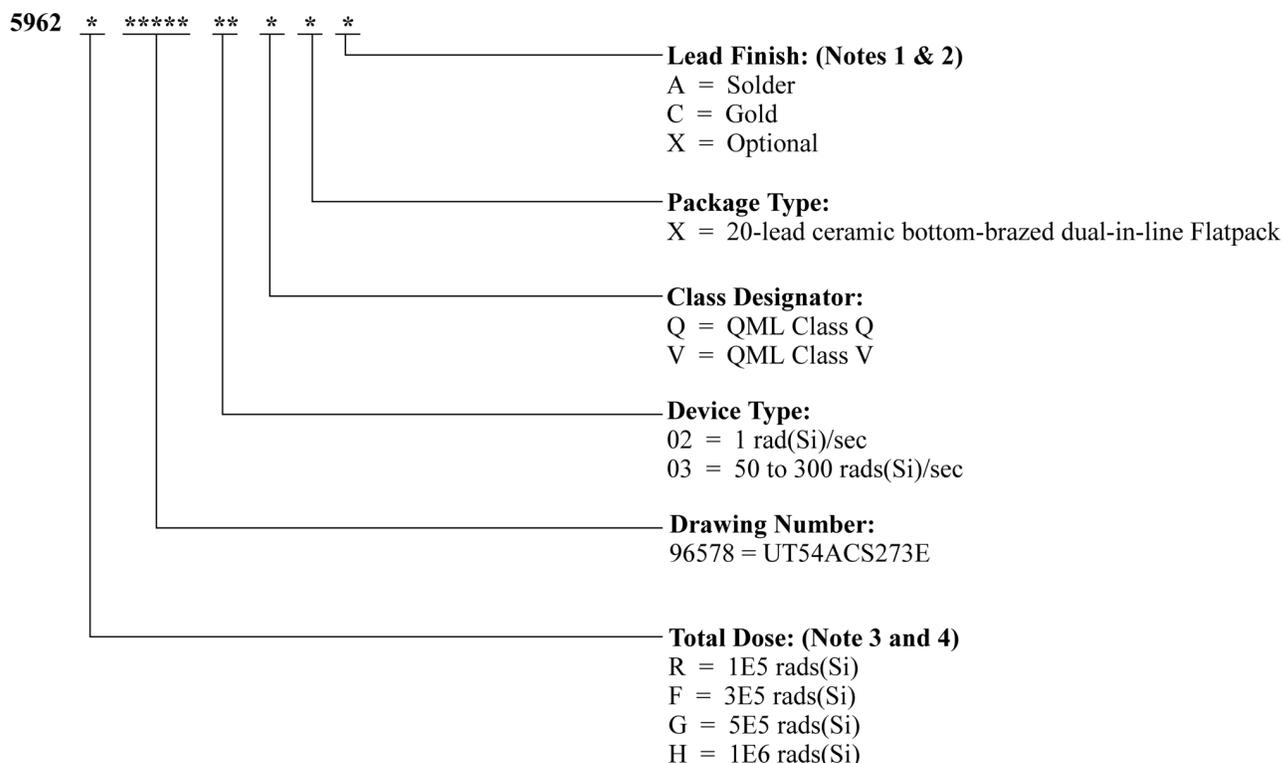
**Notes:**

- 1) All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
- 2) The lid is electrically connected to V<sub>SS</sub>.
- 3) Lead finishes are in accordance with MIL-PRF- 38535.
- 4) Dimension symbol is in accordance with MIL- PRF-38533.
- 5) Lead position and clarity are not measured.

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# UT54ACS273E

## Ordering Information: UT54ACS273E: SMD



**Notes:**

- 1) Lead finish (A, C, or X) must be specified.
- 2) If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
- 3) Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation Hardening. For prototype inquiries, contact factory.
- 4) Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) or 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

## Datasheet Revision History

Revision Date	Description of Change
March 2015	Initial Release of Datasheet

# UT54ACS273E

## Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet <b>is subject to change</b> . Specifications can be <b>TBD</b> and the part package and pinout are <b>not final</b> .
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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