DATASHEET

RELEASED 5/17/12

Schmitt CMOS 16-bit Bidirectional MultiPurpose Registered Transceiver

UT54ACS164646S

Features

- Flexible voltage operation
  - 5V bus to 3.3V bus
  - 3.3V bus to 5V bus
  - 5V bus to 5V bus
  - 3.3V bus to 3.3V bus
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Flow-through architecture optimizes PCB layout
- Cold- and Warm-sparing
  - 750kΩ minimum input impedance power-off
  - Guaranteed output tri-state while one power supply is "off" and the other is "on"
- Schmitt trigger inputs to filter noisy signals
- All inputs are 5V tolerant regardless of power supply voltage
- 0.6μm CRH CMOS Technology
- Operational Environment:
  - Total dose: 100K rad(Si)
  - Single Event Latchup immune>110 MeV-cm^2/mg
  - SEU Onset LET >75 MeV-cm^2/mg
- High speed, low power consumption
- Available QML Q or V processes
- Standard Microcircuit Drawing: 5962-06234
- Package:
  - 56-pin ceramic flatpack

Pin Description

Pin Names	Description
x$\overline{OE}$	Output Enable Input (Active Low)
xDIR	Direction Control Inputs
xAx	Side A Inputs or 3-State Outputs (3.3V Port)
xBx	Side B Inputs or 3-State Outputs (5V Port)
xSAB	Select real-time or stored A bus data to B bus
xSBA	Select real-time or stored B bus data to A bus
xCLKAB	Store A bus data
xCLKBA	Store B bus data

RELEASED 5/17/12

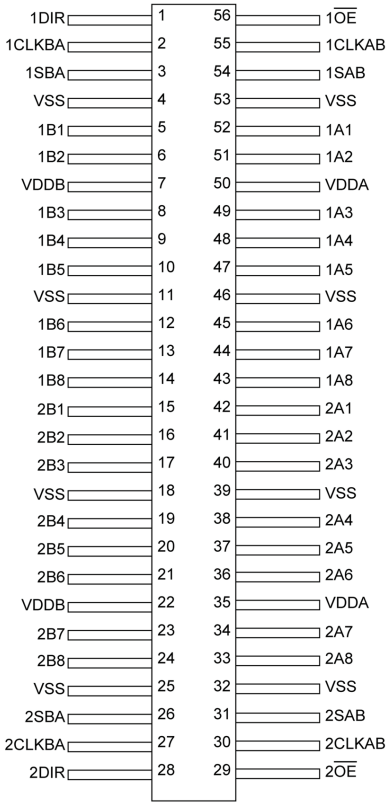
Schmitt CMOS 16-bit Bidirectional MultiPurpose Registered Transceiver

UT54ACS164646S

Description

The UT54ACS164646S is a 16-bit, MultiPurpose, registered, level shifting, bus transceiver consisting of D-type flip-flops, control circuitry, and 3-state outputs arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The high-speed, low power UT54ACS164646S transceiver is designed to perform multiple functions including: asynchronous two-way communication, signal buffering, voltage translation, cold- and warm- sparing. The device can be used as two independent 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the rising edge of the appropriate clock (xCLKAB or xCLKBA) input. With either V_{DD} supply equal to zero volts, the UT54ACS164646S outputs and inputs present a minimum impedance of 750kΩ making it ideal for "cold-spare" and "warm-spare" applications. By virtue of its flexible power supply interface, the UT54ACS164646S may operate as a 3.3-volt only, 5-volt only, or mixed 3.3V/5V bus transceiver.

The Output-enable ($x\overline{OE}$) and direction-control (xDIR) inputs are provided to control the tri-state function and input/output direction of the transceiver respectively. The select controls (xSAB and xSBA) select whether stored register data or real-time data is driven to the outputs as determined by the xDIR inputs. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Regardless of the selected operating mode ("real-time" or "recall"), a rising edge on the port input clocks (xCLKAB and xCLKBA) will latch the corresponding I/O states into their respective registers. Furthermore, when a data port is isolated ($x\overline{OE}$ = high), A-port data may be stored into its corresponding register while B-port data may be independently stored into its corresponding registers. Therefore, when an output function is disabled, the input function is still enabled and may be used to store and transmit data. Lastly, only one of the two buses, xA-port or xB-port, may be driven at a time.

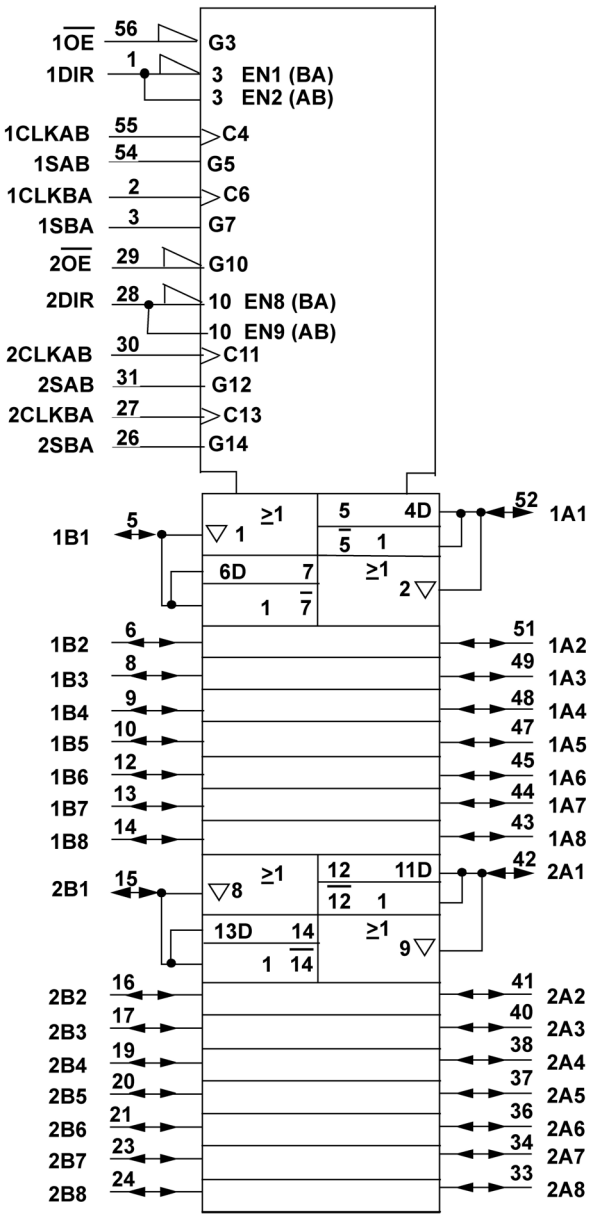


56-Lead Flatpack
Pinout

Schmitt CMOS 16-bit Bidirectional MultiPurpose Registered Transceiver

UT54ACS164646S

Logic Symbol



Power Table

Port B	Port A	Operation
5 Volts	3.3 Volts	Voltage Translator
5 Volts	5 Volts	Non Translating
3.3 Volts	3.3 Volts	Non Translating
V_{SS}	V_{SS}	Cold Spare
V_{SS}	3.3V or 5V	Port A Warm Spare
3.3V or 5V	V_{SS}	Port B Warm Spare

I/O Guidelines

Control signals xDIR, $x\overline{OE}$, xSAB, xSBA, xCLKAB, and xCLKBA are powered by V_{DDA}. All inputs are 5-volt tolerant. When VDD2 is at 3.3 volts, either 3.3 or 5-volt CMOS logic levels can be applied to all control inputs. Control signals DIRx, /OEx, xSAB, xSBA, xCLKAB, and xCLKBA are powered by VDDA. All inputs are 5-volt tolerant. Additionally, it is recommended that all unused inputs be tied to VSS through a 1KΩ to 10KΩ resistor. It's good design practice to tie the unused input to VSS via a resistor to reduce noise susceptibility. The resistor protects the input pin by limiting the current from high going variations in VSS. The number of inputs that can be tied to the resistor pull-down can vary. It is up to the system designer to choose how many inputs are tied together by figuring out the max load the part can drive while still meeting system performance specs. Input signal transitions should be driven to the device with a rise and fall time that is <100ms.

Function Table

Inputs						Data I/O[+]		Operation or Function
$x\overline{OE}$	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xA1-xA8	xB1-xB8	
X	X	↑	X	X	X	Input	Unspecified	Store A, B unspecified[+]
X	X	X	↑	X	X	Unspecified	Input	Store B, A unspecified[+]
H	X	↑	↑	X	X	Input	Input	Store A and B data[+]
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Recall stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B Bus
L	H	H or L	X	H	X	Input	Output	Recall stored A data to B bus

Note:

1) [+]The data-output functions may be enabled or disabled by various signals $x\overline{OE}$ or xDIR. Data-input functions are always enabled, i.e. data at the bus terminals is stored on every low-to-high transition of the clock inputs.

Power Application Guidelines

For proper operation connect power to all V_{DDx} pins and ground all V_{SS} pins (i.e., no floating V_{DDx} or V_{SS} input pins). By virtue of the UT54ACS164646S warm-spare feature, power supplies V_{DDB} and V_{DDA} may be applied to the device in any order. To ensure the device is in cold-spare mode, both supplies, V_{DDB} and V_{DDA} , must be equal to V_{SS} +/- 0.3V. Warmspare operation is in effect when one power supply is >1V and the other power supply is equal to V_{SS} +/- 0.3V. If V_{DDB} has a power-on ramp rate longer than 1 second, then V_{DDA} should be powered-on first to ensure proper control of xDIR and $x\overline{OE}$. During normal operation of the part, after power-up, ensure $V_{DDB} \geq V_{DDA}$.

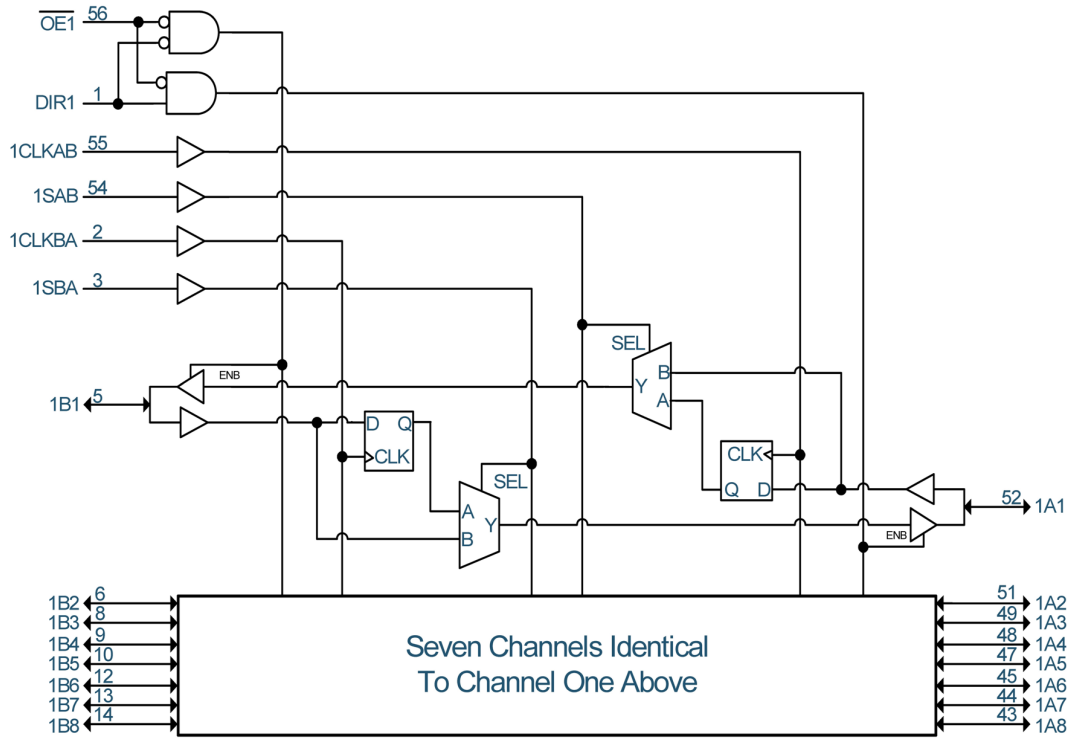
By definition, warm sparing occurs when half of the chip receives its normal VDD supply value while the VDD supplying the other half of the chip is set to 0.0V. When the chip is 'warm spared', the side that has its VDD set to a normal operational value is 'actively' tristated because the chip's internal OE signal is forced low. The side of the chip that has VDD set to 0.0V is 'passively' tristated by the cold spare circuitry.

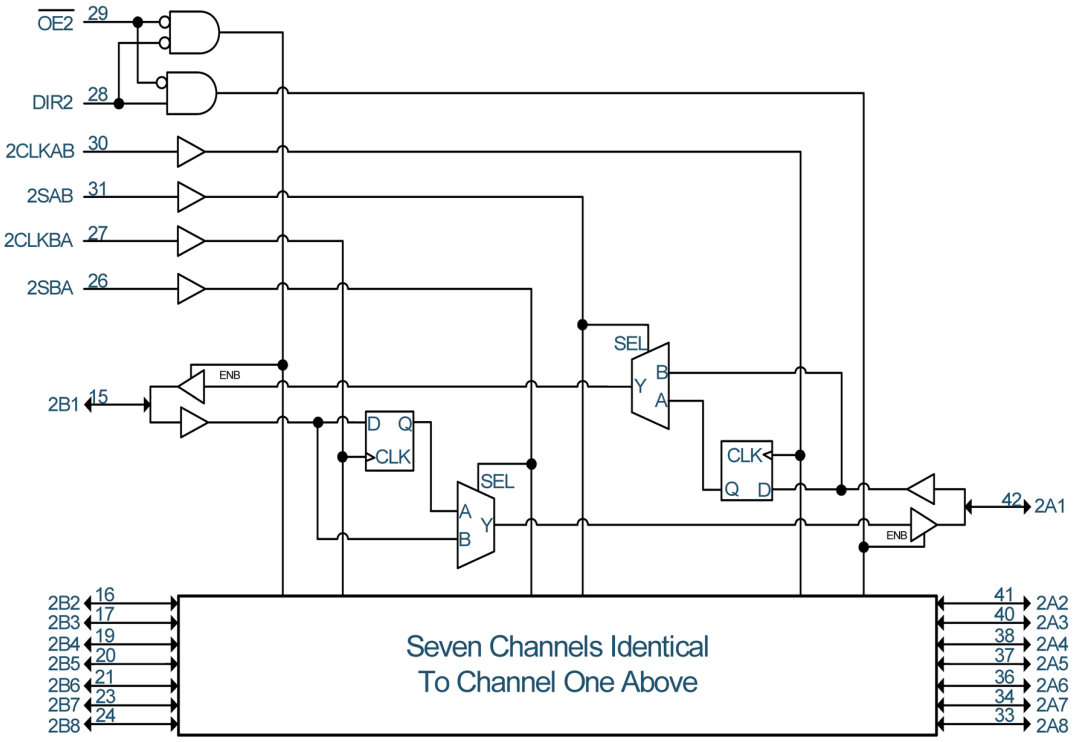
In order to minimize transients and current consumption, the user is encouraged to first apply a high level to the $x\overline{OE}$ pins and then power down the appropriate supply.

Schmitt CMOS 16-bit Bidirectional MultiPurpose Registered Transceiver

UT54ACS164646S

Logic Diagram





Schmitt CMOS 16-bit Bidirectional MultiPurpose Registered Transceiver

UT54ACS164646S

Operational Environment [1]

Parameter	Limit	Units
Total Dose	1.0E5	rad(Si)
SEL LET Threshold	>110	MeV-cm^2/mg
SEU Onset LET Threshold [4]	>97 @4.5V, >74@ 3.0V	MeV-cm^2/mg
SEU Error Rate [2]	Immune @4.5V, 6.3E-10 @3.0V	errors/bit-day
Neutron Fluence [3]	1.0E14	n/cm^2

Notes:

1) Logic will not latchup during radiation exposure within the limits defined in the table.
2) Adams 90% worst case particle environment, geosynchronous orbit, 100mils of Aluminum shielding
3) Not tested, inherent of CMOS technology.
4) Core logic is driven by V_{DDB}.

Absolute Maximum Ratings [1]

Symbol	Parameter	Limit (Mil Only)	Units
$V_{I/OB}$ (Port B) [2]	Voltage any pin	-0.3 to 6.0	V
$V_{I/OA}$ (Port A) [2]	Voltage any pin	-0.3 to 6.0	V
V_{DDB}	Supply voltage	-0.3 to 6.0	V
V_{DDA}	Supply voltage	-0.3 to 6.0	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
Θ_{JC}	Thermal resistance junction to case	20	°C/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation	250	mW

Notes:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2) For cold spare mode (V_{DDx} = V_{SS} +/- 0.3V), $V_{I/Ox}$ may be -0.3V to the maximum recommended operating V_{DDx} + 0.3V.

Dual Supply Operating Conditions

Symbol	Parameter	Limit	Units
V_{DDB} [1]	Supply voltage	3.0 to 3.6 or 4.5 to 5.5	V
V_{DDA} [1]	Supply voltage	3.0 to 3.6 or 4.5 to 5.5	V
V_{INB} (Port B) [2]	Input voltage any pin	0 to V_{DDB}	V
V_{INA} (Port A) [2]	Input voltage any pin	0 to V_{DDA}	V
T_C	Temperature range	-55 to +125	°C

Notes:

1) During normal operation, $V_{DDB} \geq V_{DDA}$.
2) All input pins are 5-volt tolerant inputs powered by V_{DDA}. Therefore, when V_{DDA} is at 3.3 volts, either 3.3 or 5-volt CMOS logic levels can be applied to all control inputs.

DC Electrical Characteristics [1]

(T_C =-55°C +125°C); Unless otherwise noted, Tc is per the temperature ordered.

Symbol	Parameter	Condition		MIN	MAX	Unit
V_T+	Schmitt Trigger, positive going threshold [2]	V_{DDx} from 3.0V to 5.5V			.7V_{DDx}	V
V_T-	Schmitt Trigger, negative going threshold [2]	V_{DDx} from 3.0V to 5.5V		.3V_{DDx}		V
V_{H1}	Schmitt Trigger range of hysteresis	V_{DDx} from 4.5V to 5.5V		0.7		V
V_{H2}	Schmitt Trigger range of hysteresis	V_{DDx} from 3.0V to 3.6V		0.5		V
I_{IN}	Input leakage current	V_{DDx} from 3.6V to 5.5V V_{IN} = V_{DDx} or V_{SS}		-1	1	µA
I_{OZ}	Three-state output leakage current	V_{DDx} from 3.6 to 5.5 V_{IN} = V_{DDx} or V_{SS}		-1	1	µA
I_{CS}	Cold sparing input leakage current [3] (any pin)	V_{IN} = 5.5V V_{DDB} = V_{DDA} = V_{SS}		-5	7	µA
I_{WS}	Warm sparing input leakage current [3] (any pin)	V_{IN} = 5.5; V_{DDA} = 3V to 5.5V & V_{DDB} = V_{SS} or V_{DDB} = 3V to 5.5V & V_{DDA} = V_{SS}		-3	3	µA
I_{OS1}	Short-circuit output current [6, 10]	V_O = V_{DDx} or V_{SS} V_{DDx} from 4.5 to 5.5		-200	200	mA
I_{OS2}	Short-circuit output current [6, 10]	V_O = V_{DDx} or V_{SS} V_{DDx} from 3.0 to 3.6		-100	100	mA
V_{OL1}	Low-level output voltage [4]	V_{DDx} = 4.5V; I_{OL}= 8mA			0.4	V
		V_{DDx} = 4.5V; I_{OL}= 100µA			0.2	
V_{OL2}	Low-level output voltage [4]	V_{DDx} = 4.5V I_{OL}= 12mA	-55°C, 25°C		0.4	V
			+125°C		0.55	
V_{OL3}	Low-level output voltage [4]	V_{DDx} = 3.0V; I_{OL}= 8mA			0.5	V
		V_{DDx} = 3.0V; I_{OL}= 100µA			0.2	V
V_{OL4}	Low-level output voltage [4]	V_{DDx} = 3.0V I_{OL}= 12mA	-55°C, 25°C		0.5	V
			+125°C		0.6	V
V_{OH1}	High-level output voltage [4]	V_{DDx} = 4.5V; I_{OH}= -8mA		V_{DDx} - 0.5		V
		V_{DDx} = 4.5V; I_{OH}= -100µA		V_{DDx} - 0.2		
V_{OH2}	High-level output voltage [4]	V_{DDx} = 4.5V I_{OL}= -12mA	-55°C, 25°C	V_{DDx} - 0.6		V
			+125°C	V_{DDx} - 0.7		V
V_{OH3}	High-level output voltage [4]	V_{DDx} = 3.0V; I_{OH}= -8mA		V_{DDx} - 0.6		V
		V_{DDx} = 3.0V; I_{OH}= -100µA		V_{DDx} - 0.2		
V_{OH4}	High-level output voltage [4]	V_{DDx} = 3.0V I_{OL}= -12mA	-55°C, 25°C	V_{DDx} - 0.8		V
			+125°C	V_{DDx} - 0.95		V

Symbol	Parameter	Condition	MIN	MAX	Unit
P_{total1}	Power dissipation [5, 7, 8]	C_L = 20pF V_{DDB} = V_{DDA} = 4.5V to 5.5V		2.0	mW/ MHz
P_{total2}	Power dissipation [5, 7, 8]	C_L = 20pF V_{DDB} = V_{DDA} = 3.0V to 3.6V		1.5	mW/ MHz
I_{DDQ}	Standby Supply Current V_{DDB} or V_{DDA} Pre-Rad 25°C	VIN = VDDx or VSS VDDB = VDDA = 5.5V $x\overline{OE}$ = VDDA		10	µA
	Standby Supply Current V_{DDB} or V_{DDA} Pre-Rad -55°C, +125°C			100	
	Standby Supply Current V_{DDB} or V_{DDA} Post-Rad 25°C			100	
C_{IN}	Input capacitance [9]	f = 1MHz V_{DDx} from 3.0V to 5.5V		15	pF
C_{OUT}	Output capacitance [9]	f = 1MHz V_{DDx} from 3.0V to 5.5V		15	pF

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25×C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) All specifications valid for radiation dose ≤ 1E5 rad(Si) per MIL-STD-883, Method 1019.
2) Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: V_{IH} = V_{IH}(min) + 20%, - 0%; V_{IL} = V_{IL}(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL}(max).
3) This parameter is uneffected by the state of $x\overline{OE}$ or xDIR.
4) Per MIL-PRF-38535, for current density ≤ 5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF-MHz.
5) Guaranteed by characterization.
6) Not more than one output may be shorted at a time for maximum duration of one second.
7) Power does not include power contribution of any CMOS output sink current.
8) Power dissipation specified per switching output.
9) Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
10) Supplied as a design limit, but not guaranteed or tested.

Schmitt CMOS 16-bit Bidirectional MultiPurpose Registered Transceiver

UT54ACS164646S

AC Electrical Characteristics *[1] (Port B = 5 Volt, Port A = 3.3 Volt)

(V_{DDB} = 5V ±10%; V_{DDA} = 3.3V ±0.3V); Unless otherwise noted, Tc is per the temperature ordered.

Symbol	Parameter	Minimum	Maximum	Unit
t_{PLH1}	Propagation delay Data to Bus	3.5	9	ns
t_{PHL1}	Propagation delay Data to Bus	3.5	9	ns
t_{PLH2}	xCLKAB↑ or xCLKBA↑ to Bus	4.5	10.5	ns
t_{PHL2}	xCLKAB↑ or xCLKB ↑ to Bus	4.5	10.5	ns
t_{PLH3} [2]	xSAB↑ or xSBA↑ to Bus	4	10.5	ns
t_{PHL3} [2]	xSAB↑ or xSBA↑ to Bus	4	10.5	ns
t_{PLH4} [2]	xSBA↓ or xSAB ↓ to Bus	4	10.5	ns
t_{PHL4} [2]	xSBA↓ or xSAB ↓ to Bus	4	10.5	ns
t_{PZH1}	Output enable time $x\overline{OE}$ to Bus	4	10	ns
t_{PZL1}	Output enable time $x\overline{OE}$ to Bus	4	10	ns
t_{PLZ1}	Output disable time $x\overline{OE}$ to Bus high impedance	3	10	ns
t_{PHZ1}	Output disable time $x\overline{OE}$ to Bus high impedance	3	10	ns
t_{PZH2} [3]	Output enable time xDIR to Bus	3	12	ns
t_{PZL2} [3]	Output enable time xDIR to Bus	3	12	ns
t_{PLZ2} [3]	Output disable time xDIR to Bus high impedance	3	12	ns
t_{PHZ2} [3]	Output disable time xDIR to Bus high impedance	3	12	ns
t_{SKEW} [4]	Skew between outputs		800	ps
t_{OST} [5]	Differential skew between outputs		1500	ps
t_{PART} [6]	Part to part skew		500	ps

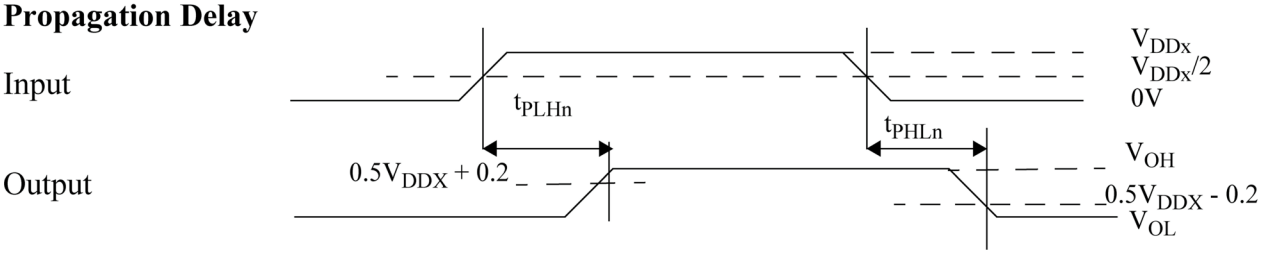
Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

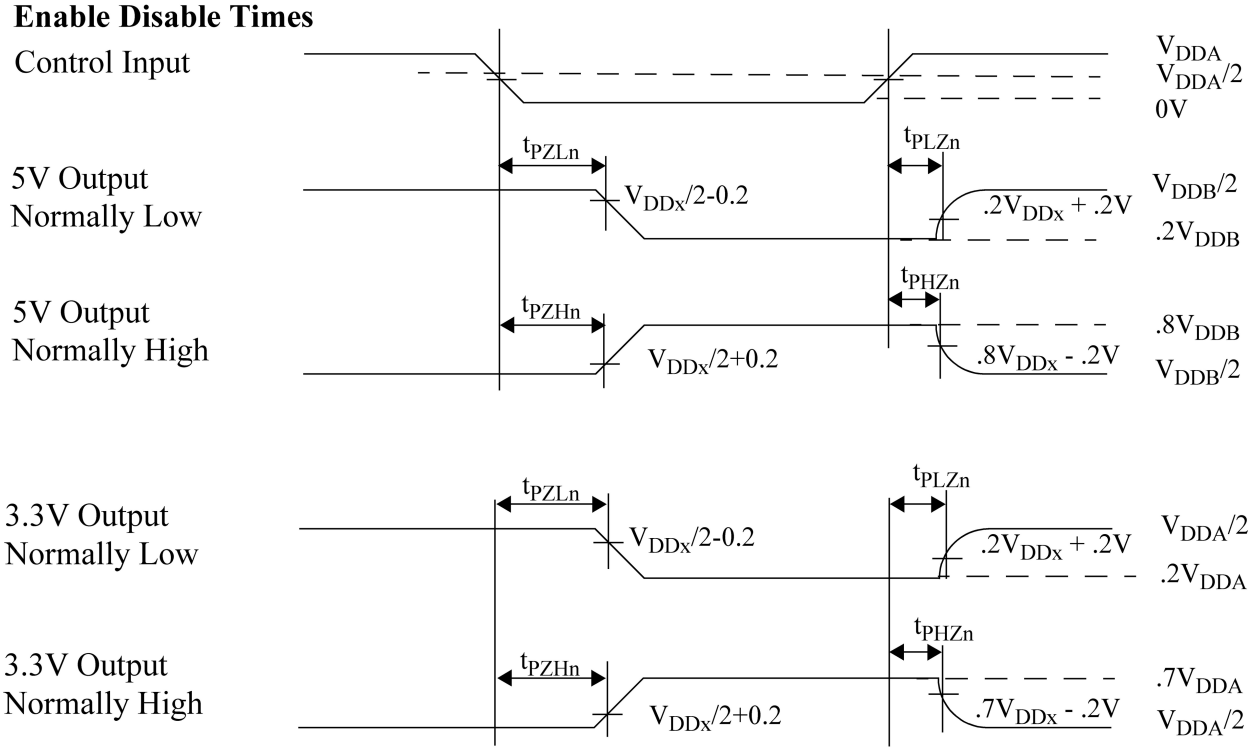
1) All specifications valid for radiation dose ≤ 1E5 rad(Si) per MIL-STD-883, Method 1019.
2) These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
3) xDIR to bus times are guaranteed by design, but not tested. $x\overline{OE}$ to bus times are tested.
4) Output skew is defined as a comparison of any two output transitions of the same type at the saame temperature and voltage for the same port within the same byte: 1A1 through 1A8 are compared high-to-low versus high-to-low and low-to-high versus low-to-high; similarly 1B1 through 1B8 are compared, 2A1 through 2A8 are compared, and 2B1 through 2B8 are compared.
5) Differential output skew is defined as a comparison of any two output transitions of opposite types on the same type at the same temperature and voltage for the same port within the same byte: 1A1 through 1A8 are compared high-to-low versus low-to-high; similarly 1B1 through 1B8 are compared, 2A1 through 2A8 are compared, and 2B1 through 2B8 are compared.
6) Guaranteed by characterization, but not tested.

UT54ACS164646S

Propagation Delay



Enable Disable Times



AC Timing Waveforms for Level Translation
(e.g. V_{DDA} = 3.3V +/- 0.3V and V_{DDB} = 5V +/- 10%)

Schmitt CMOS 16-bit Bidirectional MultiPurpose Registered Transceiver

UT54ACS164646S

AC Electrical Characteristics *[1] (Port A = Port B, 5 Volt Operation)

(V_{DDB} = 5V ±10%; V_{DDA} = 5V ±10%) (T_C = -55°C to +125°C)**;** Unless otherwise noted, Tc is per the temperature ordered

Symbol	Parameter	Minimum	Maximum	Unit
t_{PLH1}	Propagation delay Data to Bus	3.5	7.5	ns
t_{PHL1}	Propagation delay Data to Bus	3.5	7.5	ns
t_{PLH2}	xCLKAB ↑ or xCLKBA ↑ to Bus	4	9	ns
t_{PHL2}	xCLKAB ↑ or xCLKBA ↑ to Bus	4	9	ns
t_{PLH3} [2]	xSAB ↑ or xSBA ↑ to Bus	3	8	ns
t_{PHL3} [2]	xSAB ↑ or xSBA ↑ to Bus	3	8	ns
t_{PLH4} [2]	xSBA ↓ or xSAB ↓ to Bus	3	8	ns
t_{PHL4} [2]	xSBA ↓ or xSAB ↓ to Bus	3	8	ns
t_{PZH1}	Output enable time $x\overline{OE}$ to Bus	3.5	9	ns
t_{PZL1}	Output enable time $x\overline{OE}$ to Bus	3.5	9	ns
t_{PLZ1}	Output disable time $x\overline{OE}$ to Bus high impedance	3	8	ns
t_{PHZ1}	Output disable time $x\overline{OE}$ to Bus high impedance	3	8	ns
t_{PZH2} [3]	Output enable time xDIR to Bus	3	11	ns
t_{PZL2} [3]	Output enable time xDIR to Bus	3	11	ns
t_{PLZ2} [3]	Output disable time xDIR to Bus high impedance	3	11	ns
t_{PHZ2} [3]	Output disable time xDIR to Bus high impedance	3	11	ns
t_{SKEW} [4]	Skew between outputs		600	ps
t_{OST} [5]	Differential outputs skew		1500	ps
t_{PART} [6]	Part to part skew		500	ps

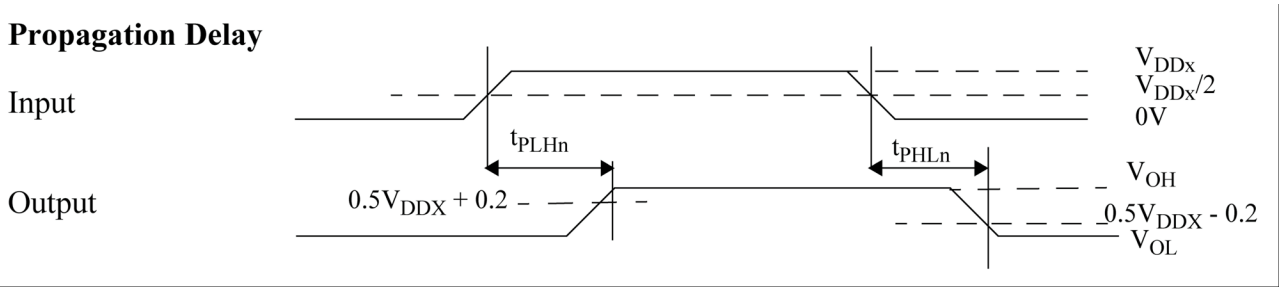
Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

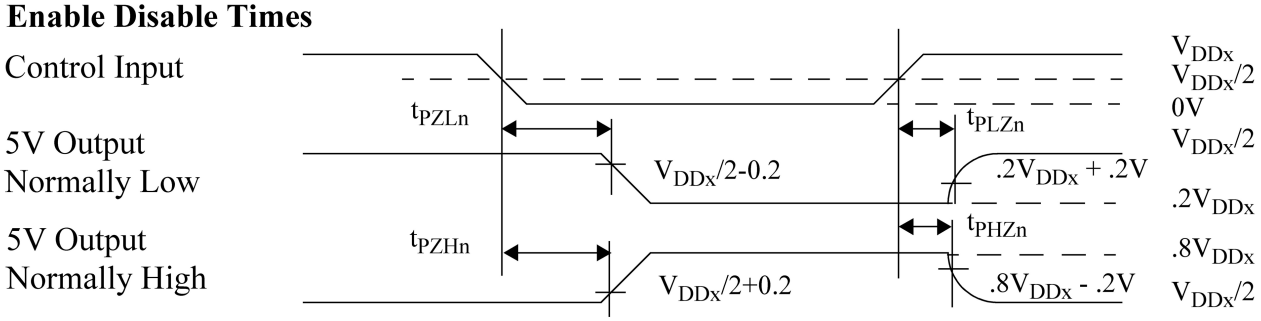
1) All specifications valid for radiation dose ≤ 1E5 rad(Si) per MIL-STD-883, Method 1019.
2) These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
3) xDIR to bus times are guaranteed by design, but not tested. $x\overline{OE}$ to bus times are tested.
4) Output skew is defined as a comparison of any two output transitions of the same type at the same temperature and voltage for the same port within the same byte: 1A1 through 1A8 are compared high-to-low versus high-to-low and low-to-high versus low-to-high; similarly 1B1 through 1B8 are compared, 2A1 through 2A8 are compared, and 2B1 through 2B8 are compared.
5) Differential output skew is defined as a comparison of any two output transitions of opposite types on the same type at the same temperature and voltage for the same port within the same byte: 1A1 through 1A8 are compared high-to-low versus low-to-high; similarly 1B1 through 1B8 are compared, 2A1 through 2A8 are compared, and 2B1 through 2B8 are compared.
6) Guaranteed by characterization, but not tested.

UT54ACS164646S

Propagation Delay



Enable Disable Times



AC Timing Waveforms for 5-Volt only operation
(e.g. $V_{DDA} = V_{DDB} = 5V +/- 10\%$)

Schmitt CMOS 16-bit Bidirectional MultiPurpose Registered Transceiver

UT54ACS164646S

AC Electrical Characteristics *[1] (Port A = Port B, 3.3 Volt Operation)

(V_{DDB} = V_{DDA} = 3.3V ±0.3V) (T_C = -55°C to +125°C); Unless otherwise noted, Tc is per the temperature ordered

Symbol	Parameter	Minimum	Maximum	Unit
t_{PLH1}	Propagation delay Data to Bus	4	10	ns
t_{PHL1}	Propagation delay Data to Bus	4	10	ns
t_{PLH2}	xCLKAB ↑ or xCLKBA ↑ to Bus	4.5	12.5	ns
t_{PH2}	xCLKAB ↑ or xCLKB ↑ to Bus	4.5	12.5	ns
t_{PLH3} [2]	xSAB ↑ or xSBA ↑ to Bus	4.5	11	ns
t_{PHL3} [2]	xSAB ↑ or xSBA ↑ to Bus	4.5	11	ns
t_{PLH4} [2]	xSBA ↓ or xSAB ↓ to Bus	4.5	11	ns
t_{PHL4} [2]	xSBA ↓ or xSAB ↓ to Bus	4.5	11	ns
t_{PZH1}	Output enable time $x\overline{OE}$ to Bus	4	11	ns
t_{PZL1}	Output enable time $x\overline{OE}$ to Bus	4	11	ns
t_{PLZ1}	Output disable time $x\overline{OE}$ to Bus high impedance	4	10	ns
t_{PHZ1}	Output disable time $x\overline{OE}$ to Bus high impedance	4	10	ns
t_{PZH2} [3]	Output enable time xDIR to Bus	3	13	ns
t_{PZL2} [3]	Output enable time xDIR to Bus	3	13	ns
t_{PLZ2} [3]	Output disable time xDIR to Bus high impedance	3	13	ns
t_{PHZ2} [3]	Output disable time xDIR to Bus high impedance	3	13	ns
t_{SKEW} [4]	Skew between outputs		700	ps
t_{OST} [5]	Differential outputs skew		1500	ps
t_{PART} [6]	Part to part skew		500	ps

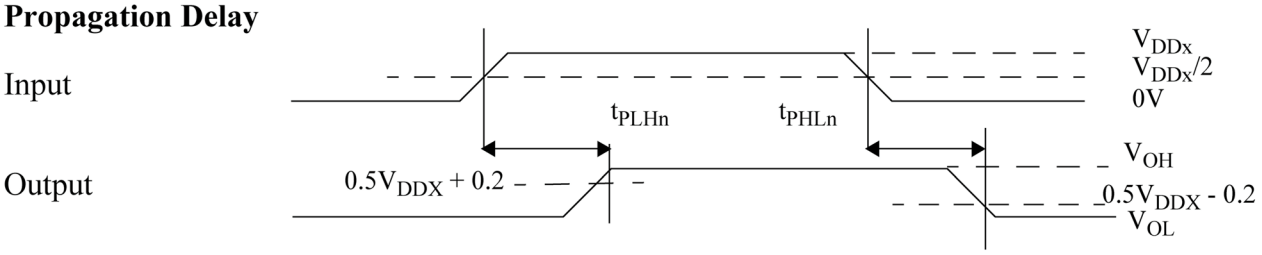
Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

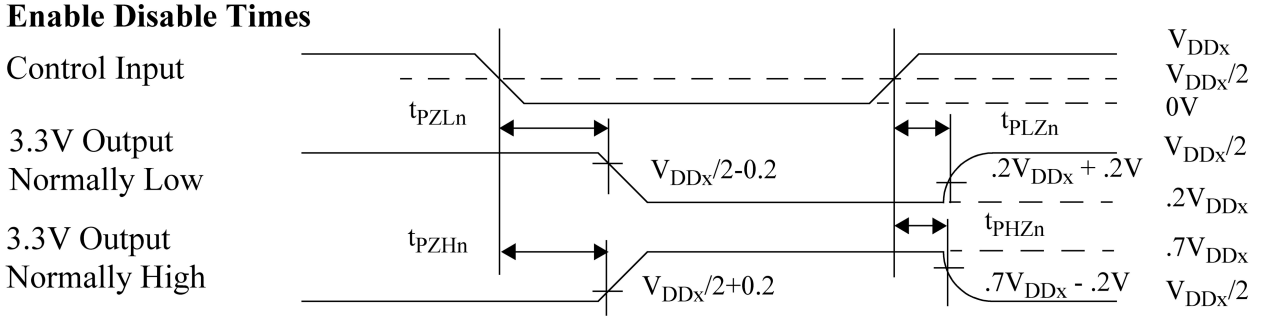
1) All specifications valid for radiation dose ≤ 1E5 rad(Si) per MIL-STD-883, Method 1019.
2) These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
3) xDIR to bus times are guaranteed by design, but not tested. $x\overline{OE}$ to bus times are tested.
4) Output skew is defined as a comparison of any two output transitions of the same type at the same temperature and voltage for the same port within the same byte: 1A1 through 1A8 are compared high-to-low versus high-to-low and low to high versus low-to-high; similarly 1B1 through 1B8 are compared, 2A1 through 2A8 are compared, and 2B1 through 2B8 are compared.
5) Differential output skew is defined as a comparison of any two output transitions of opposite types on the same type at the same temperature and voltage for the same port within the same byte: 1A1 through 1A8 are compared high-to-low versus low-to-high; similarly, 1B1 through 1B8 are compared, 2A1 through 2A8 are compared, and 2B1 through 2B8 are compared.
6) Guaranteed by characterization, but not tested.

UT54ACS164646S

Propagation Delay



Enable Disable Times



AC Timing Waveforms for 3-Volt only operation
(e.g. V_{DDA} = V_{DDB} = 3.3V +/- 0.3V)

AC Electrical Characteristics (Clock Input Timing Relationships)

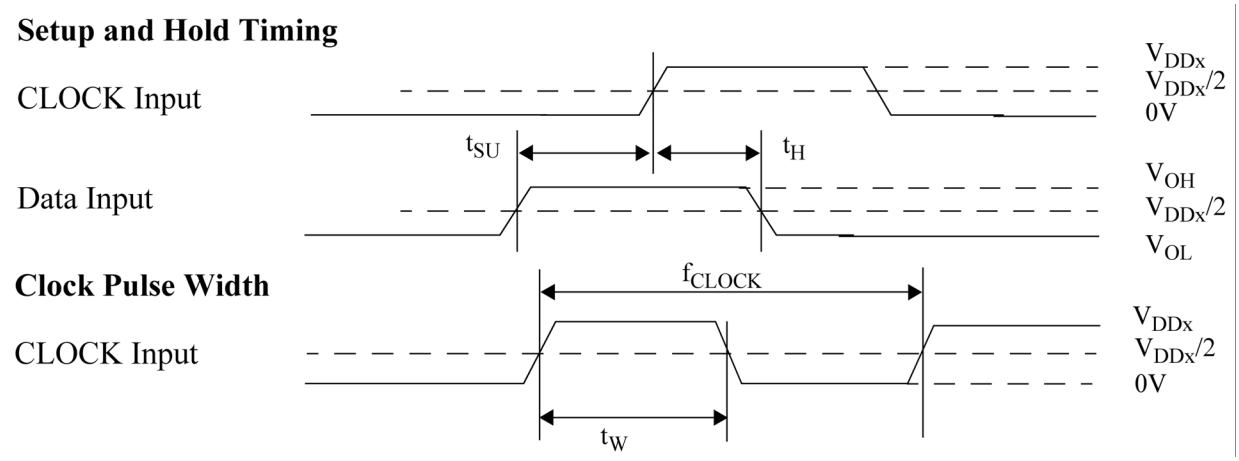
Symbol	Parameter		VDDA	VDDB	MIN	MAX	Unit
f_{CLOCK} [1]	Clock Frequency		4.5 3.0 3.0	4.5 4.5 3.0		100 90 80	MHz
t_P [1]	Clock Period		4.5 3.0 3.0	4.5 4.5 3.0	10 11.1 12.5		ns
t_W [1]	Pulse duration. CLKAB or CLKBA high or low		4.5 3.0 3.0	4.5 4.5 3.0	3.5 5 5		ns
t_{SU}	Setup time. A before CLKAB rising edge or B before CLKBA rising edge	Data High	4.5 3.0 3.0	4.5 4.5 3.0	2 3 3		ns
		Data Low	4.5 3.0 3.0	4.5 4.5 3.0	1 2 2		
t_H	Hold time. Bus A after CLKAB rising edge or Bus B after CLKBA rising edge		4.5 3.0 3.0	4.5 4.5 3.0	1.5 1.5 1.5		ns

Note:

1) Guaranteed by functional test.

UT54ACS164646S

Setup and Hold Timing



Clock Pulse Width

AC Electrical Characteristics (Input Rise and Fall Requirements)

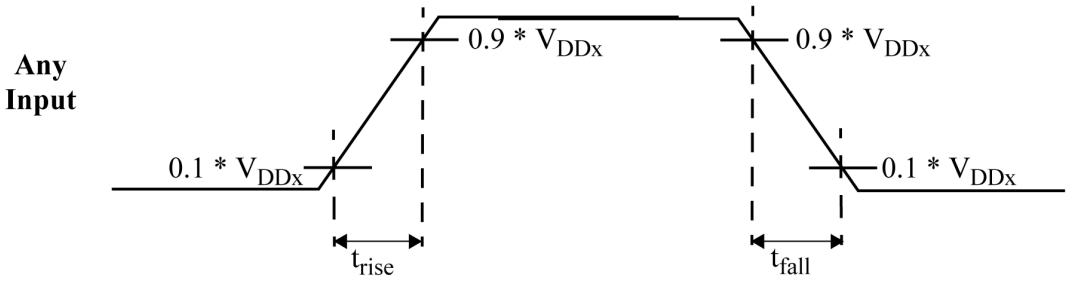
(All Power Supply Ranges, -55°C < T_C < +125°C)

Symbol	Parameter	Minimum	Maximum	Unit
t_{rise} [1]	Input rise time	--	100	ms
t_{fall} [1]	Input fall time	--	100	ms

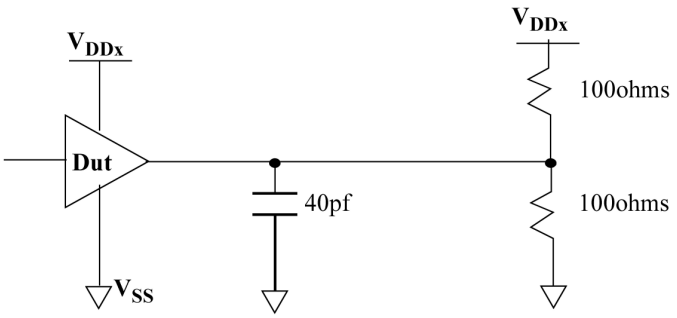
Note:

1) The input rise and fall parameter is guaranteed by characterization and is not tested.

Input Rise and Fall Timing:



AC Test Load or Equivalent



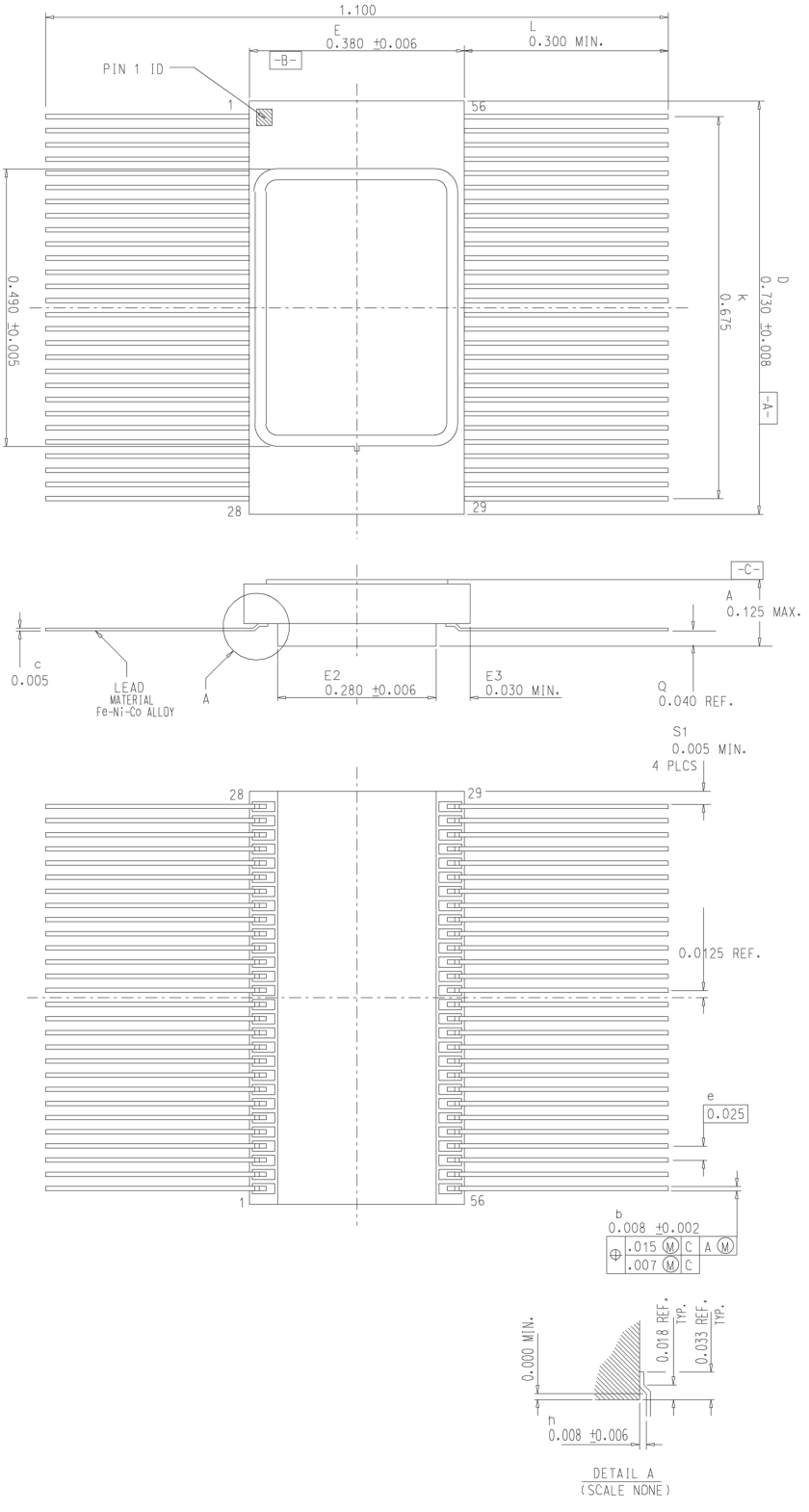
Note:

1) Equivalent test circuit means that DUT performance will be correlated and remain guaranteed to the applicable test circuit, above, whenever a test platform change necessitates a deviation from the applicable test circuit.

Schmitt CMOS 16-bit Bidirectional MultiPurpose Registered Transceiver

UT54ACS164646S

Package



Schmitt CMOS 16-bit Bidirectional MultiPurpose Registered Transceiver

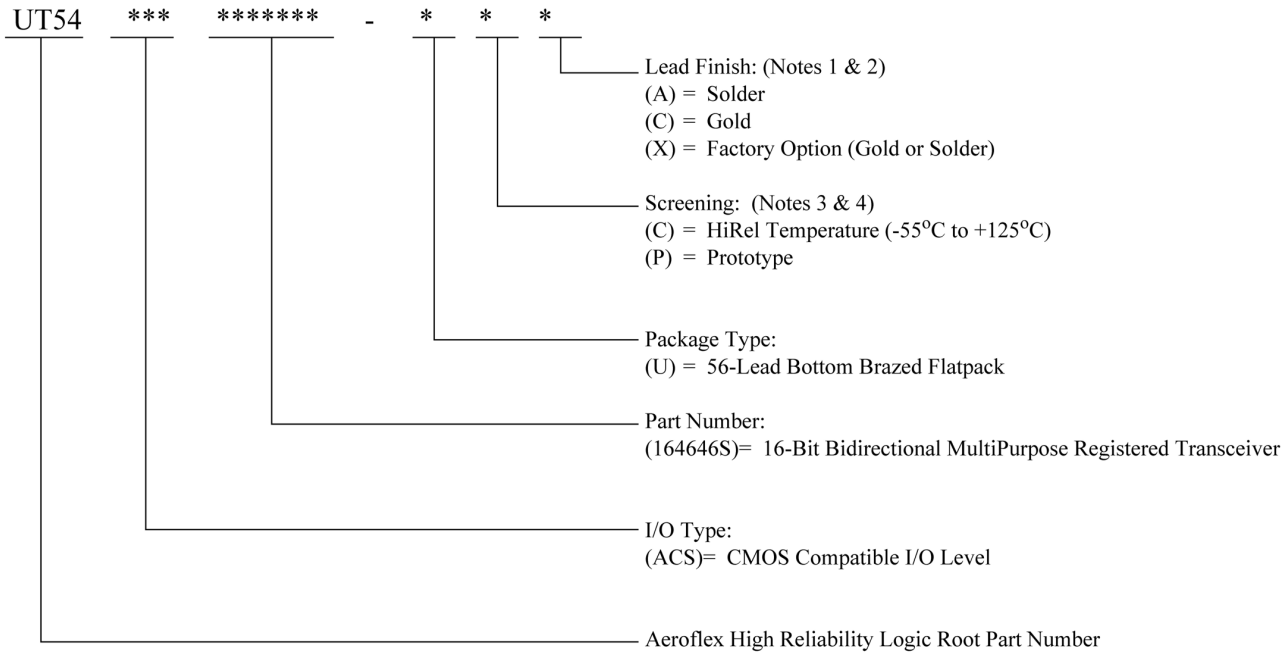
UT54ACS164646S

Notes:

1) All exposed metalized areas must be gold plated 100 over electroplated nickel underplating 100 microinches thick per MIL-PRF-38535.
2) Lead finish is in accordance with MIL-PRF-38535.
3) Seal ring is electrically connected to VSS.
4) Ceramic is dark alumina.
5) Letter designations are to cross-referenced to MIL-STD-1835.
6) Lead true position tolerance and coplanarity are not measured.

Ordering Information

UT54ACS164646S



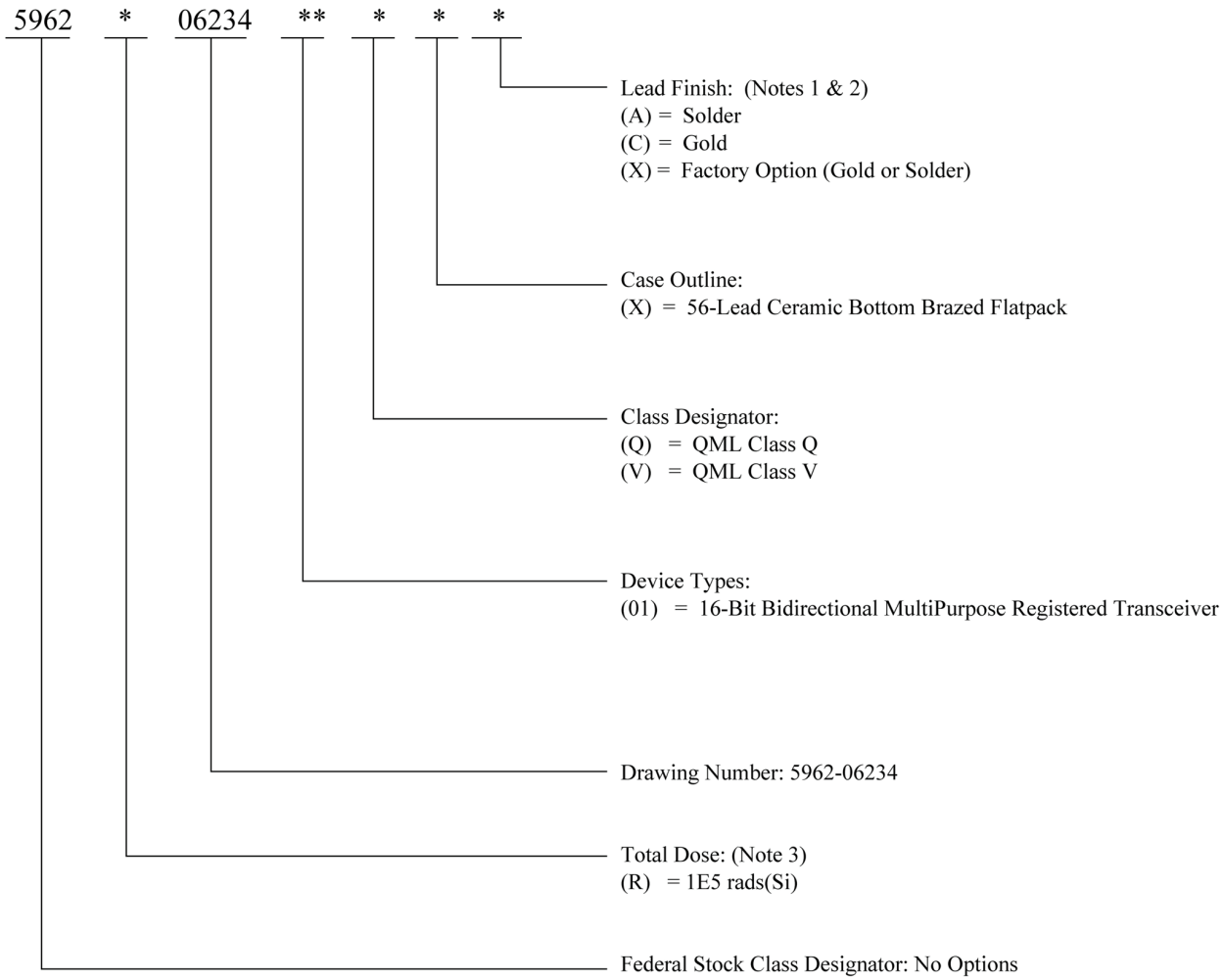
Notes:

1) Lead finish (A, C, or X) must be specified.
2) If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3) Prototype flow per CAES Colorado Springs Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4) HiRel Temperature Range flow per CAES Colorado Springs Manufacturing Flows Document. Devices are tested at -55°C, 25°C and 125°C. Radiation neither tested nor guaranteed.

Schmitt CMOS 16-bit Bidirectional MultiPurpose Registered Transceiver

UT54ACS164646S

UT54ACS164646S: SMD



Notes:

1) Lead finish (A, C, or X) must be specified.
2) If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3) Total dose radiation must be specified when ordering. QML-Q and QML-V are not available without radiation hardening.

DATASHEET

RELEASED 5/17/12

Schmitt CMOS 16-bit Bidirectional MultiPurpose Registered Transceiver

UT54ACS164646S

Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

The following United States (U.S.) Department of Commerce statement shall be applicable if these commodities, technology, or software are exported from the U.S.: These commodities, technology, or software were exported from the United States in accordance with the Export Administration Regulations. Diversion contrary to U.S. law is prohibited.