FRONTGRADE

PRELIM DATASHEET

UT24CP1008

CertusPro®-NX-RT Family

12/5/2023

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ADC	Analog to Digital Convertor
AES	Advanced Encryption Standard
ALU	Arithmetic Logic Unit
BGA	Ball Grid Array
CDR	Clock and Data Recovery
CMUX	Center MUX
CRC	Cycle Redundancy Code
CSI	Camera Serial Interface
DCC	Dynamic Clock Control
DCS	Dynamic Clock Select
DDR	Double Data Rate
DLL	Delay Locked Loop
DQS	DQ Strobe
DRAM	Dynamic RAM
DSI	Display Serial Interface
DSP	Digital Signal Processing
EBR	Embedded Block RAM
ECC	Error Correction Coding
ECDSA	Elliptic Curve Digital Signature Algorithm
ECLK	Edge Clock
ECLKDIV	Edge Clock Divider
eDP/DP	Embedded DisplayPort/DisplayPort
FD-SOI	Fully Depleted Silicon on Insulator
FFT	Fast Fourier Transform
FIFO	First In First Out
FIR	Finite Impulse Response
GPIO	General Purpose I/O
GPLL	Global Phase Locked Loop
HFOSC	High Frequency Oscillator
HMAC	Hash-based Message Authentication Code
HP	High Performance
HS	High Speed
I^2C	Inter-Integrated Circuit
I3C	Improved Inter-Integrated Circuit
IP	Intellectual Property
LC	Logic Cell
LOL	Loss Of Lock
LFOSC	Low Frequency Oscillator

Acronym	Definition
LMMI	Lattice Memory Mapped Interface
LP	Low Power
LSB	Least Significant Bit
LPDDR	Low Power Double Data Rate
LRAM	Large Random Access Memory
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTL	Low Voltage Transistor-Transistor Logic
LUT	Look Up Table
MAC	Multiply and Accumulate
MLVDS	Multipoint Low-Voltage Differential Signaling
MPCS	Multi-Protocol PCS
MSPS	Million Samples Per Second
MUX	Multiplexer
OSC	Oscillator
PCI	Peripheral Component Interconnect
PCS	Physical Coding Sublayer
PCLK	Primary Clock
PCLKDIV	Primary Clock Divider
PDPR	Pseudo Dual Port RAM
PFU	Programmable Functional Unit
PIC	Programmable I/O Cell
PLL	Phase Locked Loop
POR	Power On Reset
PTAT	Proportional To Absolute Temperature
RAM	Random-access Memory
RLAT	Radiation Lot Acceptance Testing
ROM	Read Only Memory
RST	Reset
SAR	Successive Approximation Register
SCI	SerDes Client Interface
SCL	Serial Clock
SDA	Serial Data
SEC	Soft Error Correction
SED	Soft Error Detection
SER	Soft Error Rate
SEU	Single Event Upset
SGMII	Serial Gigabit Media Independent Interface
SHA	Secure Hash Algorithm
SLVS	Scalable Low-Voltage Signaling

Acronym	Definition
SLVS-EC	Scalable Low-Voltage Signaling Embedded Clock
SPI	Serial Peripheral Interface
SSPI	Slave Serial Peripheral Interface
SPR	Single Port RAM
SRAM	Static Random-Access Memory
TAP	Test Access Port
TDM	Time Division Multiplexing
Tx	Transmitter
TLP	Transaction Layer Packet
UCFG	User Configuration Space Register Interface
Rx	Receiver
WR	Wide Range

1. Description

The CertusPro™-NX-RT family of low-power general purpose FPGAs featuring 6.25Gbps SerDes, LPDDR4 memory interface support and 100k logic cells can be used in a wide range of applications across multiple markets. It is built on the Lattice Nexus FPGA platform, using low-power 28 nm FD-SOI technology. It combines the extreme flexibility of an FPGA with the low power and high reliability (due to extremely low SER) of FD-SOI technology, and offers small footprint package option as well as 0.8 ball-pitch package option.

CertusPro-NX-RT supports a variety of interfaces including PCI Express® (Gen1, Gen2, and Gen3), Ethernet (up to 6.25Gbps), SLVS-EC, CoaXPress, eDP/DP, LVDS, Generic 8b10b, LVCMOS (0.9–3.3 V), and more.

Processing features of CertusPro-NX-RT include 100k logic cells, 156 multipliers (18 × 18), 7.3 Mb of embedded memory (consisting of EBR and LRAM blocks), distributed memory and DRAM interfaces (supporting DDR3, DDR3L, LPDDR2, and LPDDR4 up to 1066 Mbps × 64bit data width).

CertusPro-NX-RT FPGAs support fast configuration of the reconfigurable SRAM-based logic fabric, ultra-fast configuration of its programmable sysI/O™ and the TransFR™ field upgrade feature. Design security features, such as AES-256 encryption and ECDSA authentication, are also supported. In addition to the high reliability inherent to FD-SOI technology (due to its extremely low SER), active reliability features such as built-in frame-based Soft Error Detection (SED)/Soft Error Correction (SEC) (for SRAM-based logic fabric), and ECC (for EBR and LRAM) are also supported in CertusPro-NX-RT device. Dual 1 MSPS 12-bit Analog to Digital Convertors (ADCs) are available on-chip for system monitoring functions.

The Lattice Radiant™ design software allows large complex user designs to be efficiently implemented in CertusPro-NX-RT FPGA family. Synthesis library support for CertusPro-NX-RT devices is available for popular logic synthesis tools. Radiant tools use the synthesis tool output along with constraints from its floor planning tools to place and route the user design in CertusPro-NX-RT device. The tools extract timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered Intellectual Property (IP) modules for CertusPro-NX-RT family. By using these configurable soft IP cores as standardized blocks, you are free to concentrate on the unique aspects of your design, increasing your productivity.

1.1 Features

- Programmable architecture
  - 100k logic cells
  - 156 multipliers (18 × 18) in sysDSP™ blocks
  - 7.3 Mb of embedded memory (including EBR and LRAM)
  - 299 programmable sysI/O (High Performance and Wide Range I/O)
- Programmable sysI/O designed to support wide variety of interfaces
  - High Performance (HP) I/O supported on bottom I/O banks
    - Supports up to 1.8 V VCCIO
    - Mixed voltage support (1.0 V, 1.2 V, 1.5 V, and 1.8 V)
    - High-speed differential up to 1.5 Gbps
    - Supports LVDS, Soft D-PHY Transmitter (Tx)/Receiver (Rx), LVDS 7:1 Tx/Rx, SLVS Tx/Rx, subLVDS Rx
    - Supports SGMII (Gb Ethernet):
    - Two channels (Tx/Rx) at 1.25 Gbps
    - Dedicated DDR3/DDR3L and LPDDR2/LPDDR3/LPDDR4 memory support with DQS logic, up to 1066 Mbps data rate and ×64bit data width
  - Wide Range (WR) I/O supported on left, right, and top I/O Banks
    - Supports up to 3.3 V VCCIO
    - Mixed voltage support: 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V
    - Programmable slew rate: slow, medium, and fast
    - Controlled impedance mode
    - Emulated LVDS support
    - Hot Socketing Support
  - Embedded SerDes
    - From 625 Mbps up to 6.25 Gbps per channel, with up to 8 channels
      - Multiple Protocol PCS support
      - PCIe hard IP supports:
      - Gen1, Gen2, and Gen3
      - Endpoint and Root complex
      - Multi-function up to four functions
      - Up to four lanes

  - Ethernet
    - SGMII at 1.25 Gbps and 2.5 Gbps
    - XAUI at 3.125 Gbps per lane
  - SLVS-EC at 1.25 Gbps, 2.5 Gbps and 5 Gbps
  - DP/eDP at 1.62 Gbps (RBR), 2.7 Gbps (HBR), and 5.4 Gbps (HBR2)
  - CoaXPress at 1.25 Gbps, 2.5 Gbps, 3.125 Gbps, 5 Gbps and 6.25 Gbps
  - Generic 8b10b at multiple data rates
  - SerDes-only mode allows direct 8-bit or 10-bit interface to FPGA logic
- Power modes – Low Power mode and High Performance modes
  - User selectable
  - Low Power mode for power saving and/or thermal challenges
  - High Performance mode for faster processing
- Small footprint package options
  - 19 mm × 19 mm package size
- Two channels of Clock Data Recovery (CDR) up to 1.25 Gbps to support SGMII on HP I/O
  - CDR for Rx
  - 8b/10b decoding
  - Independent Loss of Lock (LOL) detector for each CDR block
- sysCLOCK™ analog PLLs
  - Three in 50k LC, and four in 100k LC
  - Six outputs per PLL
  - Fractional N
  - Programmable and dynamic phase control
  - Support spread spectrum clocking
- sysDSP enhanced DSP blocks
  - Hardened pre-adder
  - Dynamic shift for AI/ML support
  - Four 18 × 18, eight 9 × 9, two 18 × 36, or 36 × 36 multipliers
  - Advanced 18 × 36, two 18 × 18, or four 8 × 8 MAC per sysDSP blocks
- Flexible memory resources
  - Up to 3.7 Mb sysMEM™ Embedded Block RAM (EBR) available

- Programmable width
- Error Correction Coding (ECC)*
- First In First Out (FIFO)
- 639 kbits distributed RAM
  - Large RAM Blocks
    - 0.5 Mbits per block
    - Up to seven (3.5 Mbit total) per device

- Internal bus interface support
  - APB control bus
  - AHB-Lite for data bus
  - AXI4-streaming
- Configuration – Fast, Secure
  - SPI – ×1, ×2, ×4 up to 150 MHz
    - Master and Slave SPI support
  - JTAG
  - I^2C and I3C
  - Ultrafast I/O configuration for instant-on support (using Early I/O Release feature)
  - Less than 30 ms full device configuration for LFCPNX-100 device
- Cryptographic engine
  - Bitstream encryption – using AES-256
  - Bitstream authentication – using ECDSA
  - Hashing algorithms – SHA, HMAC
  - True Random Number Generator
    - AES 128/256 Encryption

- Single Event Upset (SEU) Mitigation Support
    - Extremely low Soft Error Rate (SER) due to FD-SOI technology
    - Soft Error Detect – Embedded hard macro
    - Soft Error Correction – Transparent to user design operation
    - Soft Error Injection – Emulate SEU event to debug system error handling
- Dual ADC – 1 MSPS, 12-bit Successive Approximation Register (SAR), with Simultaneous Sampling*
    - Three Continuous-time Comparators
- System-level support
    - IEEE 1149.1 and IEEE 1532 compliant
    - Reveal Logic Analyzer
    - On-chip oscillator for device initialization and general use
    - 1.0V core power supply

*Available in –8 speed grade.

Table 1.1 CertusPro-NX-RT Family Selection Guide

Device	LFCPNX-100
Logic Cells1	96k
Embedded Memory (EBR) Blocks (18 kb)	208
Embedded Memory (EBR) Bits (kb)	3,744
Distributed RAM Bits (kb)	639
Large Memory (LRAM) Blocks (512 kb)	7
Large Memory (LRAM) Bits (kb)	3,584
18 X 18 Multipliers	156
ADC Blocks3	2
450 MHz High Frequency Oscillator	1
32 kHz Low Power Oscillator	1
GPLL	4
PCIe Gen3 hard IP	1
SerDes(Quad/Channels)	2/8
Packages (Size, Ball Pitch)	SerDes Channels/I/O (Wide Range (WR) GPIO (Top/Left/Right Banks) + High Performance (HP) GPIO (Bottom Banks) + ADC dedicated inputs)
BBG484 (19 mm × 19 mm, 0.8 mm)	8/305 (167 + 132 + 6)

Notes:

1. Logic Cells = LUTs × 1.2 effectiveness.

2. Architecture

2.1 Overview

Each CertusPro-NX-RT device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM Embedded Block RAM (EBR) and rows of sysDSP Digital Signal Processing blocks, as shown in Figure 2.1. For example, the LFCPNX-100 devices have three rows of DSP blocks and contain four rows of sysMEM EBR blocks. In addition, LFCPNX-100 devices include seven large SRAM blocks. The sysMEM EBR blocks are large, dedicated 18 kbits fast memory blocks and have built-in ECC and FIFO support. Each sysMEM block can be configured to a single, pseudo dual or true dual port memory in a variety of depths and widths as RAM or ROM. Each DSP block supports a variety of multiplier and adder configurations with one 108-bit or two 54-bit accumulators supported, which are the building blocks for complex signal processing capabilities.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the CertusPro-NX-RT devices are arranged in eight banks allowing the implementation of a wide variety of I/O standards. The Wide Range (WR) I/O banks that are located on the top, left and right sides of the device provide flexible ranges of general purpose I/O configurations up to 3.3 V VCCIO. The banks located on the bottom side of the device are dedicated to High Performance (HP) interfaces such as LVDS, MIPI, DDR3, LPDDR2, LPDDR3, and LPDDR4 supporting up to 1.8 V VCCIO.

The Programmable Functional Unit (PFU) contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFU block is optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. The registers in the PFU and sysI/O blocks in CertusPro-NX-RT devices can be configured to be SET or RESET. After power up and device configuration, it enters into user mode with these registers SET/RESET according to the user design, allowing the device to power up in a known state for predictable system function.

The CertusPro-NX-RT FPGAs feature up to eight embedded 6.25 Gbps SerDes channels. Each SerDes channel contains independent 8b/10b encoding/decoding, polarity adjust and elastic buffer logic. Each group of four SerDes channels, along with its Physical Coding Sublayer (PCS) block, creates a Quad. The functionality of the SerDes/PCS Quads can be controlled by SRAM cell settings during device configuration or by registers that are addressable during device operation. The registers in every Quad can be programmed via the Lattice Memory Mapped Interface (LMMI). These Quads (up to two) are located at the top of the device. The FPGA also includes one hard PCIe link layer IP block which supports PCIe Gen1, Gen2, and Gen3.

In addition, CertusPro-NX-RT devices provide various system level functional and interface hard IP such as I^2C, SGMII/CDR, and ADC blocks. CertusPro-NX-RT devices also provide security features to help protect user designs and deliver more robust reliability by offering enhanced frame-based SED/SEC functions.

Other blocks provided include PLLs, DLLs, and configuration functions. The PLL and DLL blocks are located at the corners of each device. CertusPro-NX-RT devices also include LMMI, which is a Lattice standard interface for simple read and write operations to control internal IP.

Every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detection (SED) capability. The CertusPro-NX-RT devices use 1.0 V as their core voltage.

Figure 2.1 Simplified Block Diagram, LFCPNX-100 Device (Top Level)

2.2 PFU Blocks

The core of the CertusPro-NX-RT device consists of PFU blocks. Each PFU block consists of four interconnected slices numbered 0–3, as shown in Figure 2.2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing.

The PFU block can be used to perform Logic, Arithmetic, Distributed RAM or ROM functions. Table 2.1 shows the functions each slice can perform in either Distributed SRAM or non-Distributed SRAM modes.

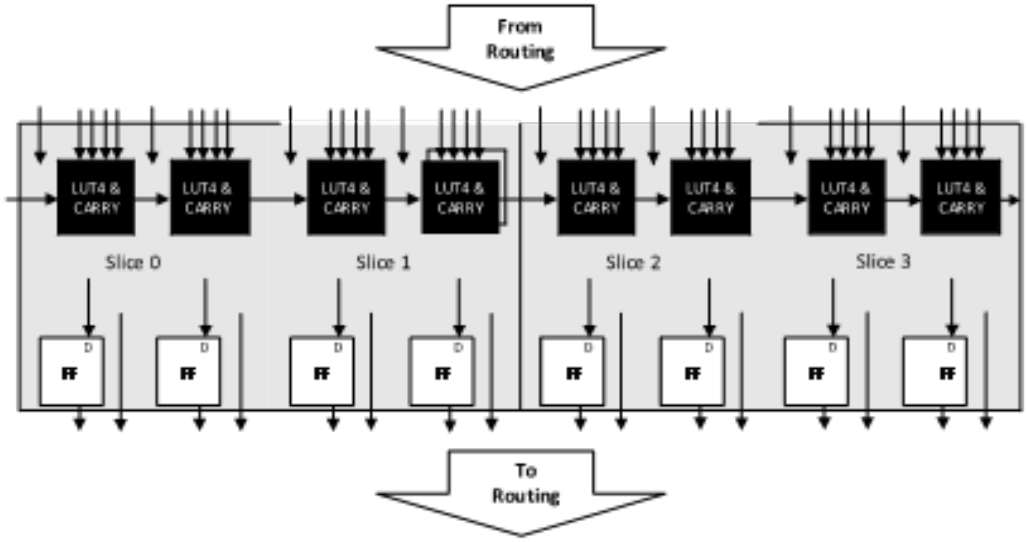


Figure 2.2 PFU Diagram

2.2.1 Slice

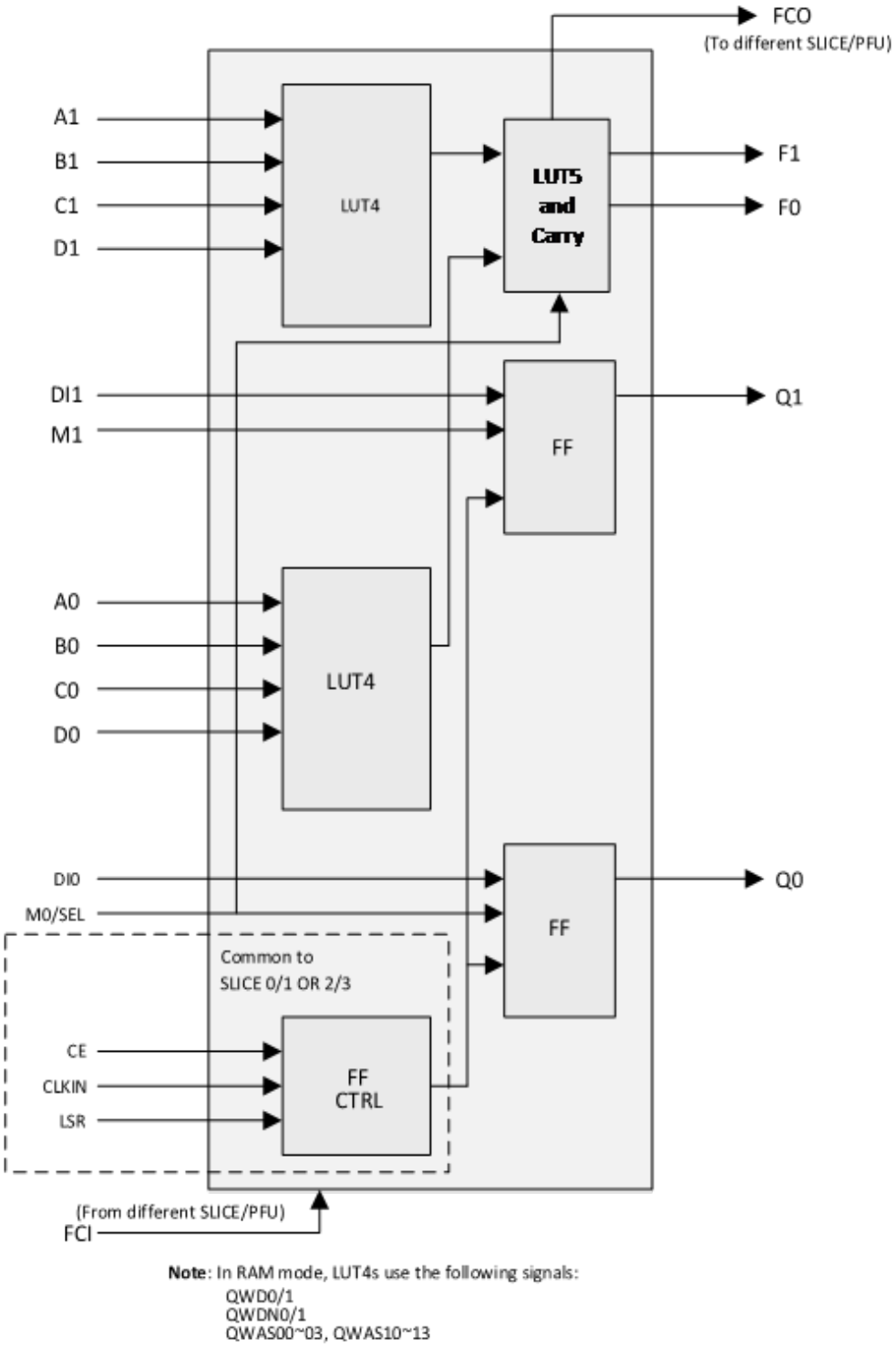
Each slice contains two LUT4s feeding two registers. In Distributed SRAM mode, Slice 0 and Slice 1 are configured as distributed memory and Slice 2 is not available as it is used to support Slice 0 and Slice 1, while Slice 3 is available as Logic or ROM. Table 2.1shows the capability of the slices along with the operation modes they can enable. In addition, each Slice contains logic that allows the LUTs to be combined to perform a LUT5 function. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select, and wider RAM/ROM functions.

Table 2.1 Resources and Modes Available per Slice

Slice	PFU (Used as Distributed SRAM)		PFU (Not used as Distributed SRAM)	
	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Figure 2.3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive or negative edge clocking.

Each slice has 17 input signals: 16 signals from routing and one from the carry-chain (from the adjacent slice or PFU). Three of them are used for FF control and shared between two slices (0/1 or 2/3). There are five outputs: four to routing and one to carry-chain (to the adjacent PFU). Signals associated with all the slices can be found in Figure 2.3 and Table 2.2. Figure 2.4 shows the slice signals that support a LUT5 or two LUT4 functions. F0 can be configured to have a LUT4 or LUT5 output, while F1 can be configured as a LUT4 output only.



Note: In RAM mode, LUT4s use the following signals:
QWD0/1
QWDN0/1
QWAS00~03, QWAS10~13

Figure 2.3 Slice Diagram

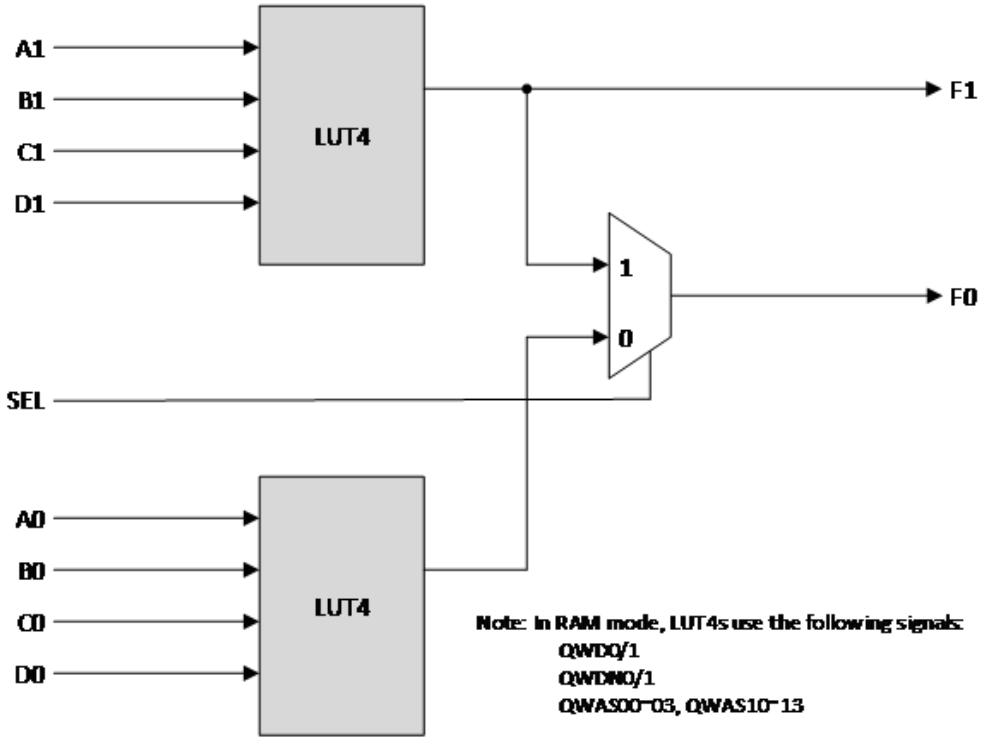


Figure 2.4 Slice Configuration for LUT4 and LUT5

Table 2.2 Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4.
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4.
Input	Data signal	M0, M1	Direct input to FF from fabric.
Input	Control signal	SEL	LUT5 mux control input.
Input	Data signal	DI0, DI1	Inputs to FF from LUT4 F0/F1 outputs.
Input	Control signal	CE	Clock Enable.
Input	Control signal	LSR	Local Set/Reset.
Input	Control signal	CLKIN	System Clock.
Input	Inter-PFU signal	FCI	Fast Carry-in.
Output	Data signals	F0	LUT4/LUT5 output signal.
Output	Data signals	F1	LUT4 output signal.
Output	Data signals	Q0, Q1	Register outputs.
Output	Inter-PFU signal	FCO	Fast carry chain output.

Note: See Figure 2.3 for connection details.

2.2.2 Modes of Operation

Slices 0-2 have up to four potential modes of operation: Logic, Ripple, RAM, and ROM. Slice 3 is not needed for the RAM mode. It can be used in the Logic, Ripple, or ROM mode.

Logic Mode

In the Logic mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice.

Ripple Mode

The Ripple mode supports the efficient implementation of small arithmetic functions. In the Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear 2-bit using dynamic control
- Up/Down counter with preload (sync) 2-bit using dynamic control
- Comparator functions of A and B inputs 2-bit
    - A greater-than-or-equal-to B
    - A not-equal-to B
    - A less-than-or-equal-to B
- Up/Down counter with A greater-than-or-equal-to B comparator 2-bit using dynamic control
- Up/Down counter with A less-than-or-equal-to B comparator 2-bit using dynamic control
- Multiplier support Ai×Bj+1 + Ai+1×Bj in one logic cell with two logic cells per slice
- Serial divider 2-bit mantissa, shift 1 bit/cycle
- Serial multiplier 2-bit, shift 1 bit/cycle or 2 bit/cycle

The Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode), two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In the RAM mode, a 16 × 4-bit distributed single or pseudo dual port RAM can be constructed in one PFU using each LUT block in Slice 0 and Slice 1 as a 16 × 2-bit memory in each slice. Slice 2 is used to provide memory address and control signals. The CertusPro-NX-RT devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different sized memories. Where appropriate, the software constructs these using distributed memory primitives that represent the capabilities of the PFU. Table 2.3 lists the number of slices required to implement different distributed RAM primitives. For more information about using RAM in CertusPro-NX-RT devices, refer to Memory Usage Guide for Nexus Platform (FPGA-TN-02094).

Table 2.3 Number of Slices Required to Implement Distributed RAM

	SPR 16 × 4	PDPR 16 × 4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

The ROM mode uses the LUT logic; hence, Slice 0 through Slice 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, refer to Memory Usage Guide for Nexus Platform (FPGA-TN-02094).

2.3 Routing

There are many resources provided in the CertusPro-NX-RT devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The CertusPro-NX-RT family has an enhanced routing architecture that produces a compact design. Lattice Radiant software tool takes the output of the synthesis tool and places and routes the design.

2.4 Clocking Structure

The CertusPro-NX-RT clocking structure consists of clock synthesis blocks (sysCLOCK PLLs), balanced clock tree networks (PCLK and ECLK) and efficient clock logic modules: Clock Dividers (PCLKDIV and ECLKDIV), Dynamic Clock Select (DCS), Dynamic Clock Control (DCC), and DDRDLLs. Each of these functions is described as follows.

2.4.1 Global PLL

The Global PLLs (GPLL) provide the ability to synthesize clock frequencies. The devices in the CertusPro-NX-RT family support three to four full-featured general purpose GPLLs.

The architecture of the GPLL is shown in Figure 2.5. A description of the GPLL functionality follows.

REFCLK is the reference frequency input to the PLL. The REFCLK source can come from external CLK inputs or from internal routing. The CLKI input feeds into the input Clock Divider block.

CLKFB is the feedback signal to the GPLL, which can come from a path internal to the PLL or from FPGA routing. The feedback divider is used to multiply the reference frequency and thus synthesize a higher or lower frequency clock output.

The PLL has six clock outputs, CLKOP, CLKOS, CLKOS2, CLKOS3, CLKOS4, and CLKOS5. Each output has its own output divider, thus allowing the GPLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. Each GPLL output can be used to drive the primary clock. Each bottom side GPLL output can be used to drive the edge clock networks.

The setup and hold times of the device can be improved by programming a phase shift into the output clocks which advances or delays the output clock with reference to the un-shifted output clock. This phase shift can be either

programmed during the configuration or can be adjusted dynamically using the DIRSEL, DIR, DYNROTATE, and LOADREG ports.

The LOCK signal is asserted when the GPLL determines it has achieved lock and de-asserted if a loss of lock is detected. The LOCK signal is asynchronous to the PLL clock outputs.

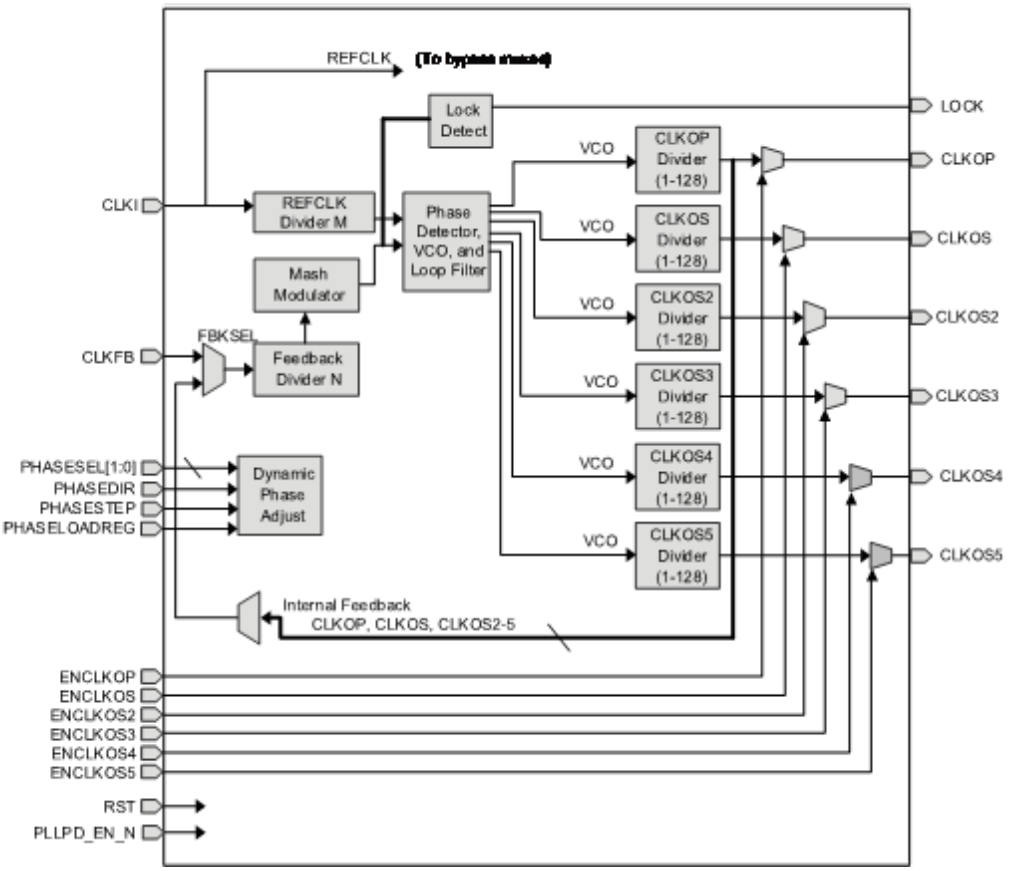


Figure 2.5 General Purpose PLL Diagram

For more details on the PLL, refer to the sysCLOCK PLL Design and Usage Guide for Nexus Platform (FPGA-TN-02095).

2.4.2 Clock Distribution Network

There are two main clock distribution networks for any member of the CertusPro-NX-RT product family, namely Primary Clock (PCLK) and Edge Clock (ECLK). These clock networks can be driven from many different sources, such as Clock Pins, PLL outputs, DLLDEL outputs, Clock Divider outputs, SerDes/PCS clocks, and user logic. There are Clock Divider blocks, ECLKDIV and PCLKDIV, to provide a slower clock from these clock sources.

CertusPro-NX-RT family supports glitchless Dynamic Clock Control (DCC) for the PCLK Clock to save dynamic power. There are also Dynamic Clock Selection logic to allow a glitchless selection between two clocks for the PCLK network (DCS).

An overview of the Clocking network for the CertusPro-NX-RT device is shown in Figure 2.6. The Upper Right PLL in Figure 2.6 is only for LFCPNX-100 Logic Cell devices.

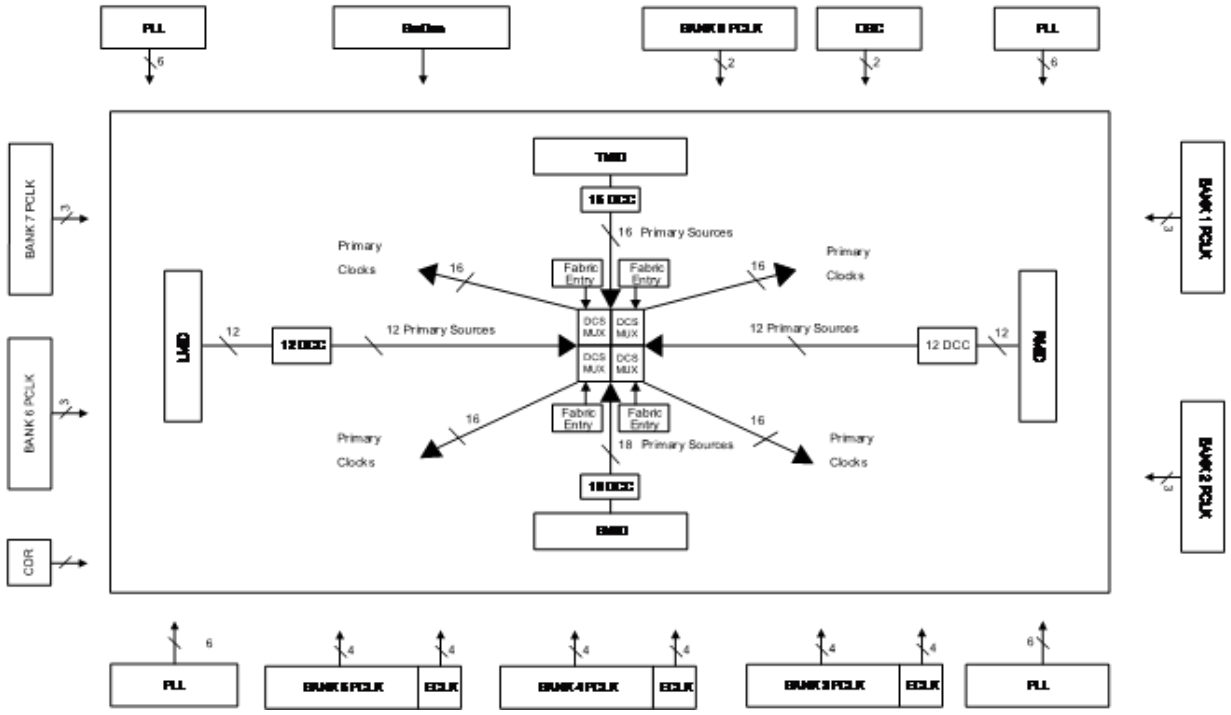


Figure 2.6 Clocking Network

2.4.3 Primary Clocks

The CertusPro-NX-RT device family provides low-skew, high fan-out clock distribution to all synchronous elements in the FPGA fabric through the Primary Clock Network. The CertusPro-NX-RT PCLK clock network is a balanced clock structure which is designed to minimize the clock skew across all destinations in the FPGA core.

The primary clock network is divided into four clock domains. Each of these domains has 16 clocks that can be distributed to the fabric in the domain.

The Lattice Radiant software can automatically route each clock to one of the domains up to a maximum of 16 clocks per domain. You can change how the clocks are routed by specifying a preference in the Lattice Radiant software to locate the clock to a specific domain. The CertusPro-NX-RT device provides you with a maximum of 64 unique clock input sources that can be routed to the primary Clock network.

Primary clock sources are:

- Dedicated clock input pins
- PLL outputs
- PCLKDIV, ECLKDIV outputs
- Internal FPGA fabric entries (with minimum general routing)
- SGMII-CDR, SerDes/PCS clocks
- OSC clock

These sources routed to each of the four clock switches are called Mid Mux. They are LMID, RMID, TMID, and BMID. The outputs of the Mid MUX are routed to the center of the FPGA where additional clock switches (DCS MUX) are used to route the primary clock sources to primary clock distribution to the CertusPro-NX-RT fabric. These routing multiplexers are shown in Figure 2.6. Potentially there are 64 unique clock domains that can be used in the CertusPro-NX-RT device. For more information about the primary clock tree and connections, refer to sysCLOCK PLL Design and Usage Guide for Nexus Platform (FPGA-TN-02095).

2.4.4 Edge Clock

CertusPro-NX-RT FPGAs have a number of high-speed edge clocks that are intended for use with the PIO in the implementation of high-speed interfaces. There are four ECLK networks per bank I/O on the bottom side of the device. The Edge clock network is powered by a separate power domain (to reduce power noise injection from the core and reduce overall noise induced jitter) while controlled by the same logic that gates the FPGA core and PCLK domains for power management.

Each Edge Clock can be sourced from the following:

- Dedicated PIO Clock input pins (PCLK)
- DLLDEL output (PIO Clock delayed by 90°)
- Bottom PLL outputs (CLKOP, CLKOS, CLKOS2, CLKOS3, CLKOS4, and CLKOS5)
- Internal Nodes

Figure 2.7 illustrates various ECLK sources. Bank 3 is an ECLK source example. Bank 4 and Bank 5 are similar.

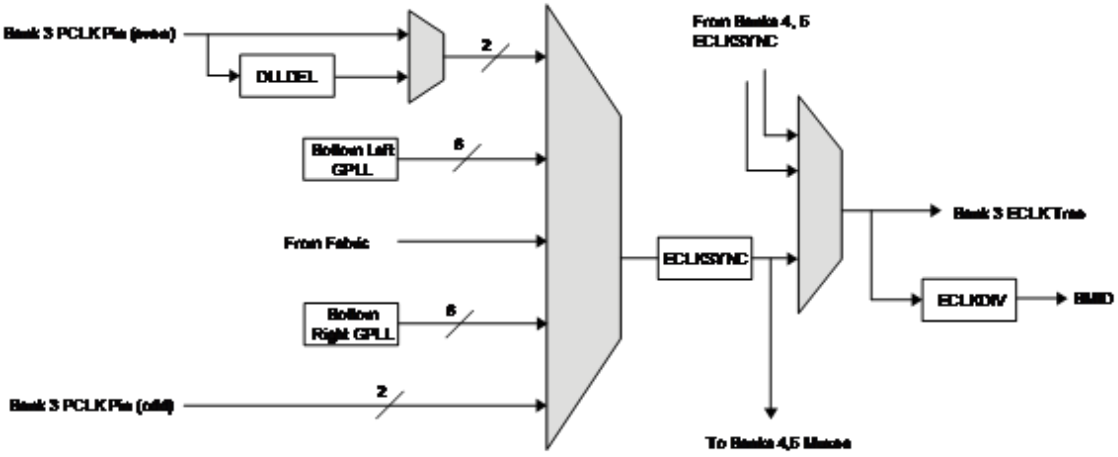


Figure 2.7 Edge Clock Sources per Bank

The edge clocks have low injection delay and low skew. They are typically used for DDR Memory or Generic DDR interfaces. For detailed information on Edge Clock connections, refer to sysCLOCK PLL Design and Usage Guide for Nexus Platform (FPGA-TN-02095).

2.4.5 Clock Dividers

CertusPro-NX-RT FPGAs have two distinct types of clock divider, Primary and Edge. There are two (2) Primary Clock Dividers (PCLKDIV) which are located in the DCS_CMUX block(s) and at the center of the device. There are 12 ECLKDIV dividers per device, which are located near the bottom high-speed I/O banks.

PCLKDIV supports ÷2, ÷4, ÷8, ÷16, ÷32, ÷64, ÷128, and ÷1 (bypass) operation. As shown in Figure 2.8, the PCLKDIV is fed from a DCSMUX within the DCS_CMUX block. The clock divider output drives one input of the Dynamic Clock Select (DCS) within the DCS_CMUX block. The Reset (RST) control signal is asynchronous and forces all outputs to low. The divider output starts at the next cycle after the reset is synchronously released.

ECLKDIV, as shown in Figure 2.7, is intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷3.5, ÷4, or ÷5 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The ECLKDIV can be fed from selected PLL outputs, external primary clock pins (with or without DLLDEL Delay) or from routing. The clock divider outputs feed into the Bottom Mid-mux (BMID). The Reset (RST) control signal is asynchronous and forces all outputs to low. The divider output starts at the next cycle after the reset is synchronously released.

For further information on clock dividers, refer to sysCLOCK PLL Design and Usage Guide for Nexus Platform (FPGA-TN-02095).

2.4.6 Clock Center Multiplexer Blocks

All clock sources are selected and combined for primary clock routing through the Dynamic Clock Selector Center Multiplexer logic (DCS_CMUX). There is one DCS_CMUX block per device. The DCS_CMUX block contains four DCSMUX blocks, two PCLKDIV, two DCS blocks, and four CMUX blocks. See Figure 2.8 for a representative DCS_CMUX block diagram.

The heart of the DCS_CMUX is the Center Multiplexer (CMUX) block. It can accept up to 64 feed clock sources, Mid-muxes RMID, LMID, TMID, BMID, and DCC to drive up to 16 primary clock trunk lines.

There are two Dynamic Clock Select (DCS) blocks in the DCS_CMUX. For each DCS block, there can be up to two clock inputs. Only one of the two clock inputs can be driven by the Primary Clock Divider (PCLKDIV). For more information about the DCS_CMUX, refer to sysCLOCK PLL Design and Usage Guide for Nexus Platform (FPGA-TN-02095).

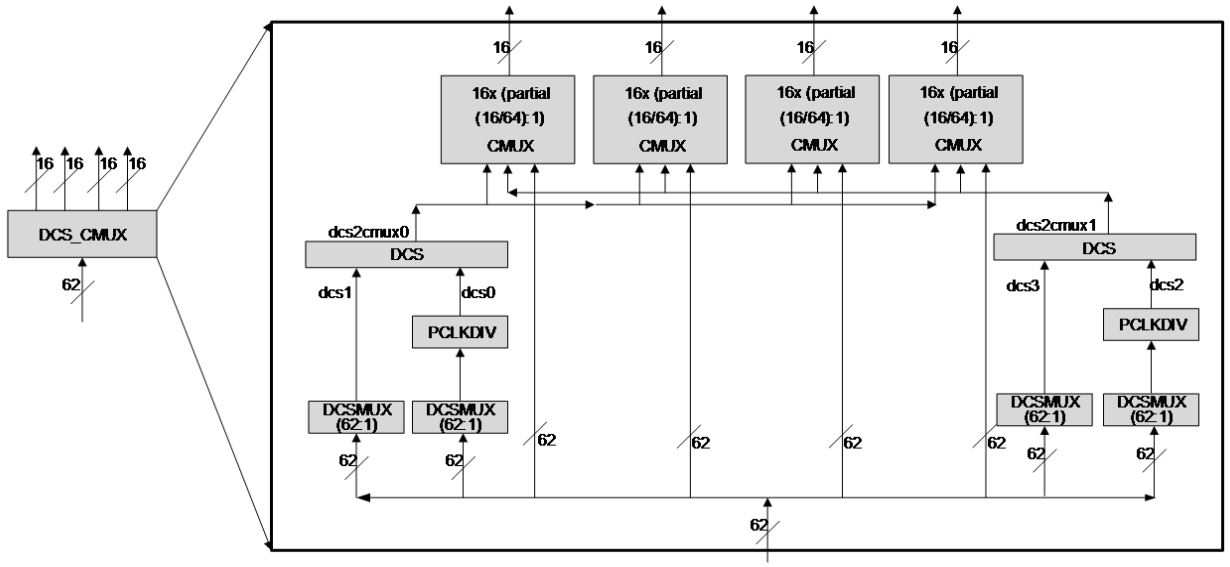


Figure 2.8 DCS_CMUX Block Diagram

2.4.7 Dynamic Clock Select

The Dynamic Clock Select (DCS) is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources. Depending on the operational modes, DCS switches between two independent input clock sources either with or without any glitches. This is achieved regardless of when the selected signal is toggled. Both input clocks must be running to achieve a functioning glitchless DCS output clock, but running clocks are not required when being used as a normal non-glitchless clock multiplexer.

Two DCS blocks per device feed all clock domains. The DCS blocks are located in the DCS_CMUX block. The inputs to the DCS blocks come from MIDMUX outputs and user logic clocks via DCC elements. The DCS elements are located at the center of the PLC array core. The output of the DCS is connected to the inputs of Primary Clock Center MUXs (CMUX).

Figure 2.9 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, refer to sysCLOCK PLL Design and Usage Guide for Nexus Platform (FPGA-TN-02095).

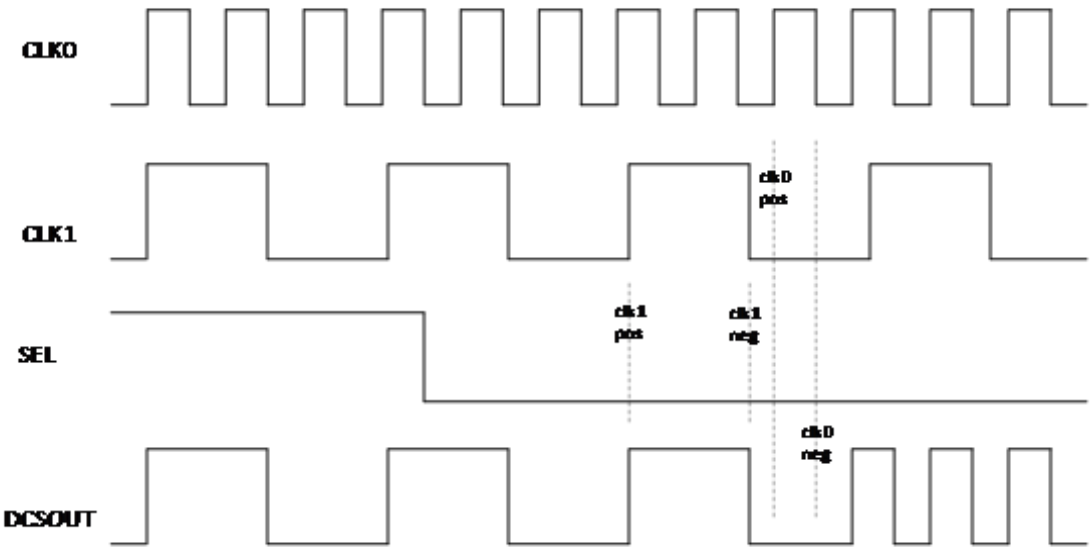


Figure 2.9 DCS Waveforms

2.4.8 Dynamic Clock Control

The Dynamic Clock Control (DCC), Domain Clock enable/disable feature allows internal logic control of the domain primary clock network. When a clock network is disabled, the clock signal is static and does not toggle. All the logic fed by that clock also does not toggle, reducing the overall power consumption of the device. The disable function is glitchless, and does not increase the clock latency to the primary clock network.

Four additional DCC elements control the clock inputs from the CertusPro-NX-RT domain logic to the Center MUX elements (DSC_CMUX).

This DCC controls the clock sources from the Primary CLOCK MIDMUX before they are fed to the Primary Center MUXs that drive the domain clock network. For more information about the DCC, refer to sysCLOCK PLL Design and Usage Guide for Nexus Platform (FPGA-TN-02095).

2.4.9 DDRDLL

CertusPro-NX-RT has two identical DDRDLL blocks located in the lower left and the lower right corners of the device. Each DDRDLL, the master DLL block, can generate a 9-bit phase shift value corresponding to a 90-degree phase shift of the reference clock input, and provide this value to every DQS block and DLLDEL slave delay element. The reference clock can be from either PLL or an input pin. The DQSBUF uses this value to control the delay of the DQS inputs from a DDR memory interface to achieve a 90-degree shift in order to clock DQ inputs at the center of the data eye.

The code is also sent to another slave DLL, DLLDEL, which takes a primary clock input and generates a 90-degree shift clock output to drive the clocking structure. This is useful to interface edge-aligned Generic DDR, where 90-degree clocking needs to be created. Not all primary clock inputs have associated DLLDEL control. Figure 2.10 shows DDRDLL connectivity to a DLLDEL block. The connectivity to DQSBUF blocks is similar.

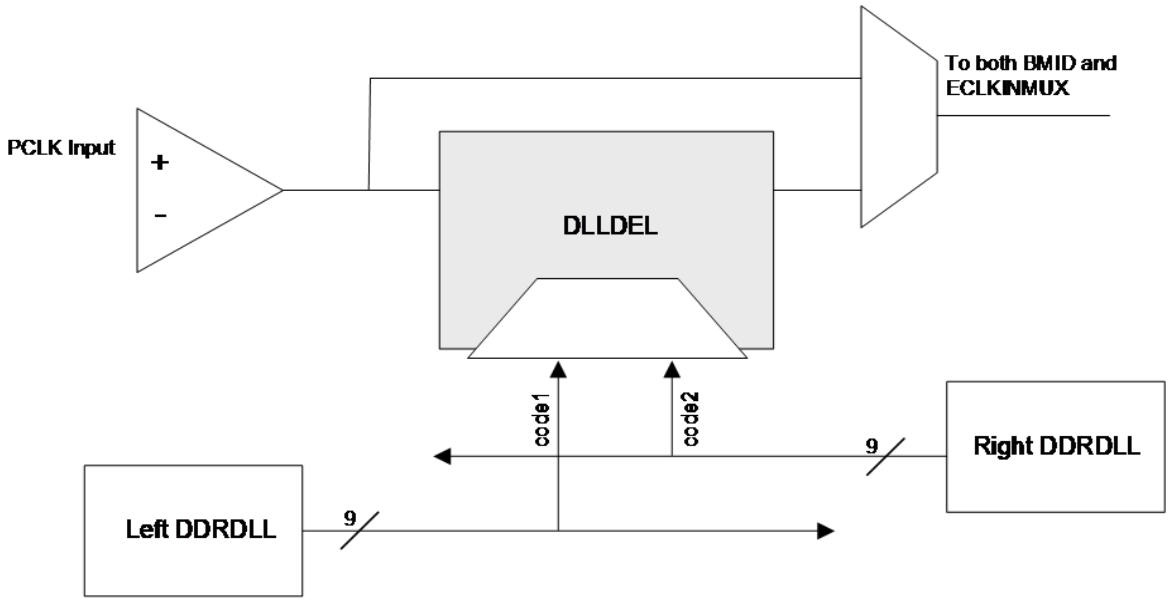


Figure 2.10 DLLDEL Function Diagram

Each DDRDLL can generate a delay value based on the reference clock frequency. The slave DLLs (DQSBUF and DLLDEL) use the value (code) to either create phase shifted inputs from the DDR memory or create a 90-degree shifted clock. Figure 2.11 shows the connections between the DDRDLL and the slave DLLs.

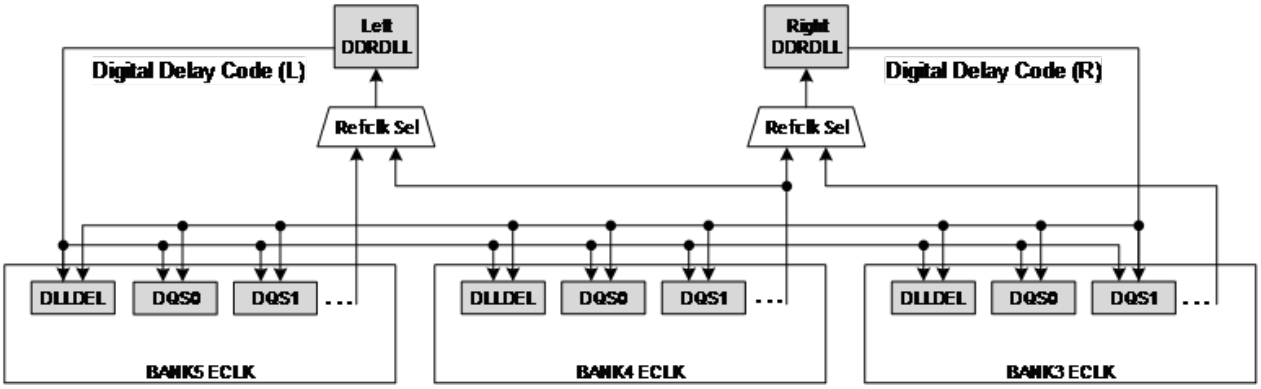


Figure 2.11 CertusPro-NX-RT DDRDLL Architecture

2.5 SGMII TX/RX

The CertusPro-NX-RT device utilizes different components/resources for the transmit and receive paths of SGMII. For the SGMII transmit path, Generic DDR I/O with X5 gearing are used. For more information, refer to GDDRX5_TX.ECLK.Aligned interface on the CertusPro-NX High-Speed I/O Interface (FPGA-TN-02244).

For the SGMII receive path, one of the two available hardened CDR (Clock and Data Recovery) Components can be used. There are three main blocks in each CDR: the CDR, deserializer, and FIFO. Each CDR features two loops. The first loop is locked to the reference clock. Once locked, the loop switches to the data path loop where the CDR tracks the data signals to

generate the correcting signals that needed to achieve and maintain phase lock with the data. The data is then passed through a deserializer which deserializes the data to 10-bit parallel data. The 10-bit parallel data is then sent to the FIFO bridge, which allows the CDR to interface with the rest of the FPGA.

Figure 2.12 shows a block diagram of the SGMII CDR IP.

The two hardened blocks are located at the bottom left of the chip and uses the high speed I/O Bank 5 for the differential pair input. It is recommended that the reference clock should be entered through a GPIO that has connection to the PLL on the lower left corner as well.

For more information about how to implement the hardened CDR for your SGMII solution, refer to the SGMII and Gb Ethernet PCS IP Core (FPGA-IPUG-02077).

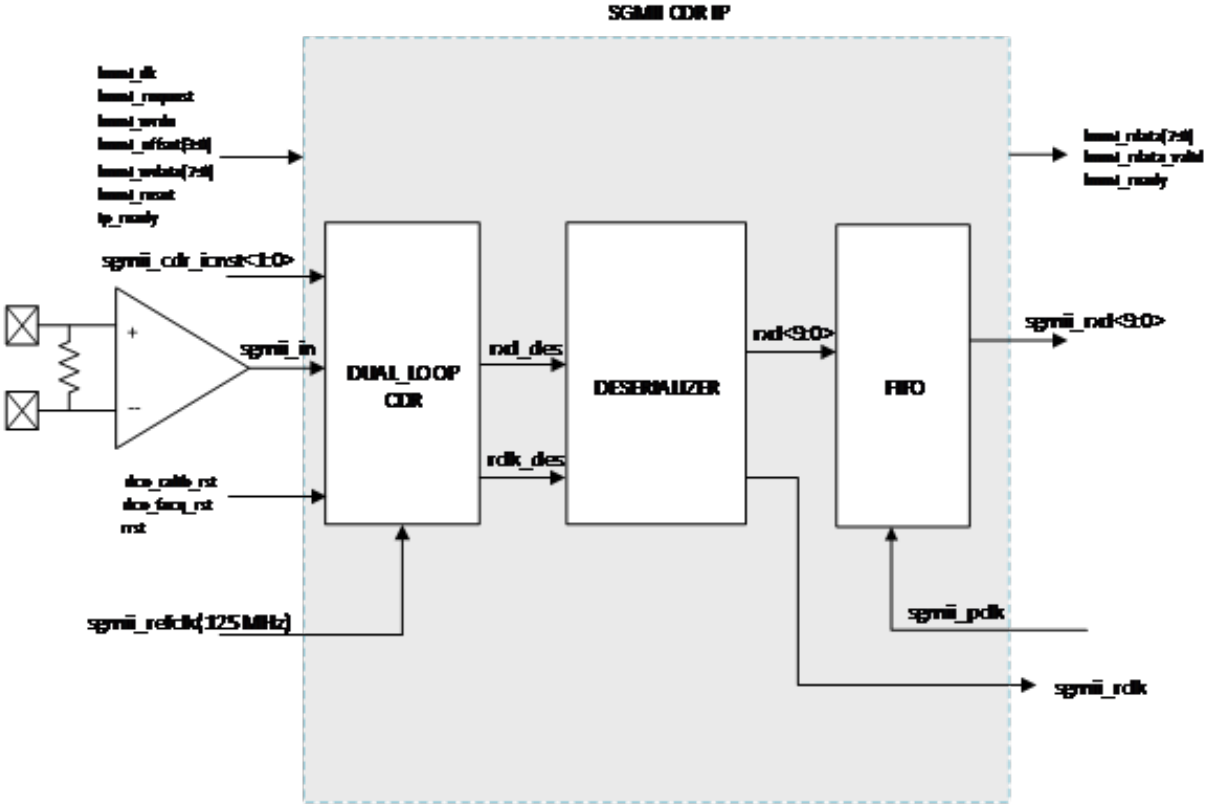


Figure 2.12 SGMII CDR IP

2.6 sysMEM Memory

The CertusPro-NX-RT devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18 kb RAM with memory core, dedicated input registers, and output registers as well as optional pipeline registers at the outputs. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM, and built in FIFO. In CertusPro-NX-RT device, the unused EBR block is powered down to minimize power consumption.

2.6.1 sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as listed in Table 2.4. FIFOs can be implemented using the built-in read and write address counters and programmable full, almost full, empty and almost empty flags. The EBR block facilitates parity checking by support an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with 18-bit and 36-bit data widths. For more information, refer to Memory Usage Guide for Nexus Platform (FPGA-TN-02094).

EBR also provides a built-in ECC engine in Lattice Automotive –7 and –8 speed grades as well as Frontgrade Space PEM QD in –8 speed grade. See ordering information for more details. The ECC engine supports a write data width of 32 bits, and it can be cascaded for larger data widths such as ×64. The ECC parity generator creates and stores parity data for each 32-bit word written. When a read operation is performed, it compares the data with its associated parity data and reports back if any Single Event Upset (SEU) event has disturbed the data. Any single bit data disturb is automatically corrected at the data output. In addition, two dedicated error flags indicate when a single-bit or two-bit error has occurred.

Table 2.4 sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 × 1
	8,192 × 2
	4,096 × 4
	2,048 × 9
	1,024 × 18
	512 × 36
True Dual Port	16,384 × 1
	8,192 × 2
	4,096 × 4
	2,048 × 9
	1,024 × 18
Pseudo Dual Port	16,384 × 1
	8,192 × 2
	4,096 × 4
	2,048 × 9
	1,024 × 18
	512 × 36

2.6.2 Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports, except that the ECC mode only supports a write data width of 32 bits. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

2.6.3 RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during the device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

2.6.4 Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

2.6.5 Single, Dual, and Pseudo-Dual Port Modes

In all the sysMEM RAM modes, the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

2.6.6 Memory Output Reset

The EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset signal, GSRN, can reset both ports. The output data latches and the associated resets for both ports are shown in Figure 2.13. The optional Pipeline Registers at the outputs of both ports are also reset in the same way.

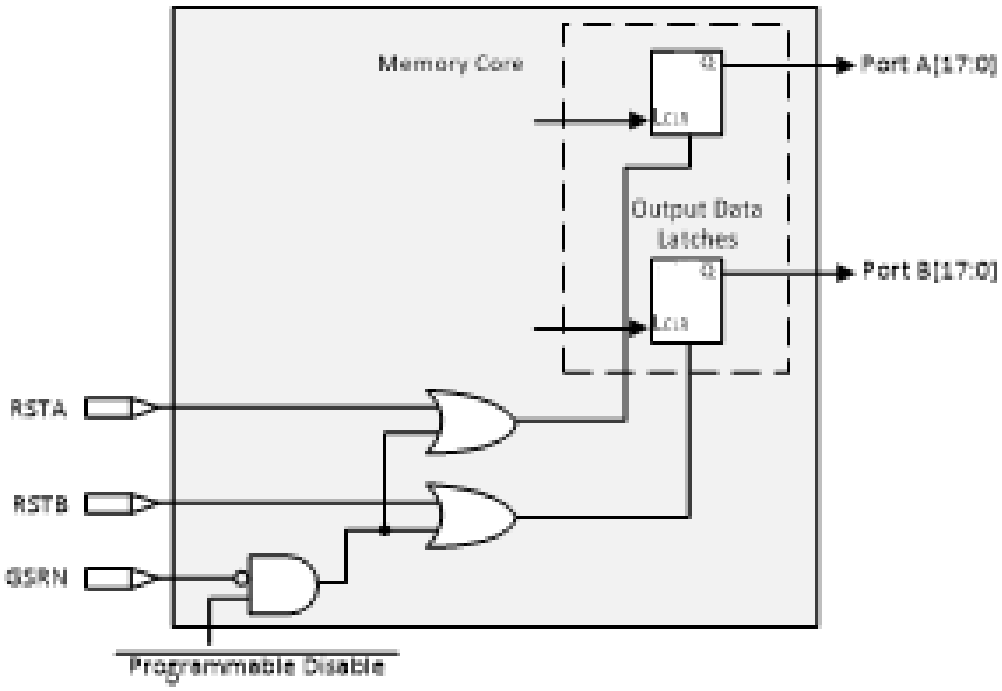


Figure 2.13 Memory Core Reset

For further information on the sysMEM EBR block, see the list of technical documentation in the References section.

2.7 Large RAM

The CertusPro-NX-RT device includes additional memory resources in the form of Large Random Access Memory (LRAM) blocks.

LRAM is designed to work as Single-Port RAM, Dual-Port RAM, Pseudo Dual-Port RAM, and ROM memories. It is meant to function as additional memory resources for you beyond what is available in the EBR and PFU.

Each individual Large RAM block contains 0.5 Mbit of memory, and has a programmable data width of up to 32 bits. Cascading Large RAM blocks allows data widths of up to 64 bits. Additionally, there is the ability to use either Error Correction Coding (ECC) or byte enable.

2.8 sysDSP

The CertusPro-NX-RT family provides an enhanced sysDSP architecture, making it ideally suitable for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks, such as multiply-adders and multiply-accumulators.

2.8.1 sysDSP Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four Multiply and Accumulate (MAC) units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. In the CertusPro-NX-RT device family, many DSP blocks can be used to support different data widths. This allows you to use high parallel implementations of DSP functions. You can optimize DSP performance versus area by choosing appropriate levels of parallelism. Figure 2.14 compares the full serial implementation to the mixed parallel and serial implementation.

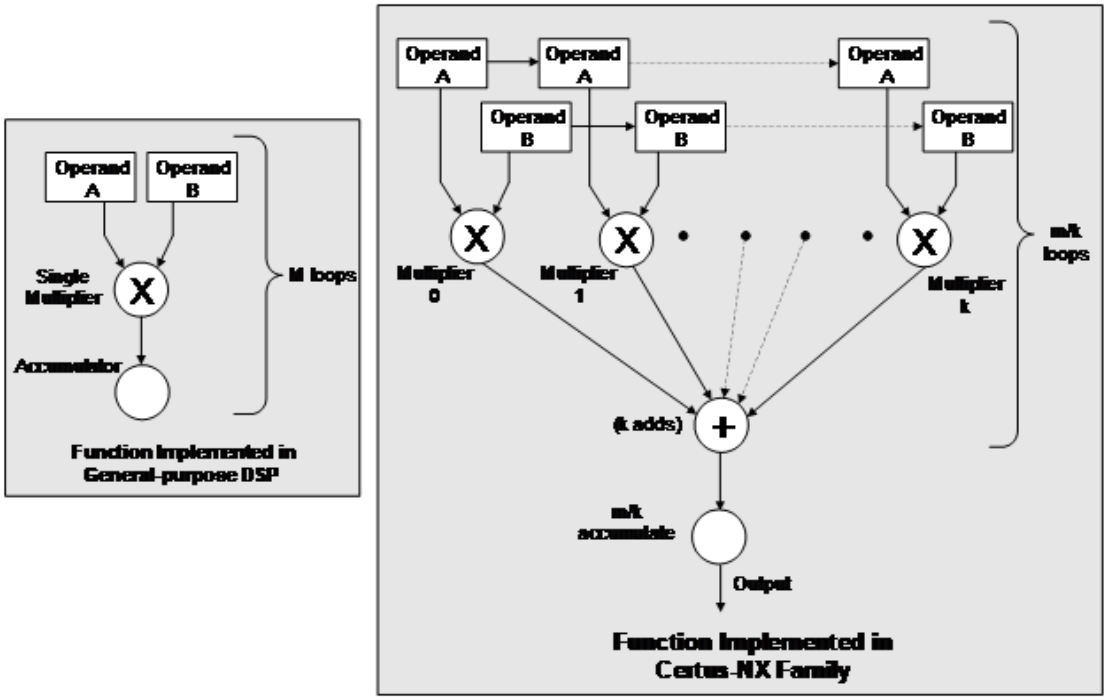


Figure2.14 Comparison of General DSP and CertusPro-NX-RT Approaches

2.8.2 sysDSP Architecture Features

The CertusPro-NX-RT sysDSP block contains two sysDSP slices. The sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The CertusPro-NX-RT sysDSP block containing two sysDSP slices supports many functions including:

- Symmetry support. The primary target application is wireless. 1D Symmetry is useful for many applications that use FIR filters when their coefficients have symmetry or asymmetry characteristics. The main motivation for using 1D symmetry is cost/size optimization. The expected size reduction is up to 2×.
    - Odd Mode – Filter with Odd number of taps.
    - Even Mode – Filter with Even number of taps.
    - Two dimensional (2D) Symmetry Mode – Supports 2D filters for mainly video applications.
- Dual-multiplier architecture. Lower accumulator overhead to half and the latency to half compared to single multiplier architecture.
- Fully cascadable DSP across slices. Support for symmetric, asymmetric and non-symmetric filters.
- Multiply (36 × 36, two 18 × 36, four 18 × 18, or eight 9 × 9).
- Multiply Accumulate (supports one 18 × 36 multiplier result accumulation, two 18 × 18 multiplier result accumulation or four 9 × 9 multiplier result accumulation).
- Two Multiplies feeding one Accumulate per cycle for increased processing with lower latency (two 18 × 18 Multiplies feed into an accumulator that can accumulate up to 54 bits).
- Pipeline registers.
- 1D Symmetry support. The coefficients of FIR filters have symmetry or negative symmetry characteristics.
    - Odd Mode – Filter with Odd number of taps.
    - Even Mode – Filter with Even number of taps.
- 2D Symmetry support. The coefficients of 2D FIR filters have symmetry or negative symmetry characteristics.
    - 3 × 3 and 3 × 5 – Internal DSP Slice support.
    - 5 × 5 and larger size 2D blocks – Semi-internal DSP Slice support.
- Flexible saturation and rounding options to satisfy a diverse set of applications situations.
- Flexible cascading DSP blocks.
    - Minimizes fabric use for common DSP functions.
    - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only.
    - Provides matching pipeline registers.
    - Can be configured to continue cascading from one row of the sysDSP slices to another for longer cascade chains.
- RTL Synthesis friendly synchronous reset on all registers, while still supporting asynchronous reset for legacy users.

- Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources for applications that require processor-like flexibility that enables different functions for each clock cycle.

For most cases, as shown in Figure 2.15, the CertusPro-NX-RT sysDSP block is backwards-compatible with the LatticeECP3™ sysDSP block, such that, legacy applications can be targeted to CertusPro-NX-RT sysDSP, except for the ALU related function. Figure 2.15 is the diagram of sysDSP block.

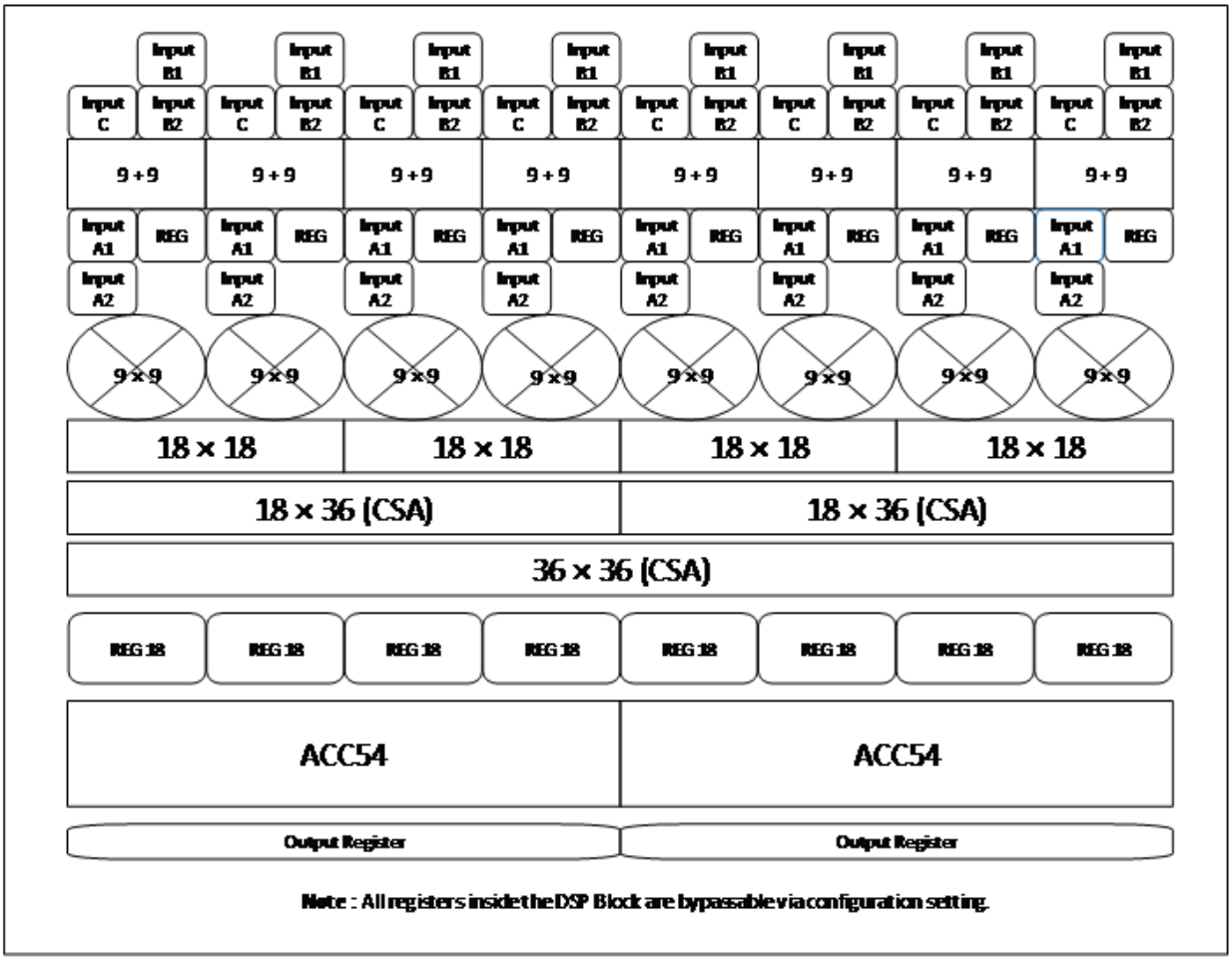


Figure 2.15 CertusPro-NX-RT DSP Functional Block Diagram

The CertusPro-NX-RT sysDSP block supports the following four basic elements:

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2.5 shows the capabilities of CertusPro-NX-RT sysDSP block versus the above elements.

Table 2.5 Maximum Number of Elements in a sysDSP block

Width of Multiply	×9	×18	×36
MULT	8	4	1
MAC	2	2	—
MULTADDSUB	2	2	—
MULTADDSUBSUM	2	2	—

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting dynamic operation, the following operations are possible:

- In the Add/Sub option, the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

For further information, refer to sysDSP Usage Guide for Nexus Platform (FPGA-TN-02096).

2.9 Programmable I/O (PIO)

The programmable logic associated with an I/O is called a Programmable I/O (PIO). Each individual PIO is connected to its respective sysI/O buffers and pads.

On all CertusPro-NX-RT devices, two adjacent PIOs can be combined to provide a complementary output driver pair.

2.10 Programmable I/O Cell (PIC)

The programmable I/O cells (PIC) provides I/O function and necessary gearing logic associated with PIO. CertusPro-NX-RT device has two types of PICs: base PICs and gearing PICs.

Base PICs contain three blocks: an input register block, an output register block, and a tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic (Figure 2.16 and Figure 2.17). Base PICs cover the top and left/right bank. Gearing PICs contain gearing logic and edge monitor used for locating the center of data window. Gearing PICs cover the bottom banks to support DDR operation.

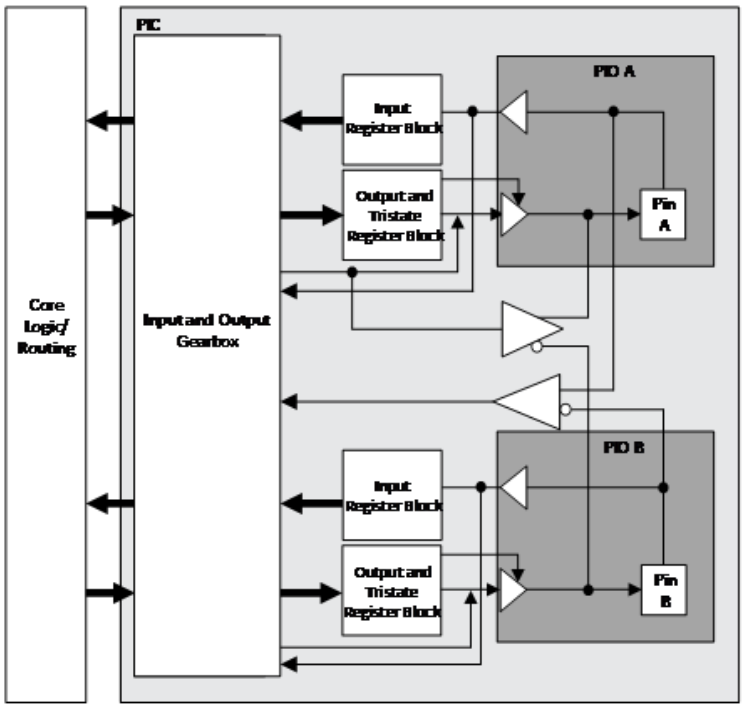


Figure 2.16. A Group of Two High Performance Programmable I/O Cells

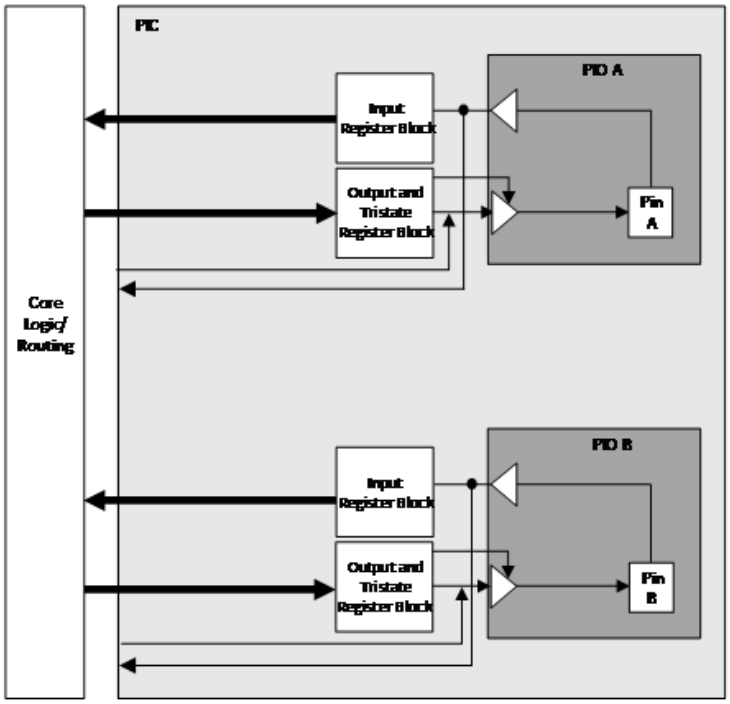


Figure 2.17 Wide Range Programmable I/O Cells

2.10.1 Input Register Block

The input register blocks for the PIO on all edges contain the delay elements and the registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition, the input register blocks for the PIO on the bottom edges include the built-in FIFO logic to interface to DDR and LPDDR memory. Table 2.6 lists all the ports for the input register block.

Table 2.6 Input Block Port Description

Name	Type	Description
D	Input	High-speed data input.
Q[1:0]/Q[3:0]/Q[6:0]/Q[7:0]/Q[9:0]	Output	Low speed data to the device core.
RST	Input	Reset to the output block.
SCLK	Input	Slow speed system clock.
ECLK	Input	High-speed edge clock.
DQS	Input	Clock from DQS Control Block used to clock DDR memory data.
ALIGNWD	Input	Data alignment signal from device core.

The Input register block on the bottom side includes the gearing logic and the registers to implement IDDRX1, IDDRX2, IDDRX4, IDDRX5 gearing functions. With two PICs sharing the DDR register path, it can also implement the IDDRX71 function used for 7:1 LVDS interfaces. It uses three sets of registers – shift, update, and transfer to implement gearing and the clock domain transfer. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. For more information on gearing function, refer to CertusPro-NX High-Speed I/O Interface (FPGA-TN-02216).

Input FIFO

The CertusPro-NX-RT PIO has a dedicated input FIFO per single-ended pin for input data register for DDR Memory interfaces. The FIFO resides before the gearing logic. It transfers data from DQS domain to continuous ECLK domain. On the write side of the FIFO, it is clocked by DQS clock, which is the delayed version of the DQS Strobe signal from DDR memory. On the Read side of FIFO, it is clocked by ECLK. ECLK may be any high-speed clock with identical frequency as DQS, the frequency of the memory chip. Each DQS group has one FIFO control block. It distributes FIFO read/write pointers to every PIC in the same DQS group. DQS grouping and the DQS Control Block are described in 2.12 DDR Memory Support section.

Figure 2.18 shows the input register block for the PIO on the top, left, and right edges.

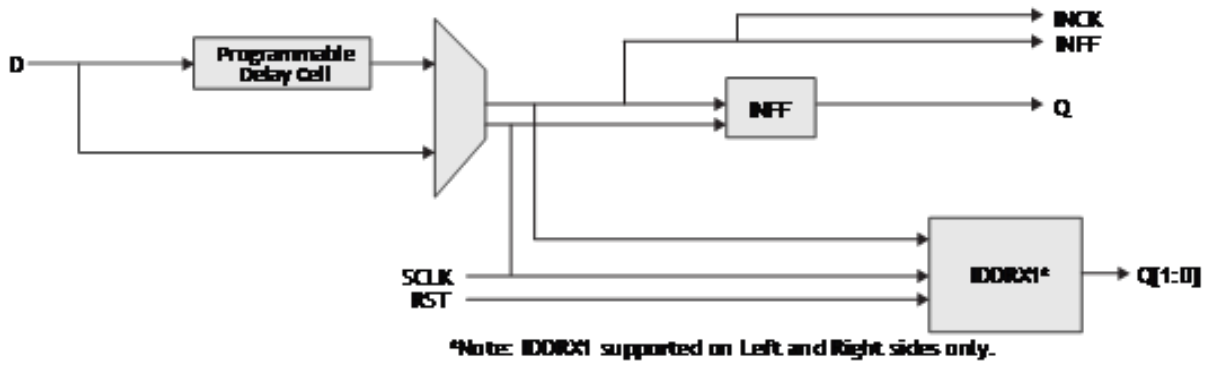


Figure 2.18 Input Register Block for PIO on Top, Left, and Right Sides of the Device

Figure 2.19 shows the input register block for the PIO located on the bottom edge.

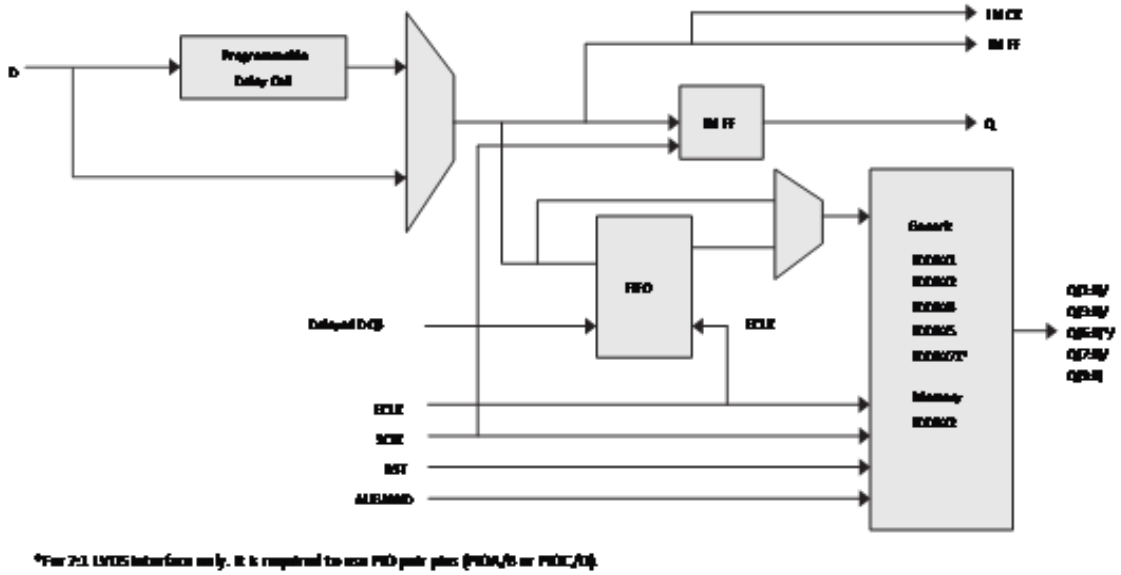


Figure 2.19 Input Register Block for PIO on Bottom Side of the Device

2.10.2 Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysI/O buffers.

CertusPro-NX-RT output data path has programmable registers and output gearing logic. On the bottom side, the output register block can support 1×, 2×, 4×, 5×, and 7:1 gearing enabling high speed DDR and DDR memory interfaces. On the left and right sides, the banks support 1× gearing. The CertusPro-NX-RT output data path diagram is shown in Figure 2.20 and Figure 2.21. The programmable delay cells are also available in the output data path. Table 2.7 lists all the ports for the output register block.

For a detailed description of the output register block modes and usage, you can refer to CertusPro-NX High-Speed I/O Interface (FPGA-TN-02216).

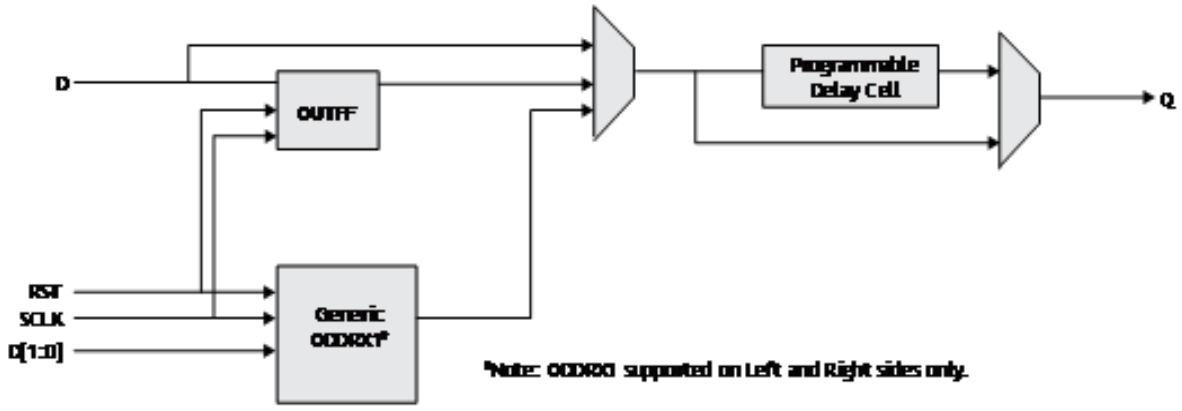


Figure 2.20 Output Register Block on Top, Left, and Right Sides

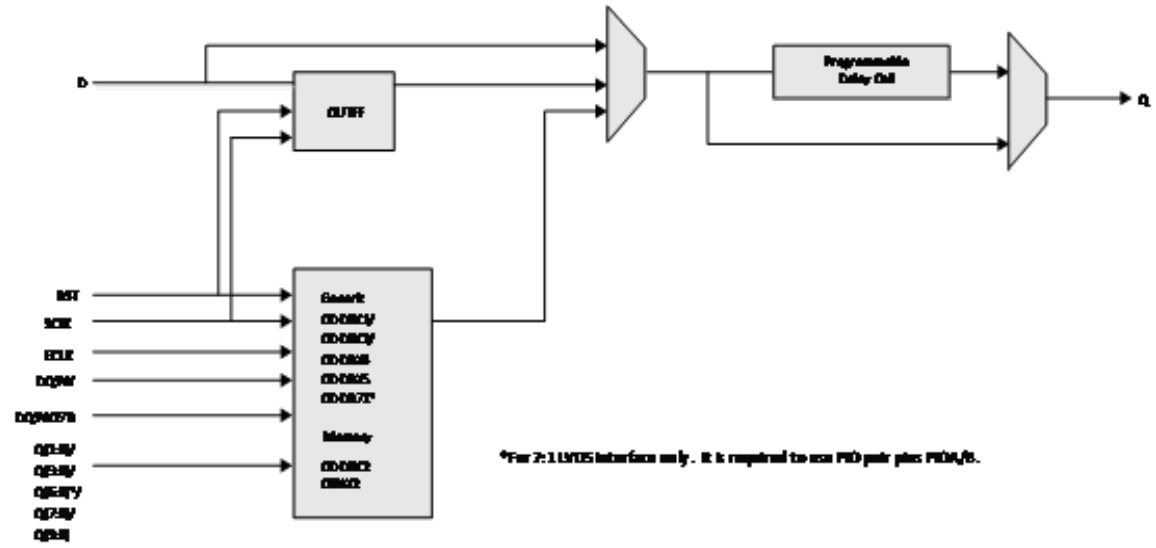


Figure 2.21 Output Register Block on Bottom Side

Table 2.7 Output Block Port Description

Name	Type	Description
Q	Output	High-speed data output.
D	Input	Data from core to output SDR register.
Q[1:0]/Q[3:0]/Q[6:0]/Q[7:0]/Q[9:0]	Input	Low speed data from device core to output DDR register.
RST	Input	Reset to the output block.
SCLK	Input	Slow speed system clock.
ECLK	Input	High-speed edge clock.
DQSW	Input	Clock from DQS Control Block used to generate DDR memory DQS output.
DQSW270	Input	Clock from DQS Control Block used to generate DDR memory DQ output.

2.11 Tri-state Register Block

The tri-state register block registers tristate control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation. In SDR, the TD input feeds one of the flip-flops that can feed the output. In DDR, operations used mainly for DDR memory interfaces can be implemented on the bottom side of the device. In addition, two inputs feed the tristate registers clocked by both ECLK and SCLK. Table 2.8 lists all the ports for the tristate register block.

Figure 2.22 and Figure 2.23 show the Tristate Register Block functions on the device. For a detailed description of the tristate register block modes and usage, you can refer to CertusPro-NX High-Speed I/O Interface (FPGA-TN-02216).

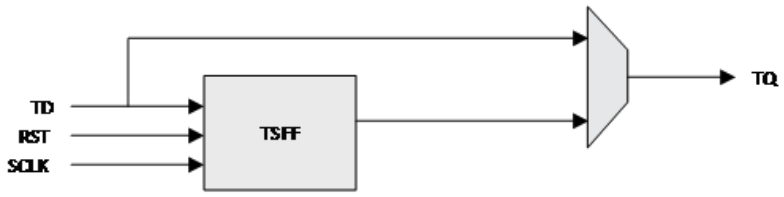


Figure 2.22 Tri-state Register Block on Top, Left, and Right Sides

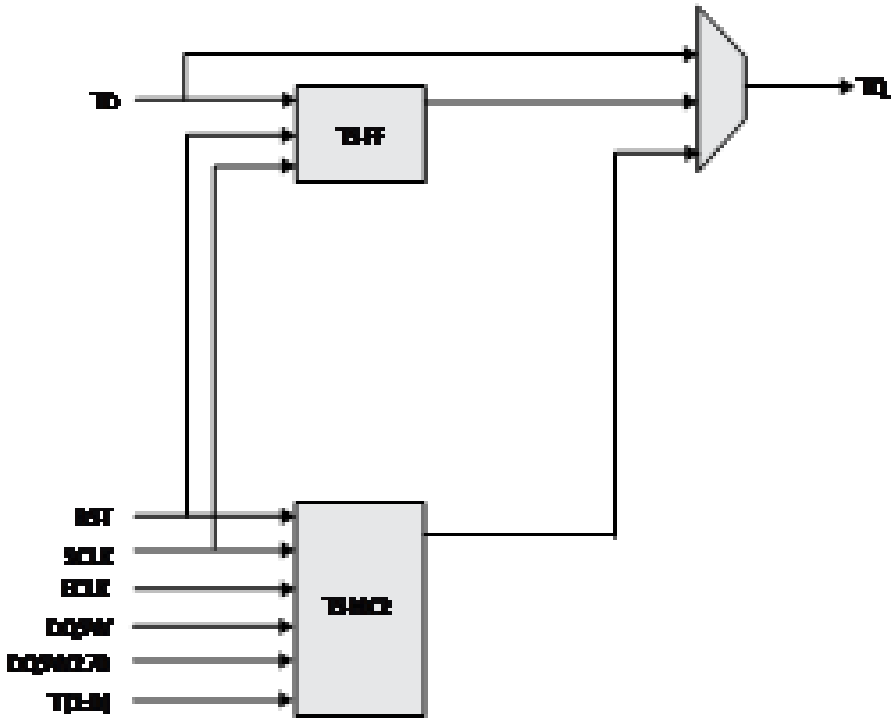


Figure 2.23 Tri-state Register Block on Bottom Side

Table 2.8 Tri-state Block Port Description

Name	Type	Description
TD	Input	Tri-state input to tri-state SDR register.
RST	Input	Reset to the tri-state block.
T [1:0]	Input	Tri-state input to TSHX2 function.
SCLK	Input	Slow speed system clock.
ECLK	Input	High-speed edge clock.
DQSW	Input	Clock from DQS Control Block used to generate DDR memory DQS output.
DQSW270	Input	Clock from DQS Control Block used to generate DDR memory DQ output.
TQ	Output	Output of the Tri-state block.

2.12 DDR Memory Support

2.12.1 DQS Grouping for DDR Memory

Some PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR3/DDR3L, LPDDR2, LPDDR3 or LPDDR4 memory interfaces. The support varies by the edge of the device detailed below.

PICs in the bottom side have fully functional elements supporting DDR3/DDR3L, LPDDR2, LPDDR3, or LPDDR4 memory interfaces. Every 12 PIOs on the bottom side are grouped into one DQS group, as shown in Figure 2.24. Within each DQS group, there are two pre-placed pins for DQS and DQS# signals. The rest of the pins in the DQS group can be used as DQ signals and DM signal. The number of pins in each DQS group bonded out is package dependent. DQS groups with less than 11 pins bonded out can only be used for LPDDR2/3 Command/ Address busses. In DQS groups with more than 11 pins bonded out, pre-defined pins are assigned to be used as virtual VCCIO, by driving them HIGH to make extra connections to the VCCIO power supply. These soft connections to VCCIO help reduce SSO noise. For details, refer to CertusPro-NX High-Speed I/O Interface (FPGA-TN-02216).

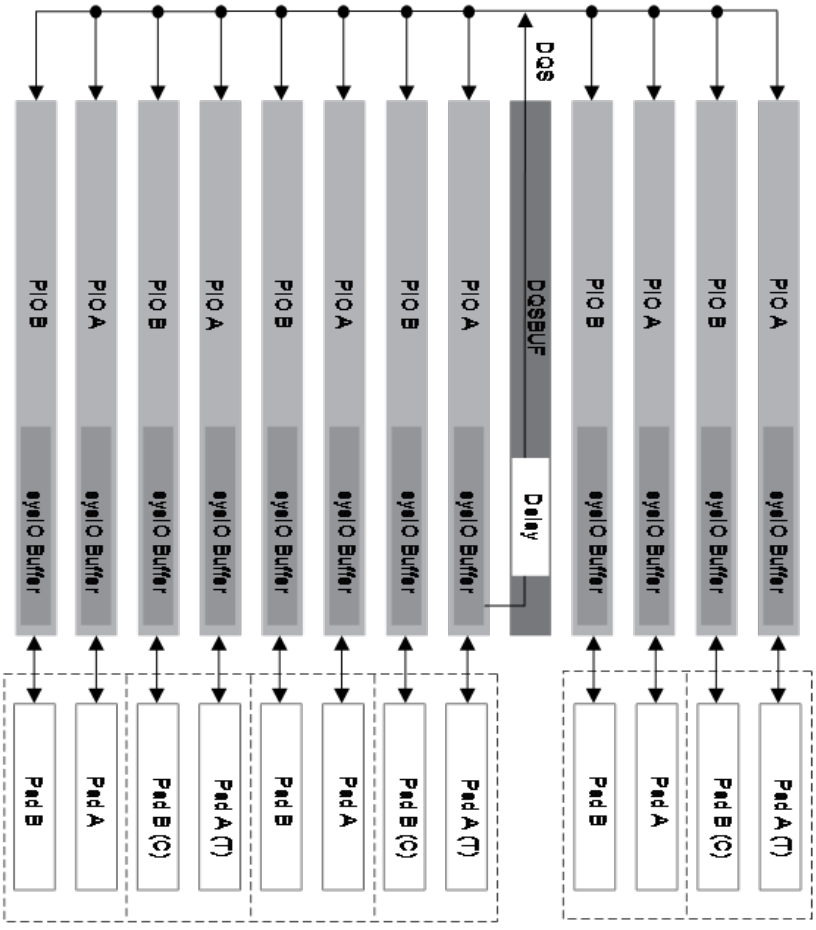


Figure 2.24 DQS Grouping on the Bottom Edge

2.12.2 DLL Calibrated DQS Delay and Control Block (DQSBUF)

To support DDR memory interfaces (DDR3/DDR3L, LPDDR2/3/4), the DQS strobe signal from the memory must be used to capture the data (DQ) in the PIC registers during memory reads. This signal is output from the DDR memory device aligned to data transitions and must be time shifted before it can be used to capture data in the PIC. This time shift is achieved by using the DQSBUF programmable delay line in the DQS Delay Block within DQS read circuit. The DQSBUF is implemented as a slave delay line and works in conjunction with a master DDRDLL.

This block also includes a slave delay line to generate delayed clocks used during writing to generate DQ and DQS with correct phases within one DQS group. There is a third delay line inside this block used to provide write leveling for DDR write if needed.

Each of the read and write side delays can be dynamically shifted using margin control signals from the core logic.

The FIFO Control Block included here generates the Read and Write Pointers for the FIFO inside the Input Register Block. These pointers are generated to control the DQS to ECLK domain crossing using the FIFO module.

Figure 2.25 shows the main functional blocks of the DQSBUF, and Table 2.9 lists all the ports.

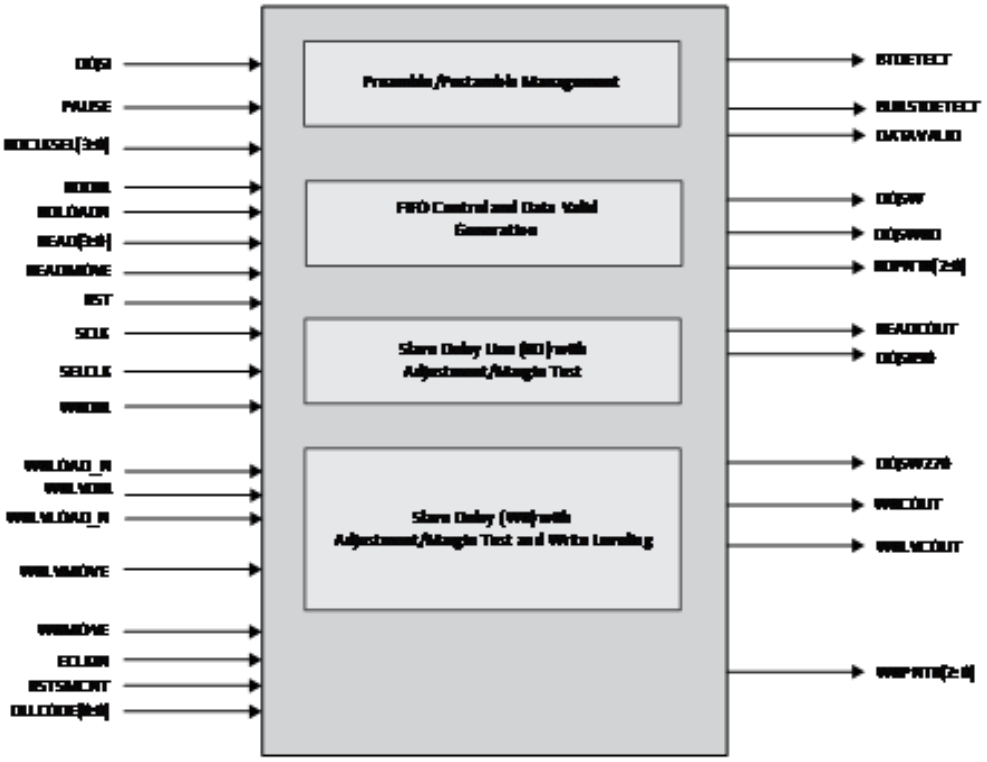


Figure 2.25 DQS Control and Delay Block (DQSBUF)

Table 2.9 DQSBUF Port List Description

Name	Type	Description
DQSI	Input	DQS signal from I/O through the PIC.
PAUSE	Input	To stop ECLK for DDR3 Write leveling and DLL code update.
RDCLKSEL[3:0]	Input	Select read clock source and polarity control (from CIB).
RDDIR	Input	0 – to increase the code. 1 – to decrease the code for DDR read.
RDLOADN	Input	1b0 – When mc1_mt_en_read=1b1 and read_load_n=1b0 the read_move pulse needs to be generated to the load the preload value consisting of the {mc1_sign_read, mc1_s_read [8:0]} value. 1b1 – When counter has preload value, read_move pulse can be used to increment and decrement the counter based on the read_direction signal value and mc1_mt_en_write should be set 1b1.
READ[3:0]	Input	Read signal for DDR read mode (from CIB).
READMOVE	Input	Move pulse needs to be at least 1 sclk cycle and should be greater than 5ns at TT corner. Pulse is used along with the eclk to generate the internal 'mov' signal to update the counter by one value. The count up or down is determined by the read_direction port.
RST	Input	DQS reset control for both DDR/CDR modes (from CIB).
SCLK	Input	SCLK from SCLK tree (CIB).
SELCLK	Input	Select the clock to be used between the output of the read section's delay cell or sclk.
WRDIR	Input	0 – to increase the code. 1 – to decrease the code for DDR write.
WRLOAD_N	Input	1b0 – When mc1_mt_en_write=1b1 and write_load_n=1b0 the write_move pulse needs to be generated to the load the preload value consisting of the {mc1_sign_write, mc1_s_write [8:0]} value. 1b1 – When counter has preload value, write_move pulse can be used to increment and decrement the counter based on the write_direction signal value and mc1_mt_en_write should be set 1b1.
WRLVDIR	Input	0 – to increase the code. 1 – to decrease the code for DDR write leveling.
WRLVLOAD_N	Input	1b0 – 9-bit counter in reset operation. 1b1 – When mc1_mt_en_write_leveling=1b1 and write_leveling_load_n=1b1 the counter can be incremented/decremented based on the direction signal using the write_leveling_move signal.

Name	Type	Description
WRLVMOVE	Input	Move pulse needs to be at least 1 sclk cycle and should be greater than 5 ns at TT corner. Pulse is used along with the eclk to generate the internal 'mov' signal to update the counter by one value. The count up or down is determined by the write_leveling_direction port.
WRMOVE	Input	Move pulse needs to be at least 1 sclk cycle and should be greater than 5ns at TT corner. Pulse is used along with the eclk to generate the internal 'mov' signal to update the counter by one value. The count up or down is determined by the write_direction port.
ECLKIN	Input	ECLK from four different ECLK tree output.
RSTSMCNT	Input	Signal to reset the smoothing counters used for the Read, Write, and Write leveling delays.
DLLCODE[8:0]	Input	DLL code selected from the DLL code routing mux.
BTDETECT	Output	READ burst detect output (to CIB).
BURSTDETECT	Output	The burst_det_sclk signal is generated using burst_det and is asserted on the rising edge of SCLK.
DATAVALID	Output	Data Valid Flag for READ mode (to CIB).
DQSW	Output	ECLK phase shifted or delayed, goes to the dqsw tree through the PIC.
DQSWRD	Output	The read training clock adjusted in the write section. The read_clk_sel[3:0] determines the selected delay and read enable position.
RDPNTR[2:0]	Output	FIFO control READ pointer (3-bits) to FIFO in PIC (through each tree to IOL).
READCOUT	Output	Margin test output flag for READ to indicate the under-flow or over-flow.
DQSR90	Output	DQSI phase shifted or delayed by 90-degree output (through DQSR tree to IOL).
DQSW270	Output	ECLK phase shifted or delayed by 270-degree output (through DQSW270 tree to IOL).
WRCOUT	Output	Margin test output flag for WRITE to indicate the under-flow or over-flow.
WRLVCOUT	Output	Margin test output flag for WRITE LEVELING to indicate the under-flow or over-flow.
WRPNTR[2:0]	Output	FIFO control WRITE pointer (3-bits) to FIFO in PIC (through each tree to IOL).

2.13 sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow you to implement a wide variety of standards that are found in today's systems including LVDS, HSUL, SSTL Class I and II, LVSTL, LVCMOS, LVTTL, and MIPI.

The CertusPro-NX-RT family contains multiple Programmable I/O Cell (PIC) blocks. Each PIC contains two Programmable I/O, PIOA and PIOB. Each PIO includes a sysI/O buffer and I/O logic. Two adjacent PIO can be joined to provide a differential I/O pair referred to as True and Comp, where True Pad is associated with the positive side of the differential I/O, and the complement with the negative.

The top, left, and right side banks support I/O standards from 3.3 V to 1.0 V, while the bottom supports I/O standards from 1.8 V to 1.0 V. Every pair of I/O on the bottom bank also have a true LVDS and SLVS Tx Driver. In addition, the bottom bank supports single-ended input termination. Both static and dynamic terminations are supported. Dynamic termination is used to support the DDR/LPDDR interface standards. For more information about DDR implementation in I/O Logic and DDR memory interface support, refer to CertusPro-NX High-Speed I/O Interface (FPGA-TN-02216).

2.13.1 Supported sysI/O Standards

CertusPro-NX-RT sysI/O buffers support both single-ended and differential standards. Single-ended standards can be further subdivided into internal ratioed standards such as LVCMOS, LVTTL, and external referenced standards such as HSUL, SSTL, and LVSTL. The buffers support the LVTTL, LVCMOS 1.0 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V standards. The supported differential standards include LVDS, SLVS, differential LVCMOS, differential SSTL, differential LVSTL, and differential HSUL. For better support of video standards, subLVDS and MIPI_D-PHY are also supported. Table 2.10 and Table 2.11 provide a list of sysI/O standards supported in CertusPro-NX-RT devices.

Table 2.10 Single-Ended I/O Standards

Standard	Input	Output	Bi-directional
LVTTL33	Yes	Yes	Yes
LVCMOS33	Yes	Yes	Yes
LVCMOS25	Yes	Yes	Yes
LVCMOS18	Yes	Yes	Yes
LVCMOS15	Yes	Yes	Yes
LVCMOS12	Yes	Yes	Yes
LVCMOS10	Yes	No	No
HSTL15 I	Yes	Yes	Yes
SSTL 15 I	Yes	Yes	Yes
SSTL 135 I	Yes	Yes	Yes
HSUL12	Yes	Yes	Yes
LVSTL_I	Yes	Yes	Yes
LVSTL_II	Yes	Yes	Yes
LVCMOS18H	Yes	Yes	Yes
LVCMOS15H	Yes	Yes	Yes
LVCMOS12H	Yes	Yes	Yes
LVCMOS10H	Yes	Yes	Yes
LVCMOS10R	Yes	—	Yes1

Note:

1. Output is supported by LVCMOS10H.

Table 2.11 Differential I/O Standards

Standard	Input	Output	Bi-directional
LVDS	Yes	Yes	Yes
SUBLVDS	Yes	No	—
SLVS	Yes	Yes	—
SUBLVDSE	—	Yes	—
SUBLVDSEH	—	Yes	—
LVDSE	—	Yes	—
MIPI_D-PHY	Yes	Yes	Yes
HSTL15D_I	Yes	Yes	Yes
SSTL15D_I	Yes	Yes	Yes
SSTL15D_II	Yes	Yes	Yes
SSTL135D_I	Yes	Yes	Yes
SSTL135D_II	Yes	Yes	Yes
HSUL12D	Yes	Yes	Yes
LVSTLD_I	Yes	Yes	Yes
LVSTLD_II	Yes	Yes	Yes
LVTTL33D	—	Yes	—
LVCMOS33D	—	Yes	—
LVCMOS25D	—	Yes	—

2.13.2 sysI/O Banking Scheme

CertusPro-NX-RT devices have up to eight banks in total. One bank on the top, two on the left and the right, and three on the bottom. The higher density a CertusPro-NX-RT device has, the more pins are included in each bank. Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7 can support up to VCCIO 3.3 V, while Bank 3, Bank 4, and Bank 5 can support up to VCCIO 1.8 V. In addition, Bank 3, Bank 4, and Bank 5 support two VREF inputs for flexibility to receive two different referenced input levels on the same bank. Figure 2.26 shows the location of each bank.

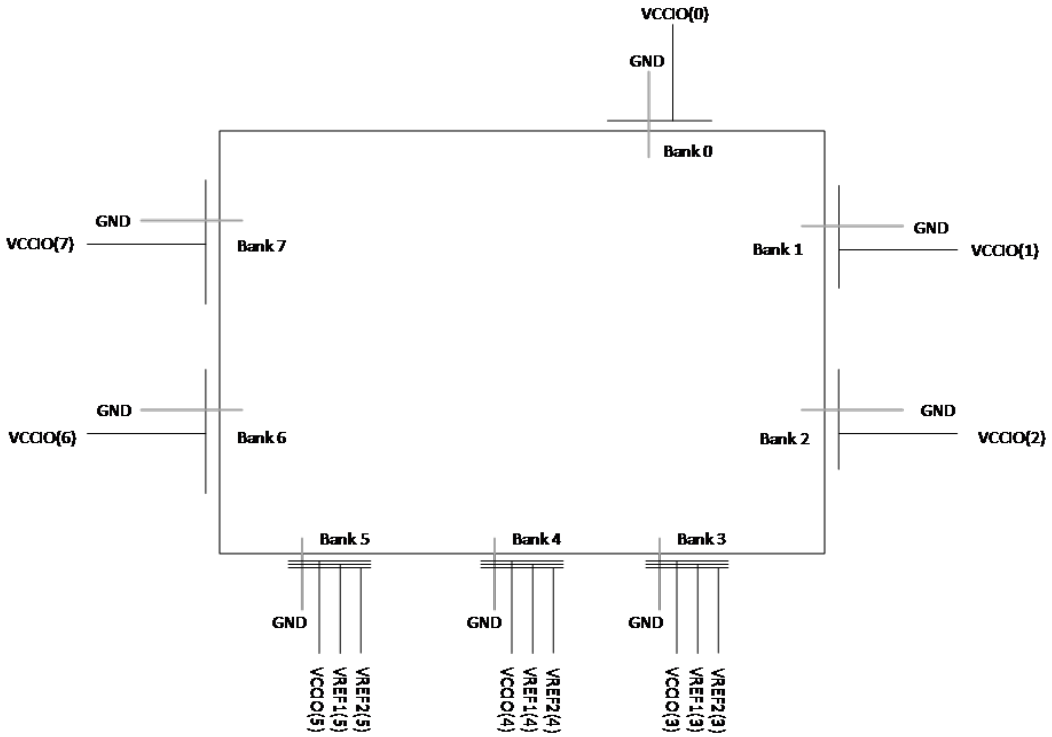


Figure 2.26 sysI/O Banking

Typical sysI/O Behavior During Power-up

The internal Power-On-Reset (POR) signal is deactivated when VCC and VCCAUX have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. You need to ensure that all other VCCIO banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in CertusPro-NX-RT devices, see the list of technical documentation in References section.

VCC and VCCAUX supply the power to the FPGA core fabric, whereas VCCIO supplies power to the I/O buffers. In order to simplify the system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. For the different power supply voltage level by the I/O banks, refer to CertusPro-NX High-Speed I/O Interface (FPGA-TN-02216) for detailed information.

VREF1 and VREF2

Bank 3, Bank 4, and Bank 5 can support two separate VREF input voltages, VREF1 and VREF2. To assign a VREF driver, use IO_Type = VREF1_DRIVER or VREF2_DRIVER. To assign VREF to a buffer, use VREF1_LOAD or VREF2_LOAD.

sysI/O Standards Supported by I/O Bank

All banks can support multiple I/O standards under the VCCIO rules discussed above. Table 2.12 and Table 2.13 summarize the I/O standards supported on various sides of the CertusPro-NX-RT device.

Table 2.12 Single-Ended I/O Standards Support on Various Sides

Standard	Top	Left	Right	Bottom
LVTTL33	Yes	Yes	Yes	—
LVCMOS33	Yes	Yes	Yes	—
LVCMOS25	Yes	Yes	Yes	—
LVCMOS18	Yes	Yes	Yes	—
LVCMOS15	Yes	Yes	Yes	—
LVCMOS12	Yes	Yes	Yes	—
LVCMOS10	Yes	Yes	Yes	—
LVCMOS18H	—	—	—	Yes
LVCMOS15H	—	—	—	Yes
LVCMOS12H	—	—	—	Yes
LVCMOS10H	—	—	—	Yes
LVCMOS10R	—	—	—	Yes
HSTL15 I	—	—	—	Yes
SSTL 15 I, II	—	—	—	Yes
SSTL 135 I, II	—	—	—	Yes
LVSTL I, II	—	—	—	Yes
HSUL12	—	—	—	Yes

Table 2.13 Differential I/O Standards Supported on Various Sides

Standard	Top	Left	Right	Bottom
LVDS	—	—	—	Yes
SUBLVDS	—	—	—	Yes
SLVS	—	—	—	Yes
SUBLVDSE	Yes	Yes	Yes	—
SUBLVDSEH	—	—	—	Yes
LVDSE	Yes	Yes	Yes	—
MIPI_D-PHY	—	—	—	Yes
HSTL15D_I	—	—	—	Yes
SSTL15D_I	—	—	—	Yes
SSTL15D_II	—	—	—	Yes
SSTL135D_I	—	—	—	Yes
SSTL135D_II	—	—	—	Yes
LVSTLD_I	—	—	—	Yes
LVSTLD_II	—	—	—	Yes
HSUL12D	—	—	—	Yes
LVTTL33D	Yes	Yes	Yes	—
LVCMOS33D	Yes	Yes	Yes	—
LVCMOS25D	Yes	Yes	Yes	—

Hot Socketing

The CertusPro-NX-RT devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/O remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits.
Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7 fully support hot socketing. Bank 3, Bank 4, and Bank 5 do not support hot socketing.

2.13.3 sysI/O Buffer Configurations

This section describes various sysI/O features available on the CertusPro-NX-RT device. Refer to sysI/O Usage Guide for Nexus Platform (FPGA-TN-02067) for detailed information.

2.13.4 MIPI D-PHY Support

The programmable I/O of the CertusPro-NX-RT device can be configured as a soft MIPI D-PHYs. The Soft D-PHY can be configured to support either Camera Serial Interface (CSI-2) or Display Serial Interface (DSI) applications as either transmitter or receiver. Below is a summary of the features supported by the Soft D-PHY.

- Transmit and receive function compliant to the MIPI Alliance D-PHY Specification version 1.2.
- High-Speed (HS) and Low-Power (LP) mode support.
    - Supports continuous clock mode or low power non-continuous clock mode.
- Up to 6 Gbps per port (1500 Mbps data rate per lane) in ASG/CBG/LFG package.
- Up to 5 Gbps per port (1250 Mbps data rate per lane) in other packages.
- Supports up to 4 data lanes and one clock lane per port.

2.14 Analog Interface ADC

The CertusPro-NX-RT family can provide an analog interface consisting of two Analog to Digital Convertors (ADC), three continuous time comparators, and an internal junction temperature monitoring diode. This feature is available in Lattice Automotive –7 and –8 speed grades as well as Space PEM QD –8 speed grade. The two ADCs can operate either sequentially or simultaneously.

2.14.1 Analog to Digital Converters

The architecture of each ADC is based upon a 12-bit, 1 MSPS SAR architecture converter. ADC supports both continuous and single shot conversion modes.

Each ADC is supported with a twelve channel analog MUX that is used to select the input from one of the following: dedicated input, dual-function I/O, internal voltage rails, or an internal temperature sensing diode. The input signal can be converted in either uni-polar or bi-polar mode.

The reference voltage is selectable between the 1.2 V internal reference generator and an external reference. An external reference is recommended for any applications that incorporate the ADC. The ADC can convert up to a 1.8 V input signal with a 1.8 V external reference voltage. ADC has an auto-calibration function that calibrates the gain and offset of the SAR (not the internal 1.2 V internal reference).

2.14.2 Continuous Time Comparators

The continuous-time comparator can be used to monitor a dedicated input pair or a GPIO input pair. The output of the comparator is provided as continuous and latched data. Each comparator uses a separate external threshold to provide system flexibility.

2.14.3 Internal Junction Temperature Monitoring Diode

On-die junction temperature can be monitored using the internal junction temperature monitoring diode. The Proportional to Absolute Temperature (PTAT) diode voltage can be monitored by ADC to provide a digital temperature readout. Refer to ADC Usage Guide for Nexus Platform (FPGA-TN-02129) for more details.

2.15 IEEE 1149.1-Compliant Boundary Scan Testability

All CertusPro-NX-RT devices, except for the "01A" Die Version, have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows the functional testing of the circuit board on which the device is mounted, which can provide a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or allowing test data to be captured and shifted out for verification. TAP consists of dedicated I/O including TDI, TDO, TCK, and TMS. TAP uses VCCIO1 for power supply. TAP is supported for VCCIO1 = 1.8 V – 3.3 V

For more information, refer to sysCONFIG Usage Guide for Nexus Platform (FPGA-TN-02099).

2.16 Device Configuration

All CertusPro-NX-RT devices contain various ports that can be used for device configuration, including a Test Access Port (TAP). The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. JTAG_EN is the only dedicated configuration pin. PROGRAMN/INITN/DONE are enabled by default, but can be turned into GPIO. The remaining sysCONFIG pins are used as dual function pins. Refer to sysCONFIG Usage Guide for Nexus Platform (FPGA-TN-02099) for more information about using the dual-use pins as general purpose I/O.

There are various ways to configure a CertusPro-NX-RT device:

- JTAG (TAP)
- Master Serial Peripheral Interface (SPI) – to load from external SPI flash using ×1, ×2, and ×4 (QSPI) interfaces.
- Inter-Integrated Circuit Bus (I^2C)
- Improved Inter-Integrated Circuit Bus (I3C)
- Slave SPI from a system host.
- Lattice Memory Mapped Interface (LMMI). Refer to Lattice Memory Mapped Interface (LMMI) and Lattice Interrupt Interface (LINTR) User Guide (FPGA-UG-02039) for more details.
- JTAG, SSPI, MSPI, I^2C, and I3C are supported for VCCIO = 1.8 V – 3.3 V

On power-up, based on the voltage level (high or low) of the PROGRAMN pin, the FPGA SRAM is configured by the appropriate sysCONFIG port. If PROGRAMN pin is low, the FPGA is in Slave configuration mode (Slave SPI, Slave I^2C, or Slave I3C) waiting for the correct Slave Configuration port activation key. PROGRAMN must be driven high within 50 ns of the end of transmission of the Slave Configuration port activation key, that is, the de-assertion of SCSN. If no slave port is declared active before the PROGRAMN pin is sensed HIGH, the FPGA is in Master SPI booting mode. In Master SPI booting mode, the

FPGA boots from an external SPI flash. Once a configuration port is activated, it remains active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by enabling the JTAG_EN pin and sending the appropriate command through the TAP port.

2.16.1 Enhanced Configuration Options

CertusPro-NX-RT devices have enhanced configuration features such as:

- Early I/O release
- Bitstream decryption and authentication
- Decompression support
- TransFR I/O
- Watchdog Timer support
- Dual and Multi-boot image support

Early I/O Release

Early I/O Release is a new configuration feature in which certain I/O banks are released earlier so that customer systems have minimal disruption. For more details, refer to sysCONFIG Usage Guide for Nexus Platform (FPGA-TN-02099).

Transparent Field Reconfiguration (TransFR)

TransFR I/O (TFR) is a unique Lattice technology that allows you to update your logic in the field without interrupting system operation. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime.

Watchdog Timer

Watchdog Timer is a new configuration feature that helps you add a programmable timer option for timeout applications.

Dual-boot and Multi-boot Image Support

Dual-boot and multi-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update to the CertusPro-NX-RT device, this device can be re-booted from this new configuration file. If there is a problem, such as corrupt data during downloading or incorrect version number with this new boot image, the CertusPro-NX-RT device can revert back to the original backup golden configuration and try again. All these actions can be done without power cycling the system. For more information, refer to sysCONFIG Usage Guide for Nexus Platform (FPGA-TN-02099).

2.17 Single Event Upset (SEU) Handling

CertusPro-NX-RT devices are unique in the underlying technology used to build these devices, which is much more robust and less prone to soft errors.

CertusPro-NX-RT devices have an improved, hardware implemented, Soft Error Detection (SED) circuit that can be used to detect SRAM errors so they can be corrected. Two layers of SED implemented in CertusPro-NX-RT family can make the device more robust and reliable.

The SED hardware in CertusPro-NX-RT devices is part of the Configuration block. The SED module in CertusPro-NX-RT is an enhanced version as compared to the SED modules implemented in other Lattice devices. The configuration data is divided

into frames so that the entire FPGA can be programmed precisely with ease. The SED hardware reads data from the FPGAs configuration memory and performs an Error Correcting Code (ECC) calculation on every frame of the configuration data. Once an error is detected, a notification is generated and SED resumes operation. For single-bit errors, the corrected value is rewritten to the particular frame using ECC information. If more than one-bit error is detected within one frame of configuration data, an error message is generated. CertusPro-NX-RT devices also have dedicated logic to perform Cycle Redundancy Code (CRC) checks for the entire bitstream, which runs in parallel along with ECC.

After the ECC is calculated on all frames of configuration data, CRC is calculated and checked for the entire bitstream. ECC and CRC checks do not include the contents of RAMs (EBR, Large SRAM and distributed RAM memory).

For further information on SED support, refer to Soft Error Detection (SED)/Correction (SEC) Usage Guide for Nexus Platform (FPGA-TN-02076).

2.18 On-chip Oscillator

The CertusPro-NX-RT device features two on-chip oscillators. Both oscillators are controlled with internal generated current.

The low frequency oscillator (LFOSC) is tailored for low power operation and runs at nominal frequency of 32 kHz. The LFOSC always runs and can be used to perform always-on functions with lowest possible power. The high frequency oscillator (HFOSC) runs at normal frequency of 450 MHz, but can be divided down to a range of 256 MHz to 2 MHz by user attributes.

2.19 User I²C IP

The CertusPro-NX-RT device has one hard I²C interface, which can be configured either as a master (controller) or as slave (responder). The pins for the I²C interface are pre-assigned.

The interface core has the option to delay either the input or the output data (SDA), or both, by 50 ns nominal, using dedicated on-chip delay elements. This provides an easier interface to any external I²C components. In addition, 50 ns glitch filters are available for both SDA and SCL.

When the interface is configured as a master (controller), it is able to control other devices on the I²C bus through the pre-assigned pins. When the core is configured as a slave (responder), the device is able to provide, for example, I/O expansion to an I²C Master (controller). The I²C core supports the following functionalities:

- Master (controller) and slave (responder) operation
- 7-bit and 10-bit addressing
- Multi-Master (controller) arbitration
- Clock stretching
- Up to 1 MHz data transfer speed including Standard-mode, Fast-mode, and Fast-mode plus
- General call
- Optional receive and transmit data FIFOs with programmable sizes
- Optional 50 ns delay on input or output data (SDA), or both
- Hard-connection and Programmable I/O connection
- Programmable to a mode compliant with I3C requirements on legacy I²C Slave devices

- Fast-mode and Fast-mode plus
- Disable clock stretching
- 50 ns SCL and SDA glitch filters
- Programmable 7-bit address

For further information on the User I^2C, refer to I^2C Hardened IP Usage Guide for Nexus Platform (FPGA-TN-02142).

2.20 Pin Migration

The CertusPro-NX-RT family is designed to ensure that different density devices in the same family and in the same package having the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a low resource utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization impact the likelihood of success in each case. An example is that some user I/O may become No Connects in smaller devices in the same package. Refer to the CertusPro-NX-RT Pin Migration Tables and Lattice Radiant software for specific restrictions and limitations.

2.21 SerDes and Physical Coding Sublayer

CertusPro-NX-RT FPGAs feature up to eight channels of embedded SerDes/PCS arranged in quad blocks at the top of the device (Figure). Each channel supports data rates up to 6.25 Gbps. Here, only devices with –9 speed grade can support 6.25Gbps SerDes usages. Figure 2.1 shows the position of the quad blocks for the LFCPNX-100 family. Table 2.14 shows the SerDes standards supported by CertusPro-NX-RT devices. Table 2.15 shows the number of the available SerDes/PCS channels for each CertusPro-NX-RT device.

CertusPro-NX-RT SerDes are organized in quads of four. Each CertusPro-NX-RT SerDes quad includes four dedicated SerDes for high speed, full duplex serial data transfer. Each quad also contains one PCI Express PCS hard block. The PCI Express PCS is designed only for PCI Express. Each CertusPro-NX-RT device contains one PCI Express hard Link Layer block. The PCI Express Link Layer block contains one ×1 engine and one ×4 engine. The ×4 PCI Express Link Layer engine can be configured in ×1, ×2 or ×4 mode. The PCI Express Link Layer block, PCI Express PCS block and SerDes channels constitute the complete PCI Express Hard IP block.

CertusPro-NX-RT devices also have a generic purpose Multi-protocol PCS (MPCS) and related support logic. CertusPro-NX-RT device also has protocol specific logic to support the standards listed below (Table 2.14). All PCS fabric interface logic for dedicated protocol support can also be bypassed to allow raw 8-bit or 10-bit interfaces to the FPGA fabric. Even though the SerDes/PCS blocks are arranged in quads, multiple baud rates can be supported within a quad with the use of a dedicated, per channel, Tx PLL. Additionally, multiple quads can be linked together to form larger data pipes. For information on how to use the SerDes/PCS blocks to support specific protocols, as well as on how to combine multiple protocols and baud rates within a device, refer to CertusPro-NX SerDes/PCS Usage Guide (FPGA-TN-02245).

Each SerDes channel integrates a CDR/PLL for Receiver and a PLL for Transmitter, and each channel can be configured to connect to the PCI Express PCS or the MPCS independently.

> **Note: Please refer to the Ordering_Information section of this document for details concerning device Lot ID–specific limitations on SERDES functional capability.**

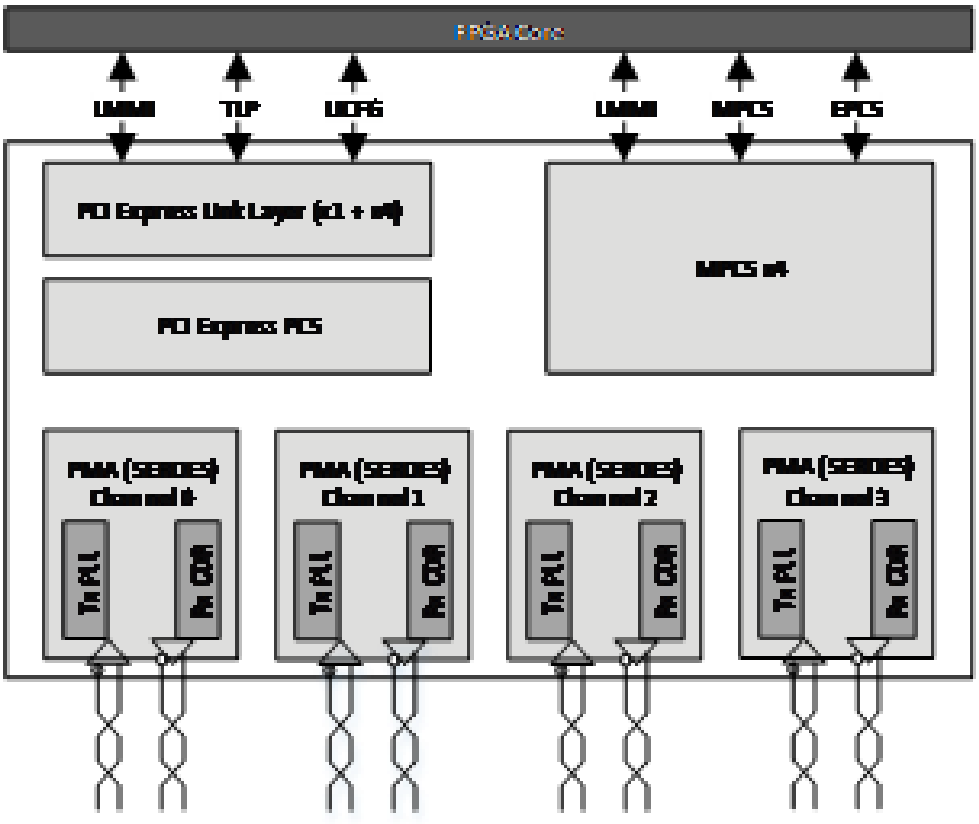


Figure 2.27 SerDes/PCS Overall Structure

The CertusPro-NX-RT SerDes/PCS supports a range of popular serial protocols including:

- PCI Express Gen1 (2.5 Gbps), and Gen 2 (5.0 Gbps) speed
- Ethernet
    - SGMII
    - XAUI at 3.125 Gbps per lane
- SLVS-EC at 1.25 Gbps, 2.5 Gbps and 5 Gbps
- DP/eDP at 1.62 Gbps (RBR), 2.7 Gbps (HBR), and 5.4 Gbps (HBR2)
- CoaXPress at 1.25 Gbps, 2.5 Gbps, 3.125 Gbps, 5 Gbps, and 6.25 Gbps
- Generic 8b10b with multiple data rates supported
- SerDes-only mode allowing a direct 8-bit or 10-bit interface to FPGA logic

Table 2.14 CertusPro-NX-RT SerDes Standard Support

Standard	Data Rate (Mbps)	System Reference Clock (MHz)	FPGA Clock (MHz)	Number of Link Width	Encoding Style
PCI Express Gen1	2500	100	125	×1, ×2, ×4	8b10b
PCI Express Gen2	5000	100	125	×1, ×2, ×4	8b10b
Ethernet SGMII	1250	125	125	×1	8b10b
Ethernet XAUI	3125	156.25	156.25	×4	8b10b
SLVS-EC Grade1	1250	125	125	×1~×8	8b10b
SLVS-EC Grade2	2500	125	125	×1~×8	8b10b
SLVS-EC Grade3	5000	125	125	×1~×8	8b10b
CoaXPress	1250	125	125	×1~×4	8b10b
	2500	125	125	×1~×4	8b10b
	3125	156.25	156.25	×1~×4	8b10b
	5000	125	125	×1~×4	8b10b
	6250	156.25	156.25	×1~×4	8b10b
DP/eDP RBR	1620	108	162	×1, ×2, ×4	8b10b
DP/eDP HBR	2700	135	135	×1, ×2, ×4	8b10b
DP/eDP HBR2	5400	135	135	×1, ×2, ×4	8b10b
10-Bit SerDes	625 – 6250	—	—	×1~×8	None
8-Bit SerDes	625 – 6250	—	—	×1~×8	None
Generic 8b10b	625 – 6250	—	—	×1~×8	8b10b

Notes:

1. BBG package can support standards with data rate up to 6.25 Gbps.
2. BFG package can support standards with data rate up to 5.5 Gbps.

Table 2.15 Number of SerDes/PCS Channel per CertusPro-NX-RT Device

Package	LFCPNX-100
BBG484	8

2.21.1 SerDes Block

A SerDes receiver channel can receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SerDes transmitter channel can receive parallel 8- or 10-bit data from the PCS block or directly from the fabric, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2.28 shows a single-channel SerDes/PCS block. Each SerDes channel provides a recovered clock and a SerDes transmit clock to the PCS block and to the FPGA core logic. Each transmit channel and receiver channel shares the same power supply (VCCSD). VCCPLLSD provides power to the SerDes PLL, and VCCAUXSD provides power to the SerDes Auxiliary block.

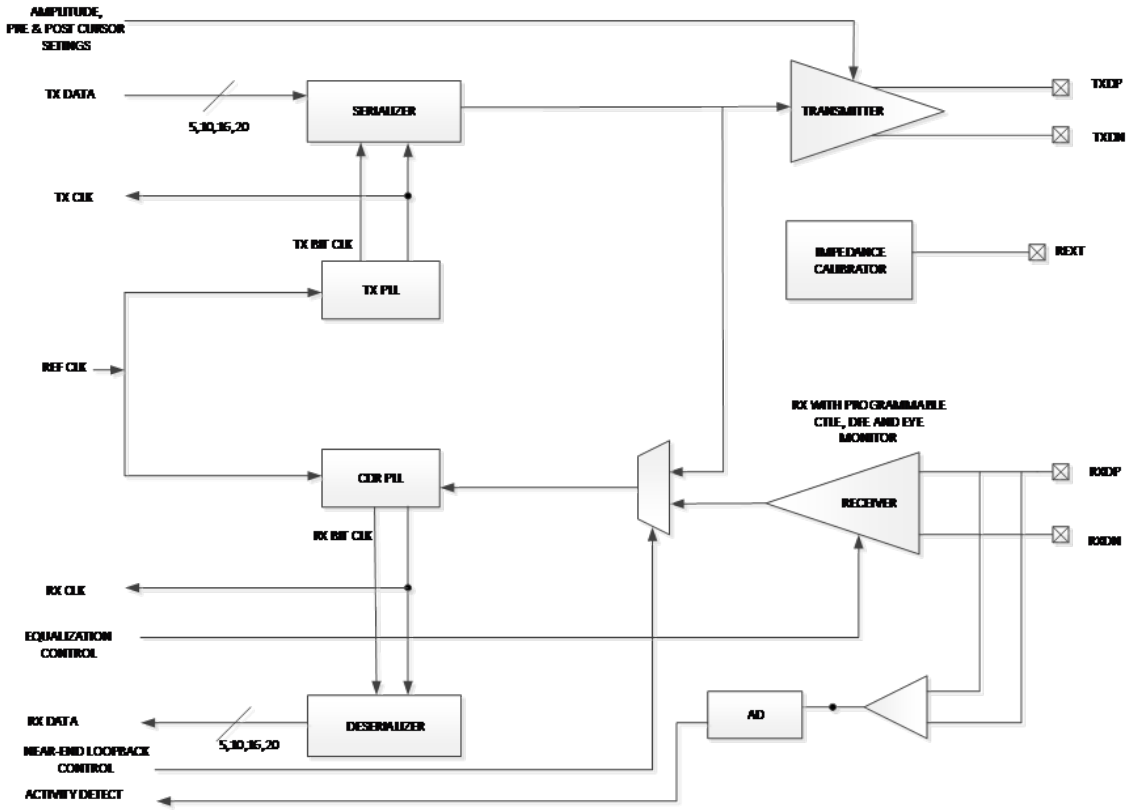


Figure 2.28 Single-channel Block Diagram for SerDes Block

2.21.2 MPCS

As shown in Figure 2.29, Figure 2.30, Figure 2.31, and Figure 2.32, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b10b), provides the clock tolerance compensation and transfers the clock domain from the recovered clock to the FPGA clock via the downsampled FIFO. For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b10b or 64b66b, selects the polarity and passes the 8/10/66 bits data to the transmit-SerDes channel. The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SerDes to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 2× bus width interface to the FPGA logic.

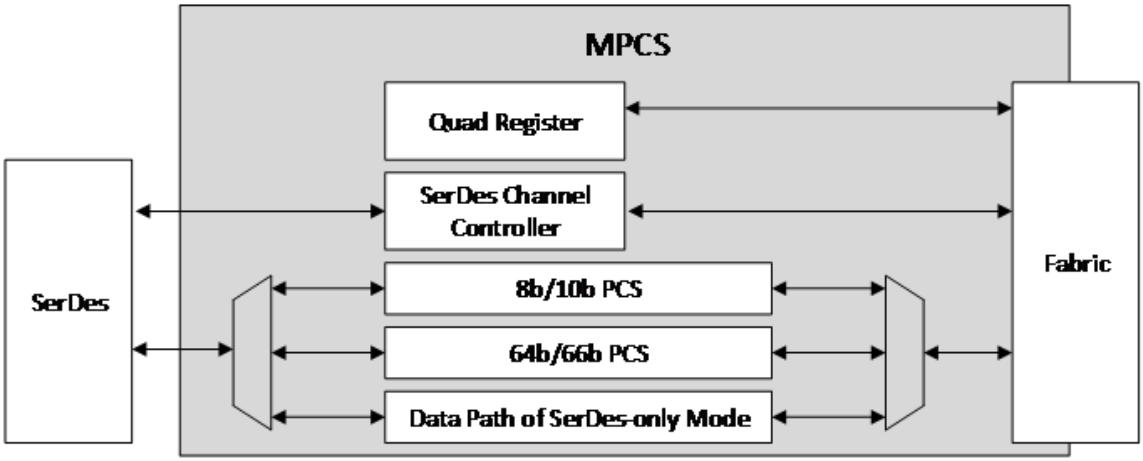


Figure 2.29 Simplified Channel Block Diagram for MPCS Block

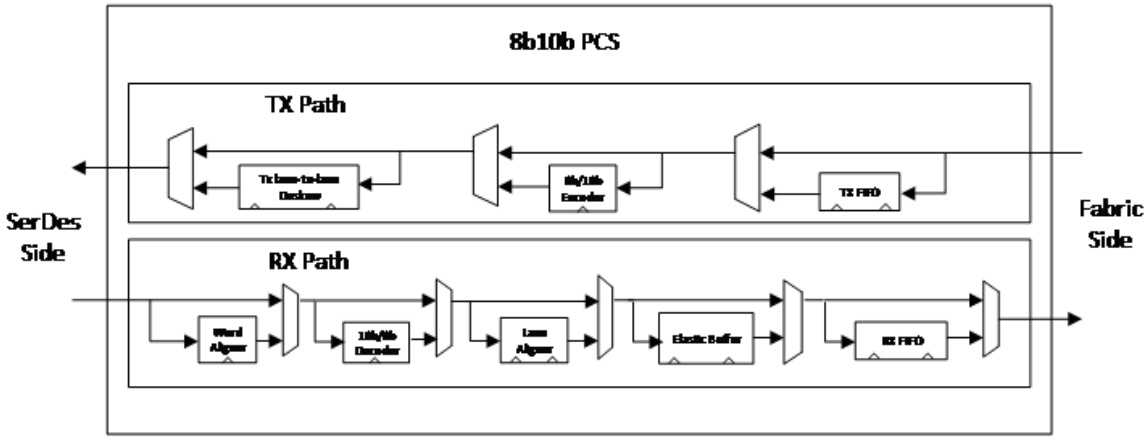


Figure 2.30 Simplified Channel Block Diagram for MPCS 8b10b Sub-Block

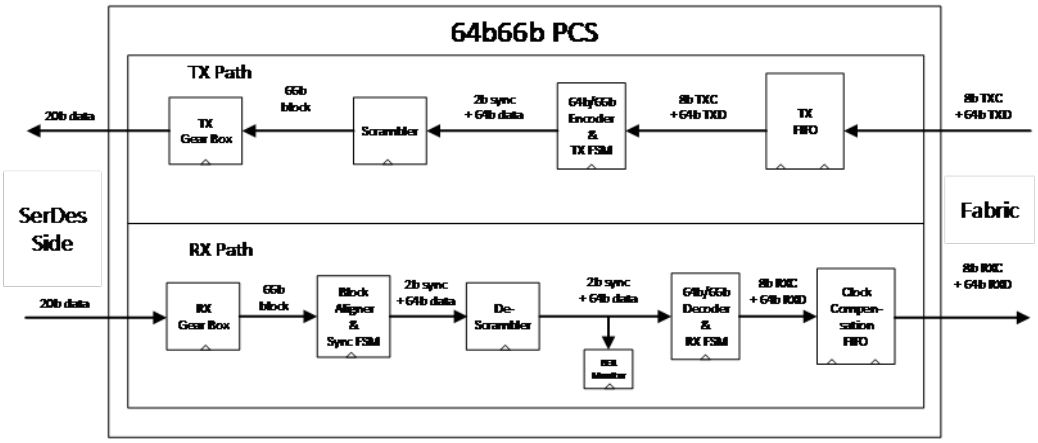


Figure 2.31 Simplified Channel Block Diagram for MPCS 64b66b Sub-Block

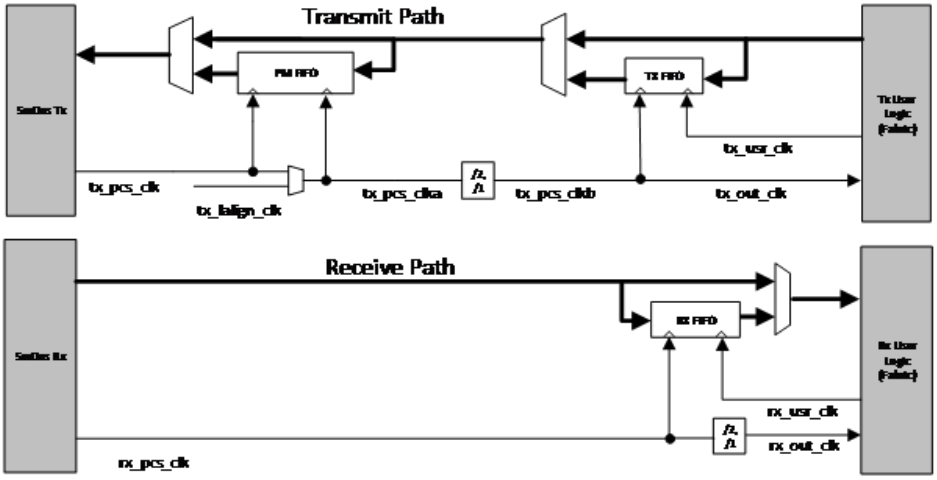


Figure 2.32 Simplified Channel Block Diagram for MPCS SerDes-only Sub-Block

2.21.3 Peripheral Component Interconnect Express (PCIe)

The CertusPro-NX-RT device features one hardened PCIe block on the top side of the device. The PCIe block implements all the three layers defined by the PCI Express Specification: Physical, Data Link, and Transaction, as shown in Figure 2.33. Below is a summary of the features supported by the PCIe bock:

- Gen 1 (2.5 Gbps), and Gen 2 (5.0 Gbps) speed
- PCIe Express Base Specification 3.0 compliant including compliance with earlier PCI Express Specifications
- Multi-function support with up to four physical functions
- Endpoint and root complex

- Type 0 configuration registers in Endpoint mode
- Complete error-handling support
- 32-bit core data width
- Many power management features including power budgeting

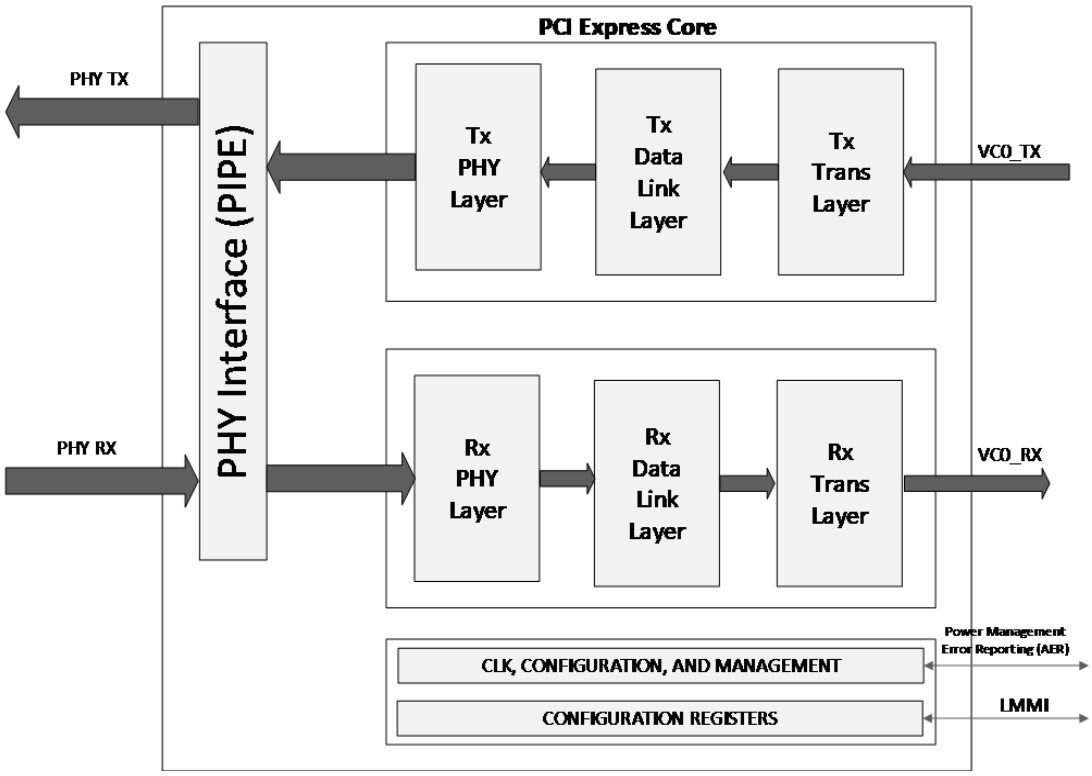


Figure 2.33 PCIe Core

The hardened PCIe block can be instantiated with the primitive PCIe through Lattice Radiant software, however, it is not recommended to directly instantiate the PCIe primitive itself. It is highly recommended to generate the PCIe Endpoint Soft IP through the Radiant IP Catalog and IP Block Wizard instead. In Figure 2.34, the PCIe core is configured as Endpoint using a Soft IP wrapper that provides useful functions such as bridging support for bus interfaces and DMA applications. In addition to the standard Transaction Layer Packet (TLP) interface, the data interface can also be configured to be AXI4 or AHB-Lite as well. The PCIe hardened block also features a register interface for LMMI and User Configuration Space Register Interface (UCFG). The PCIe block has many registers that contain information about the current status of the PCIe block as well as the capability to dynamically switch PCIe settings. One easy way to access these registers is through the Reveal Controller Tool.

For more information about the PCIe soft IP, refer to the Lattice PCIe IP Core document.

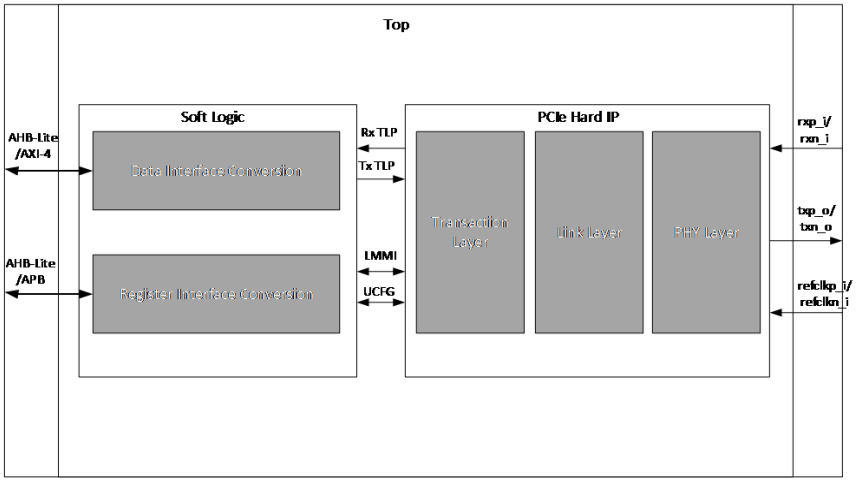


Figure 2.34 PCIe Soft IP Wrapper

2.21.4 LMMI (Lattice Memory Map Interface) Bus

The LMMI is an IP interface that allows the SerDes/PCS Quad block to be controlled by registers rather than the configuration memory cells. It is a simple register configuration interface that allows SerDes/PCS configuration without power cycling the device.

2.22 Cryptographic Engine

The CertusPro-NX-RT family of devices support several cryptographic features that help secure your design. Some of the key cryptographic features include Advanced Encryption Standard (AES) encryption, Hashing Algorithms, and true random number generation (TRNG). The CertusPro-NX-RT device also features bitstream encryption (using AES-256) for protecting confidential FPGA bitstream data, and bitstream authentication (using ECDSA) that maintains bitstream integrity.

The Cryptographic Engine (CRE) is the main block, which is responsible for bitstream encryption as well as authentication of the CertusPro-NX-RT device. Once the bitstream is authenticated and the device is ready for user functions, the CRE is available to implement various cryptographic functions in your FPGA design. To enable specific cryptographic function, the CRE has to be configured by setting a few registers.

The Cryptographic Engine supports the following user-mode features:

- True Random Number Generation (TRNG)
- Secure Hashing Algorithm (SHA)-256 bit
- Message Authentication Codes (MACs) – HMAC
- Lattice Memory Mapped Interface (LMMI) to user logic
- High Speed Port (HSP) for FIFO-based streaming data transfer

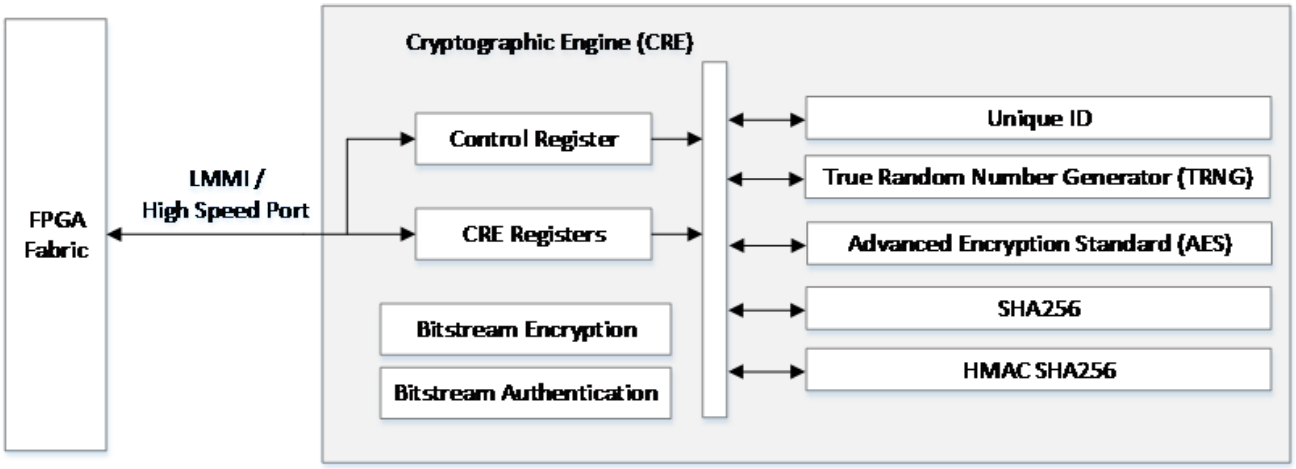


Figure 2.35 Cryptographic Engine Block Diagram

2.23 TraceID

Each CertusPro-NX-RT device contains a unique (per device) TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable. The remaining 56 bits are factory-programmed. The TraceID is accessible through the SPI, I^2C, or JTAG interfaces. For further information on TraceID, refer to Using TraceID (FPGA-TN-02084).

3. DC and Switching Characteristics for Lattice Automotive and Frontgrade Space PEM QD

Frontgrade datasheet parameters are derived from the equivalent Lattice datasheet. Only parameters specifically noted in each table are retested at Frontgrade as part of RLAT testing.

All specifications in this section are characterized within recommended operating conditions unless otherwise specified.

Note: All the data in this section is preliminary. The specifications included in this section are subject to change without prior notice.

Frontgrade CertusPro-NX-RT parts are based on Frontgrade's Space PEM QD flow screened Lattice CertusPro-NX Automotive grade devices.

3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}, V_{CCECLK}	Supply Voltage	–0.5	1.10	V
V_{CCAUX}, V_{CCAUXA}, $V_{CCAUXH3}$, $V_{CCAUXH4}$, $V_{CCAUXH5}$	Supply Voltage	–0.5	1.98	V
$V_{CCIO0, 1, 2, 6, 7}$	I/O Supply Voltage	–0.5	3.63	V
$V_{CCIO3, 4, 5}$	I/O Supply Voltage	–0.5	1.98	V
$V_{CCPLLSD}$*	SerDes Block PLL Supply Voltage	–0.5	1.98	V
V_{CCSD}*	SerDes Supply Voltage	–0.5	1.10	V
V_{CCSDCK}	SerDes Clock Buffer Supply Voltage	–0.5	1.10	V
$V_{CCADC18}$	ADC Block 1.8 V Supply Voltage	–0.5	1.98	V
$V_{CCAUXSDQ}$*	SerDes AUX Supply Voltage	–0.5	1.98	V
—	Input or I/O Voltage Applied, Bank 0, Bank 1, Bank 2, Bank 6, Bank 7	–0.5	3.63	V
—	Input or I/O Voltage Applied, Bank 3, Bank 4, Bank 5	–0.5	1.98	V
—	Voltage Applied on SerDes Pins	–0.5	1.98	V
T_A	Storage Temperature (Ambient)	–65	+150	°C
T_J	Junction Temperature	—	+125	°C

Notes:

1. Stress above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. All VCCAUX should be connected on PCB.

3.2 Recommended Operating Conditions

Table 3.2 Recommended Operating Conditions [1, 2, 3,4]

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
V_{CC}, V_{CCECLK}	Core Supply Voltage	V_{CC} = 1.0	0.95	1.00	1.05	V
V_{CCAUX}	Auxiliary Supply Voltage	Bank 0, Bank 1, Bank 2, Bank 6, Bank 7	1.71	1.80	1.89	V
$V_{CCAUXH3/4/5}$	Auxiliary Supply Voltage	Bank 3, Bank 4, Bank 5	1.71	1.80	1.89	V
V_{CCAUXA}	Auxiliary Supply Voltage for core logic	—	1.71	1.80	1.89	V
V_{CCIO}	I/O Driver Supply Voltage	VCCIO = 3.3 V, Bank 0, Bank 1, Bank 2, Bank 6, Bank 7	3.135	3.30	3.465	V
		VCCIO = 2.5 V, Bank 0, Bank 1, Bank 2, Bank 6, Bank 7	2.375	2.50	2.625	V
		VCCIO = 1.8 V, All Banks	1.71	1.80	1.89	V
		VCCIO = 1.5 V, All Banks	1.425	1.50	1.575	V
		VCCIO = 1.35 V, All Banks (For DDR3L Only)	1.2825	1.35	1.4175	V
		VCCIO = 1.2 V, All Banks	1.14	1.20	1.26	V
		VCCIO = 1.0 V, Bank 3, Bank 4, Bank 5	0.95	1.00	1.05	V
ADC External Power Supplies						
$V_{CCADC18}$	ADC 1.8 V Power Supply	—	1.71	1.80	1.89	V
SerDes Block External Power Supplies						
V_{CCSD*}	Supply Voltage for SerDes Block and SerDes I/O	—	0.95	1.00	1.05	V
V_{CCSDCK}	Supply Voltage for SerDes Clock Buffer	—	0.95	1.00	1.05	V
$V_{CCPLLSD*}$	SerDes Block PLL Supply Voltage	—	1.71	1.80	1.89	V
$V_{CCAUXSDQ}$*	SerDes Block Auxiliary Supply Voltage	—	1.71	1.80	1.89	V
Operating Temperature						
t_{JAUTO}	Junction Temperature, Automotive/Space PEM QD Operation	—	-40	—	125	°C

Notes:

1. For correct operation, all supplies must be held in their valid operation voltage range.
2. All supplies with the same voltage should be from the same voltage source. Proper isolation filters are needed to properly isolate noise from each other.
3. Common supply rails must be tied together except SerDes.
4. MSPI (Bank 0) and JTAG, SSPI, I^2C, and I3C (Bank 1) ports are supported for VCCIO = 1.8 V to 3.3 V.

3.3 Power Supply Ramp Rates

Table 3.3 Power Supply Ramp Rates

Symbol	Parameter	Min	Typ	Max	Unit
t_{RAMP}	Power Supply ramp rates for all supplies 1	0.1	—	50	V/ms

Notes:

1. Assumes monotonic ramp rates.
2. All supplies need to be in the operating range as defined in Recommended Operating Conditions when the device has completed configuration and entering into User Mode. Supplies that are not in the operating range needs to be adjusted to faster ramp rate, or you have to delay configuration or wake up.

3.4 Power up Sequence

Power-On-Reset (POR) puts the CertusPro-NX-RT device into a reset state. There is no power up sequence required for the CertusPro-NX-RT device.

Table 3.4 Power-On Reset

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PORUP}	Power-On-Reset ramp-up trip point (Monitoring V_{CC}, V_{CCAUX}, V_{CCIO0} and V_{CCIO1})	V_{CC}	0.73	—	0.83	V
		V_{CCAUX}	1.34	—	1.71	V
		V_{CCIO0}, V_{CCIO1}	0.89	—	1.05	V
V_{PORDN}	Power-On-Reset ramp-down trip point (Monitoring V_{CC} and VCCAUX)	V_{CC}	0.51	—	0.81	V
		V_{CCAUX}	1.38	—	1.54	V

Note: V_{CCIO0} does not have a Power-On-Reset ramp down detection. V_{CCIO0} must remain within the Recommended Operating Conditions to ensure proper operation.

3.5 On-chip Programmable Termination

The CertusPro-NX-RT devices support a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 50 Ω, 75 Ω, or 150 Ω. Termination to ground for LPDDR4, and termination to VCCIO/2 for all other non-LPDDR4.
- Common mode termination of 100 Ω for differential inputs.

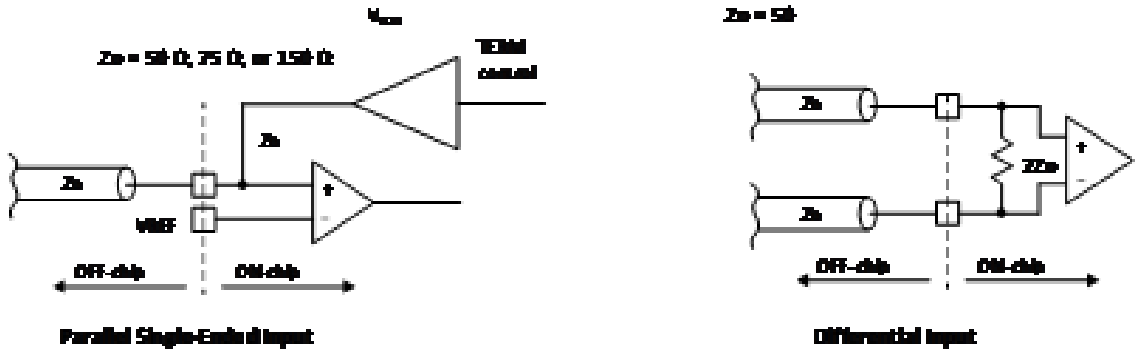


Figure 3.1. On-chip Termination

See Table 3.5 for termination options for input modes.

Table 3.5 On-Chip Termination Options for Input Modes

IO_TYPE	Differential Termination Resistor*	Terminate to VCCIO/2*
subLVDS	100, OFF	OFF
SLVS	100, OFF	OFF
MIPI_DPHY	100	OFF
HSTL15D_I	100, OFF	OFF
SSTL15D_I	100, OFF	OFF
SSTL135D_I	100, OFF	OFF
HSUL12D	100, OFF	OFF
LVSTLD_I	OFF	OFF
LVSTLD_II	OFF	OFF
LVCMOS15H	OFF	OFF
LVCMOS12H	OFF	OFF
LVCMOS10H	OFF	OFF
LVCMOS12H	OFF	OFF
LVCMOS10H	OFF	OFF
LVCMOS18H	OFF	OFF, 40, 50, 60, 75
HSTL15_I	OFF	50
SSTL15_I	OFF	OFF, 40, 50, 60, 75
SSTL135_I	OFF	OFF, 40, 50, 60, 75
HSUL12	OFF	OFF, 40, 50, 60, 75
LVSTL_I	OFF	OFF, 40, 48, 60, 80, 120
LVSTL_II	OFF	OFF, 80, 120

Notes:

1. Single-ended Terminate Resistor (to ground for LPDDR4, to VCCIO/2 for all other non-LPDDR4) and Differential Resistor when turned on can only have one setting per bank. Only left and right banks have this feature.

2. Use of Single-ended Terminate Resistor (to ground for LPDDR4, to VCCIO/2 for all other non-LPDDR4) and Differential Termination Resistor are mutually exclusive in an I/O bank.
3. Tolerance for single-ended termination resistor is -10/60%, while for differential termination resistor is -15/15%.

Refer to sysI/O Usage Guide for Nexus Platform (FPGA-TN-02067) for on-chip termination usage and value ranges.

3.6 Hot Socketing Specifications

Table 3.6 Hot Socketing Specifications for GPIO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DK}	Input or I/O Leakage Current for Wide Range I/O (excluding MCLK/MCSN/MOSI/INITN/DONE)	$0 < V_{IN} < V_{IH}$(max) $0 < V_{CC} < V_{CC}$(max) $0 < V_{CCIO} < V_{CCIO}$(max) $0 < V_{CCAUX} < V_{CCAUX}$(max)	–1.5	—	1.5	mA

Notes:

1. I_{DK} is additive to I_{PU}, I_{PD}, or I_{BH}.
2. Hot socketing specification is defined at a device junction temperature of 85°C or below. When the device junction temperature is above 85 °C, the IDK current can exceed the above specification limit.
3. Going beyond the hot socketing ranges specified here can cause exponentially higher leakage currents and potential reliability issues. A total of 64 mA per 8 I/O should not be exceeded.

3.7 ESD Performance

Refer to the CertusPro-NX-RT Product Family Qualification Summary for complete qualification data, including ESD performance.

3.8 DC Electrical Characteristics

Table 3.7 DC Electrical Characteristics – Wide Range (Over Recommended Operating Conditions)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IL}, I_{IH}[1,3]	Input or I/O Leakage current (Automotive/Space PEM QD)	$0 \le V_{IN} \le V_{CCIO}$	—	—	10	µA
I_{IH}[2]	Input or I/O Leakage current	$V_{CCIO} \le V_{IN} \le V_{IH}$ (max)	—	—	100	µA
I_{PU}	I/O Weak Pull-up Resistor Current	$0 \le V_{IN} \le 0.7 \times V_{CCIO}$	–30	—	–150	µA
I_{PD}	I/O Weak Pull-down Resistor Current	V_{IL} (max) $\le V_{IN} \le V_{CCIO}$	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (max)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7 \times V_{CCIO}$	–30	—	—	µA
I_{BHLO}	Bus hold low Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—	—	150	µA
I_{BHHO}	Bus hold high Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—	—	–150	µA
V_{BHT}	Bus Hold Trip Points	—	V_{IL} (max)	—	V_{IH} (min)	V

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output tri-stated. Bus Maintenance circuits are disabled.
2. The input leakage current IIH is the worst-case input leakage per GPIO when the pad signal is high and also higher than the bank VCCIO. This is considered a mixed mode input.
3. I_{IL}, and I_{IH} characteristics in the first row are tested as part of RLAT. .

Table 3.8 DC Electrical Characteristics – High Speed (Over Recommended Operating Conditions)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IL}, I_{IH}[1,2]	Input or I/O Leakage	$0 \le V_{IN} \le V_{CCIO}$	—	—	10	µA
I_{PU}	I/O Weak Pull-up Resistor Current	$0 \le V_{IN} \le 0.7 \times V_{CCIO}$	–30	—	–150	µA
I_{PD}	I/O Weak Pull-down Resistor Current	V_{IL} (max) $\le V_{IN} \le V_{CCIO}$	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (max)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7 \times V_{CCIO}$	–30	—	—	µA
I_{BHLO}	Bus hold low Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—	—	150	µA
I_{BHHO}	Bus hold high Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—	—	–150	µA
V_{BHT}	Bus Hold Trip Points	—	V_{IL} (max)	—	V_{IH} (min)	V

Note:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output tri-stated. Bus Maintenance circuits are disabled.
2. I_{IL}, and I_{IH} characteristics in the first row are tested as part of RLAT.

Table 3.9 Capacitors – Wide Range (Over Recommended Operating Conditions)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_1[1]	I/O Capacitance[1]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = typ., V_{IO} = 0 to V_{CCIO} + 0.2V	—	6	—	pF
C_2[1]	Dedicated Input Capacitance[1]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = typ., V_{IO} = 0 to V_{CCIO} + 0.2V	—	6	—	pF

Note:

1. TA 25 °C, f = 1.0 MHz.

Table 3.10 Capacitors – High Performance (Over Recommended Operating Conditions)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_1[1]	I/O Capacitance[1]	V_{CCIO} = 1.8 V, 1.5 V, 1.2 V, V_{CC} = typ., V_{IO} = 0 to V_{CCIO} + 0.2V	—	6	—	pF
C_2[1]	Dedicated Input Capacitance[1]	V_{CCIO} = 1.8 V, 1.5 V, 1.2 V, V_{CC} = typ., V_{IO} = 0 to V_{CCIO} + 0.2V	—	6	—	pF
C_3[1]	SerDes I/O Capacitance	V_{CCSD}* = 1.0 V, V_{CC} = typ., V_{IO} = 0 to V_{CCSD}* + 0.2 V	—	5	—	pF

Note:

1. TA 25 °C, f = 1.0 MHz.

Table 3.11 Single Ended Input Hysteresis – Wide Range (Over Recommended Operating Conditions)

IO_TYPE	VCCIO	TYP Hysteresis
LVCMOS33	3.3 V	250 mV
LVCMOS25	3.3 V	200 mV
	2.5 V	250 mV
LVCMOS18	1.8 V	180 mV
LVCMOS15	1.5 V	50 mV
LVCMOS12	1.2 V	0
LVCMOS10	1.2 V	0

Table 3.12 Single Ended Input Hysteresis – High Performance (Over Recommended Operating Conditions)

IO_TYPE	VCCIO	TYP Hysteresis
LVCMOS18H	1.8 V	180 mV
LVCMOS15H	1.8 V	50 mV
	1.5 V	150 mV
LVCMOS12H	1.2 V	0
LVCMOS10H	1.0 V	0
MIPI-LP-RX	1.2 V	>25 mV

3.9 Supply Currents

For estimating and calculating current, use Power Calculator in Lattice Design Software.

This operating and peak current is design dependent, and can be calculated in Lattice Design Software. Some blocks can be placed into low current standby modes. Refer to CertusPro-NX Power Usage Guide (FPGA-TN-02214).

3.10 sysI/O Recommended Operating Conditions

Table 3.13 sysI/O Recommended Operating Conditions

Standard	Support Banks	VCCIO (Input)	VCCIO (Output)
		Typ.	Typ.
Single-Ended			
LVCMOS33	0, 1, 2, 6, 7	3.3	3.3
LVTTL33	0, 1, 2, 6, 7	3.3	3.3
LVCMOS25[1], [2]	0, 1, 2, 6, 7	2.5, 3.3	2.5
LVCMOS18[1], [2]	0, 1, 2, 6, 7	1.2, 1.5, 1.8, 2.5, 3.3	1.8
LVCMOS18H	3, 4, 5	1.8	1.8
LVCMOS15[1], [2]	0, 1, 2, 6, 7	1.2, 1.5, 1.8, 2.5, 3.3	1.5
LVCMOS15H[1]	3, 4, 5	1.5, 1.8	1.5
LVCMOS12[1], [2]	0, 1, 2, 6, 7	1.2, 1.5, 1.8, 2.5, 3.3	1.2
LVCMOS12H[1]	3, 4, 5	1.2, 1.35[7], 1.5, 1.8	1.2
LVCMOS10[1]	0, 1, 2, 6, 7	1.2, 1.5, 1.8, 2.5, 3.3	—
LVCMOS10H[1]	3, 4, 5	1.0, 1.2, 1.35[7], 1.5, 1.8	1.0
LVCMOS10R[1]	3, 4, 5	1.0, 1.2, 1.35[7], 1.5, 1.8	—
SSTL135_I, SSTL135_II[3]	3, 4, 5	1.35[7]	1.35
SSTL15_I, SSTL15_II[3]	3, 4, 5	1.5[8]	1.5[8]
HSTL15_I[3]	3, 4, 5	1.5[8]	1.5[8]
HSUL123	3, 4, 5	1.2	1.2
LVSTL_I, LVSTL_II[3]	3, 4, 5	1.1	1.1
MIPI D-PHY LP Input[6]	3, 4, 5	1.2	1.2
Differential[6]			
LVDS	3, 4, 5	1.2, 1.35, 1.5, 1.8	1.8
LVDSE5	0, 1, 2, 6, 7	—	2.5

Standard	Support Banks	VCCIO (Input)	VCCIO (Output)
		Typ.	Typ.
subLVDS	3, 4, 5	1.2, 1.35, 1.5, 1.8	—
subLVDSE[5]	0, 1, 2, 6, 7	—	1.8
subLVDSEH[5]	3, 4, 5	—	1.8
SLVS[6]	3, 4, 5	1.0, 1.2, 1.35[7], 1.5, 1.8[4]	1.2, 1.35[7], 1.5, 1.8 [4]
MIPI D-PHY[6]	3, 4, 5	1.2	1.2
LVCMOS33D[5]	0, 1, 2, 6, 7	—	3.3
LVTTL33D[5]	0, 1, 2, 6, 7	—	3.3
LVCMOS25D[5]	0, 1, 2, 6, 7	—	2.5
SSTL135D_I, SSTL135D_II[5]	3, 4, 5	—	1.35[7]
SSTL15D_I, SSTL15D_II[5]	3, 4, 5	—	1.5
HSTL15D_I[5]	3, 4, 5	—	1.5
HSUL12D[5]	3, 4, 5	—	1.2
LVSTLD_I, LVSTLD_II[5]	3, 4, 5	—	1.1

Notes:

1. Single-ended input can mix into I/O Banks with VCCIO different from the standard requires due to some of these input standards use internal supply voltage source (VCC, VCCAUX) to power the input buffer, which makes them to be independent of VCCIO voltage. For more details, refer to sysI/O Usage Guide for Nexus Platform (FPGA-TN-02067). The following is a brief guideline to follow:

a) Weak pull-up on the I/O must be set to OFF.

b) Bank 3, Bank 4, and Bank 5 I/O can only mix into banks with VCCIO higher than the pin standard, due to clamping diode on the pin in these banks. Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7 does not have this restriction.

c) LVCMOS25 uses VCCIO supply on input buffer in Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7. It can be supported with VCCIO = 3.3 V to meet the VIH and VIL requirements, but there is additional current drawn on VCCIO. Hysteresis has to be disabled when using 3.3 V supply voltage.

d) LVCMOS15 uses VCCIO supply on input buffer in Bank 3, Bank 4, and Bank 5. It can be supported with VCCIO = 1.8 V to meet the VIH and VIL requirements, but there is additional current drawn on VCCIO.

2. Single-ended LVCMOS inputs can be mixed into I/O Banks with different VCCIO, providing weak pull-up not being used.

   For additional information on Mixed I/O in Bank VCCIO, refer to sysI/O Usage Guide for Nexus Platform (FPGA-TN-02067).

3. These inputs use differential input comparator in Bank 3, Bank 4, and Bank 5. The differential input comparator uses VCCAUXH power supply. These inputs require the VREF pin to provide the reference voltage in the Bank. Refer to sysI/O Usage Guide for Nexus Platform (FPGA-TN-02067) for details.

4. All differential inputs use differential input comparator in Bank 3, Bank 4, and Bank 5. The differential input comparator uses VCCAUXH power supply. There is no differential input signaling supported in Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7.

5. These outputs are emulating differential output pair with single-ended output drivers with true and complement outputs driving on each of the corresponding true and complement output pair pins. The common mode voltage VCM is ½ × VCCIO. Refer to sysI/O Usage Guide for Nexus Platform (FPGA-TN-02067) for details.

6. Soft MIPI D-PHY HS using sysI/O is supported with SLVS input and output that can be placed in banks with VCCIO voltage shown in SLVS. D-PHY with HS and LP modes supported needs to be placed in banks with VCCIO voltage = 1.2 V. Soft MIPI D-PHY LP input and output using sysI/O are supported with LVCMOS12.

7. VCCIO = 1.35 V is only supported in Bank 3, Bank 4, and Bank 5, for use with DDR3L interface in the bank. These Input and Output standards can fit into the same bank with the VCCIO = 1.35 V.

8. LVCMOS15 input uses VCCIO supply voltage. If VCCIO is 1.8 V, the DC levels for LVCMOS15 are still met, but there could be increase in input buffer current.

3.11 sysI/O Single-Ended DC Electrical Characteristics

Table 3.14 sysI/O DC Electrical Characteristics – Wide Range I/O (Over Recommended Operating Conditions)

Input/Output Standard	V_{IL}[1]		V_{IH}[1]		V_{OL} Max (V)	V_{OH} Min[2] (V)	I_{OL} (mA)	I_{OH} (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVTTL33 LVCMOS33 [6]	—	0.8	2.0	3.465[5]	0.4	VCCIO – 0.4	2, 4, 8, 12, 16, “50RS”3	–2, –4, –8, –12, –16, “50RS”3
LVCMOS25	—	0.7	1.7	3.465[5]	0.4	VCCIO – 0.45	2, 4, 8, 10, “50RS”3	–2, –4, –8, –10, “50RS”3
LVCMOS18	—	0.35 × VCCIO	0.65 × VCCIO	3.465[5]	0.4	VCCIO – 0.45	2, 4, 8, “50RS”3	–2, –4, –8, “50RS”3
LVCMOS15	—	0.35 × VCCIO	0.65 × VCCIO	3.465[5]	0.4	VCCIO – 0.4	2, 4	–2, –4
LVCMOS12	—	0.35 × VCCIO	0.65 × VCCIO	3.465[5]	0.4	VCCIO – 0.4	2, 4	–2, –4
LVCMOS10	—	0.35 × VCCIO	0.65 × VCCIO	3.465[5]	No O/P Support			

Notes:

1. VCCIO for input level refers to the supply rail level associated with a given input standard.
2. VCCIO for the output levels refer to the VCCIO of the CertusPro-NX-RT device.
3. Selecting “50RS” in driver strength is to select 50 Ω series impedance driver.
4. For electro-migration, the combined DC current sourced or sinked by I/O pads between two consecutive VCCIO or GND pad connections, or between the last VCCIO or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed a maximum of n × 8 mA. n is the number of I/O pads between the two consecutive bank VCCIO or GND connections or between the last VCCIO and GND in a bank and the end of a bank. I/O Grouping can be found in the Data Sheet Pin Summary Tables, which can also be generated from the Lattice Radiant software.
5. If the input clamp is OFF, VIH (Max) in Banks 0, 1, 2, 6, and 7 can go up to 3.465 V. Otherwise, the input voltage cannot be higher than VCCIO + 0.3 V.
6. LVTTL33/LVCMOS33 characteristics in the first row are tested as part of RLAT: V_{IL}, V_{IH}, V_{OL} @ 12mA only, V_{OH} @ -12mA only.

Table 3.15 sysI/O DC Electrical Characteristics – High Performance I/O (Over Recommended Operating Conditions)

Input/Output Standard	V_{IL}[1]		V_{IH}[1]		V_{OL} Max (V)	V_{OH} Min[2] (V)	I_{OL} (mA)	I_{OH} (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS18H [5]	—	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.4	V_{CCIO} – 0.45	2, 4, 8, 12, "50RS"[3]	–2, –4, –8, –12, "50RS"[3]
LVCMOS15H	—	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.4	V_{CCIO} – 0.4	2, 4, 8, "50RS"[3]	–2, –4, –8, "50RS"[3]
LVCMOS12H	—	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.4	V_{CCIO} – 0.4	2, 4, 8, "50RS"[3]	–2, –4, –8, "50RS"[3]
LVCMOS10H	—	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.27 × V_{CCIO}	0.75 × V_{CCIO}	2, 4	–2, –4
SSTL15_I	—	V_{REF} – 0.10	V_{REF} + 0.1	V_{CCIO} + 0.3	0.30	V_{CCIO} – 0.30	7.5	–7.5
SSTL15_II	—	V_{REF} – 0.10	V_{REF} + 0.1	V_{CCIO} + 0.3	0.30	V_{CCIO} – 0.30	8.8	–8.8
HSTL15_I	—	V_{REF} – 0.10	V_{REF} + 0.1	V_{CCIO} + 0.3	0.40	V_{CCIO} – 0.40	8	–8
SSTL135_I	—	V_{REF} – 0.09	V_{REF} + 0.09	V_{CCIO} + 0.3	0.27	V_{CCIO} – 0.27	6.75	–6.75
SSTL135_II	—	V_{REF} – 0.09	V_{REF} + 0.09	V_{CCIO} + 0.3	0.27	V_{CCIO} – 0.27	8	–8
LVCMOS10R	—	V_{REF} – 0.10	V_{REF} + 0.10	V_{CCIO} + 0.3	—	—	—	—
HSUL12	—	V_{REF} – 0.10	V_{REF} + 0.10	V_{CCIO} + 0.3	0.3	V_{CCIO} – 0.3	8.0, 7.5, 6.25, 5	–8.0, –7.5, –6.25, –5
LVSTL_I	–0.2	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.2	0.1 × V_{CCIO}	0.3 × V_{CCIO}	2, 4, 6, 8, 10	–2, –4, –6, –8, –10
LVSTL_II	–0.2	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.2	0.1 × V_{CCIO}	0.36 × V_{CCIO}	4, 6	–4, –6

Notes:

1. VCCIO for input level refers to the supply rail level associated with a given input standard.
2. VCCIO for the output levels refer to the VCCIO of the CertusPro-NX-RT device.
3. Select "50RS" in driver strength is selecting the 50Ω series impedance driver.
4. For electro-migration, the combined DC current sourced or sinked by I/O pads between two consecutive VCCIO or GND pad connections, or between the last VCCIO or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed a maximum of n × 8 mA. n is the number of I/O pads between the two consecutive bank VCCIO or GND connections or between the last VCCIO and GND in a bank and the end of a bank. I/O Grouping can be found in the Data Sheet Pin Summary Tables, which can also be generated from the Lattice Radiant software.
5. LVCMOS18H characteristics in the first row are tested as part of RLAT: V_{IL}, V_{IH}, V_{OL} @ 12mA only, V_{OH} @ -12mA only.

Table 3.16 I/O Resistance Characteristics (Over Recommended Operating Conditions)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
50RS	Output Drive Resistance when 50RS Drive Strength Selected	V_{CCIO} = 1.8 V, 2.5 V, or 3.3 V	—	50	—	Ω
R_{DIFF}	Input Differential Termination Resistance	Bank 3, Bank 4, and Bank 5, for I/O selected to be differential	—	100	—	Ω
SE Input Termination	Input Single Ended Termination Resistance	Bank 3, Bank 4, and Bank 5 for I/O selected to be Single Ended	36	40	64	Ω
			46	50	80	
			56	60	96	
			71	75	120	

Table 3.17 VIN Maximum Overshoot/Undershoot Allowance – Wide Range1,2

AC Voltage Overshoot	% of UI at –40 °C to 125 °C	AC Voltage Undershoot	% of UI at –40 °C to 125 °C
V_{CCIO} + 0.4	100.0%	–0.4	100.0%
V_{CCIO} + 0.5	100.0%	–0.5	44.2%
V_{CCIO} + 0.6	94.0%	–0.6	10.1%
V_{CCIO} + 0.7	21.0%	–0.7	1.3%
V_{CCIO} + 0.8	10.2%	–0.8	0.3%
V_{CCIO} + 0.9	2.5%	–0.9	0.1%

Notes:

1. The peak overshoot or undershoot voltage and the duration above VCCIO + 0.2 V or below GND – 0.2 V must not exceed the values in this table.
2. For UI less than 20 µs.

Table 3.18 VIN Maximum Overshoot/Undershoot Allowance – High Performance[1,2]

AC Voltage Overshoot	% of UI at –40 °C to 125 °C	AC Voltage Undershoot	% of UI at –40 °C to 125 °C
VCCIO + 0.5	100.0%	–0.5	100.0%
VCCIO + 0.6	47.3%	–0.6	47.3%
VCCIO + 0.7	10.9%	–0.7	10.9%
VCCIO + 0.8	2.7%	–0.8	2.7%
VCCIO + 0.9	0.7%	–0.9	0.7%

Notes:

1. The peak overshoot or undershoot voltage and the duration above VCCIO + 0.2 V or below GND – 0.2 V must not exceed the values in this table.
2. For UI less than 20 µs.

3.12 sysI/O Differential DC Electrical Characteristics

3.12.1 LVDS

LVDS input buffer on CertusPro-NX-RT device is operating with VCCAUX = 1.8 V, and the LVDS input voltage cannot exceed the VCCIO voltage of the related bank. LVDS output buffer is powered by the Bank VCCIO at 1.8 V.

LVDS can only be supported in Bank 3, Bank 4, and Bank 5. LVDS25 output can be emulated with LVDS25E in Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7. This is described in the 3.12.2 LVDS25E (Output Only) section.

Table 3.19 LVDS DC Electrical Characteristics (Over Recommended Operating Conditions)1

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{INP}, V_{INM}	Input Voltage	—	0	—	1.60[3]	V
V_{ICM}	Input Common Mode Voltage	Half the sum of the two Inputs	0.05	—	1.55[2]	V
V_{THD}	Differential Input Threshold	Difference between the two Inputs	±100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	±10	µA
V_{OH}	Output High Voltage for VOP or VOM	RT = 100 Ω	—	1.425	1.60	V
V_{OL}	Output Low Voltage for VOP or VOM	RT = 100 Ω	0.9 V	1.075	—	V
V_{OD}	Output Voltage Differential	(V_{OP} – V_{OM}), RT = 100 Ω	250	350	450	mV
ΔV_{OD}	Change in VOD Between High and Low	—	—	—	50	mV
V_{OCM}	Output Common Mode Voltage	(V_{OP} + V_{OM})/2, RT = 100 Ω	1.125	1.25	1.375	V
ΔV_{OCM}	Change in VOCM, VOCM(Max) – VOCM(Min)	—	—	—	50	mV
I_{SAB}	Output Short Circuit Current	V_{OD} = 0 V Driver outputs shorted to each other	—	—	12	mA
ΔV_{OS}	Change in V_{OS} between H and L	—	—	—	50	mV

Notes:

1. LVDS input or output are supported in Bank 3, Bank 4, and Bank 5. LVDS input uses VCCAUXH on the differential input comparator, and can be located in any VCCIO voltage bank. LVDS output uses VCCIO on the differential output driver, and can only be located in bank with VCCIO = 1.8 V.
2. VICM is depending on VID, input differential voltage, so the voltage on pin cannot exceed VINP/INM(Min/Max) requirements. VICM(Min) = VINP/INM(Min) + ½VID, VICM(Max) = VINP/INM(Max) – ½VID. Values in the table is based on minimum VID of +/- 100 mV.
3. VINP/INM(Max) must be less than or equal to VCCIO in all cases.

3.12.2 LVDS25E (Output Only)

Three sides of the CertusPro-NX-RT devices, Top, Left and Right, support LVDS25 outputs with emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3.2 is one possible solution for point-to-point signals.

Table 3.20 LVDS25E DC Conditions

Parameter	Description	Typical	Unit
VCCIO	Output Driver Supply (±5%)	2.50	V
ZOUT	Driver Impedance	20	Ω
RS	Driver Series Resistor (±1%)	158	Ω
RP	Driver Parallel Resistor (±1%)	140	Ω
RT	Receiver Termination (±1%)	100	Ω
VOH	Output High Voltage	1.43	V
VOL	Output Low Voltage	1.07	V
VOD	Output Differential Voltage	0.35	V
VCM	Output Common Mode Voltage	1.25	V
ZBACK	Back Impedance	100.5	Ω
IDC	DC Output Current	–6.03	mA

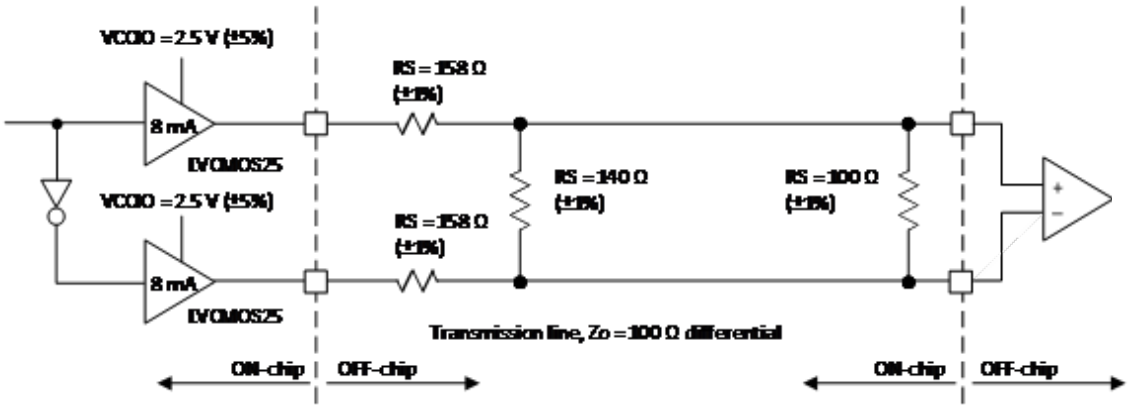


Figure 3.2. LVDS25E Output Termination Example

3.12.3 SubLVDS (Input Only)

SubLVDS is a reduced-voltage form of LVDS signaling, very similar to LVDS (Figure 3.3). It is a standard used in many camera types of applications, and follow the SMIA 1.0, Part 2: CCP2 Specification. Similar to LVDS, the CertusPro-NX-RT devices can support the subLVDS input signaling with the same LVDS input buffer, and the subLVDS input voltage cannot exceed the VCCIO voltage of the related bank. The output for subLVDS is implemented in subLVDSE/subLVDSEH with a pair of LVCMOS18 output drivers. See the SubLVDSE/SubLVDSEH (Output Only) section, for more details.

Table 3.21 1SubLVDS Input DC Electrical Characteristics (Over Recommended Operating Conditions)

Parameter	Description	Test Conditions	Min	Typ	Max1	Unit
V_{ID}	Input Differential Threshold Voltage	Over V_{ICM} range	70	150	200	mV
V_{ICM}	Input Common Mode Voltage	Half the sum of the two Inputs	0.4	0.9	1.4	V

Note:

1. VICM+½VID cannot exceed the bank VCCIO in all cases.

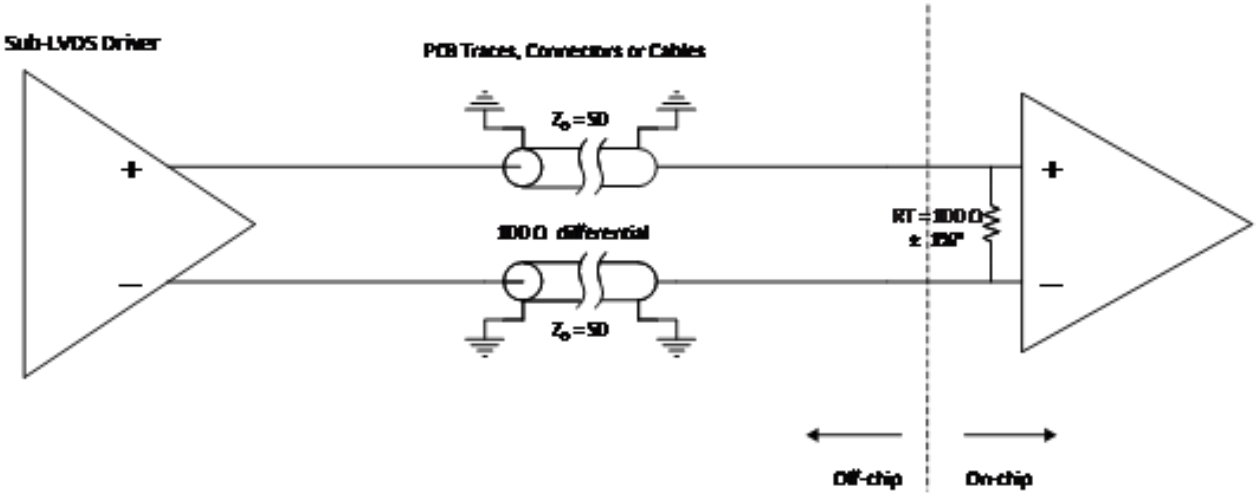


Figure 3.3. SubLVDS Input Interface

3.12.4 SubLVDSE/SubLVDSEH (Output Only)

SubLVDS output uses a pair of LVCMOS18 drivers with True and Complement outputs (Figure 3.4). VCCIO of the bank used for subLVDSE or subLVDSEH needs to be powered by 1.8 V. SubLVDSE is for Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7; and subLVDSEH is for Bank 3, Bank 4, and Bank 5.

Performance of the subLVDSE/subLVDSEH driver is limited to the performance of LVCMOS18.

Table 3.22 SubLVDS Output DC Electrical Characteristics (Over Recommended Operating Conditions)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{OD}	Output Differential Voltage Swing	—	—	150	—	mV
V_{OCM}	Output Common Mode Voltage	Half the sum of the two Outputs	—	0.9	—	V

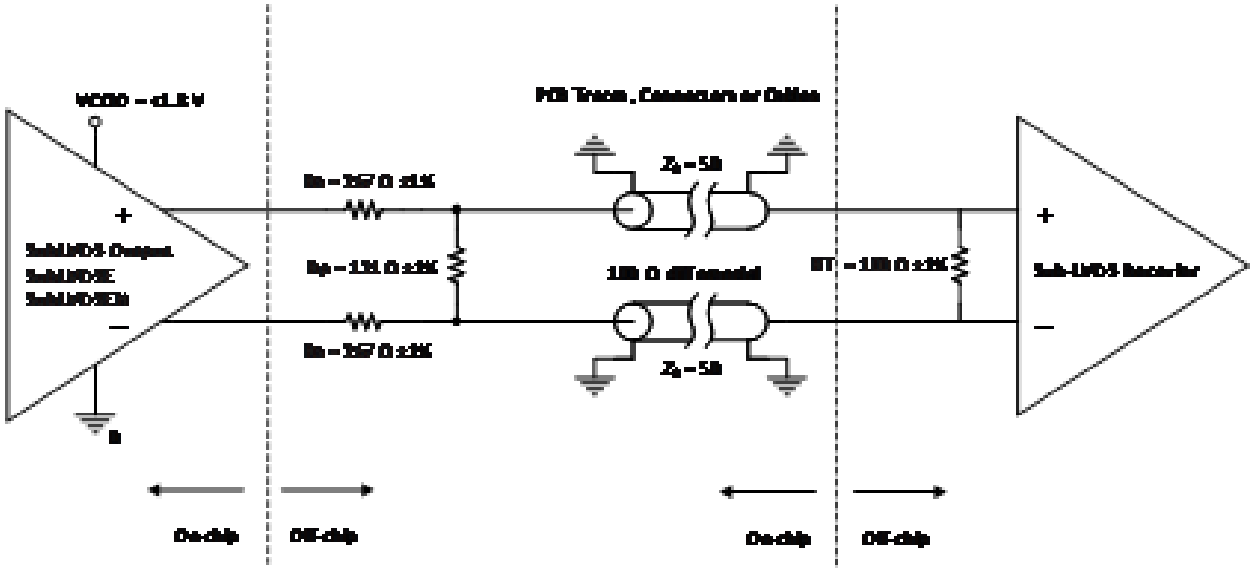


Figure 3.4. SubLVDS Output Interface

3.12.5 SLVS

Scalable Low-Voltage Signaling (SLVS) is based on a point-to-point signaling method defined in the JEDEC JESD8-13 (SLVS-400) standard. This standard evolved from the traditional LVDS standard with smaller voltage swings and a lower common-mode voltage. The 200 mV (400 mV p-p) SLVS swing contributes to a reduction in power.

The CertusPro-NX-RT devices receive SLVS differential input with the LVDS input buffer (Table 3.23). This LVDS input buffer is design to cover wide input common mode range that can meet the SLVS input standard specified by the JEDEC standard.

Table 3.23 SLVS Input DC Characteristics (Over Recommended Operating Conditions)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{ID}	Input Differential Threshold Voltage	Over VICM range	70	—	—	mV
V_{ICM}	Input Common Mode Voltage	Half the sum of the two Inputs	70	200	330	mV

The SLVS output on the CertusPro-NX-RT device is supported with the LVDS drivers found in Bank 3, Bank 4, and Bank 5. The LVDS driver on the CertusPro-NX-RT device is a current controlled driver (Figure 3.5). It can be configured as LVDS driver, or configured with the 100 Ω differential termination with center-tap set to VOCM at 200 mV. This means the differential output driver can be placed into bank with VCCIO = 1.2 V, 1.5 V, or 1.8 V, even if it is powered by VCCIO. See Table 3.24 for more details.

Table 3.24 SLVS Output DC Characteristics (Over Recommended Operating Conditions)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{CCIO}	Bank V_{CCIO}	—	–5%	1.2, 1.5, 1.8	+ 5%	V
V_{OD}	Output Differential Voltage Swing	—	140	200	270	mV
V_{OCM}	Output Common Mode Voltage	Half the sum of the two Outputs	150	200	250	mV
Z_{OS}	Single-Ended Output Impedance	—	37.5	50	62.5	Ω

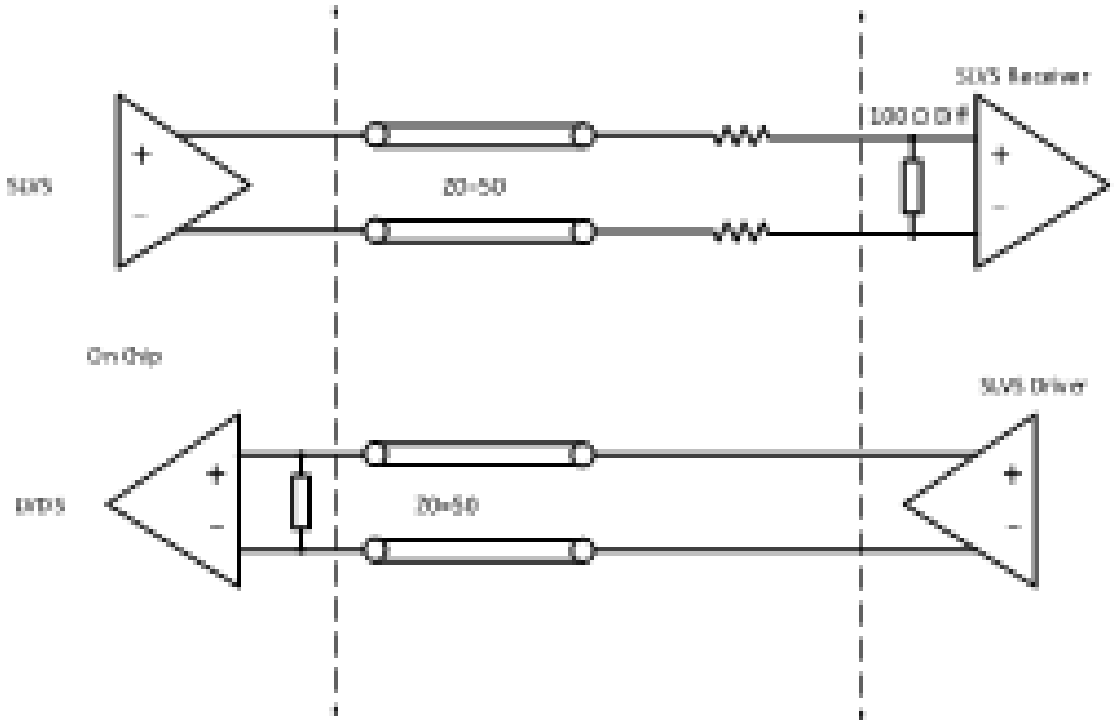


Figure 3.5. SLVS Interface

3.12.6 Soft MIPI D-PHY

When Soft D-PHY is implemented inside the FPGA logic, the I/O interface needs to use sysI/O buffers to connect to external D-PHY pins.

The CertusPro-NX-RT sysI/O provides support for SLVS, as described in SLVS section, plus the LVCMOS12 input/output buffers together to support the High Speed (HS) and Low Power (LP) modes as defined in MIPI Alliance Specification for D-PHY.

To support MIPI D-PHY with SLVS (LVDS) and LVCMOS12, the bank VCCIO cannot be set to 1.5 V or 1.8 V. It has to connect to 1.2 V, or 1.1 V (Figure 3.6).

All other DC parameters are the same as listed in SLVS section. DC parameters for the LP driver and receiver are the same as listed in LVCMOS12.

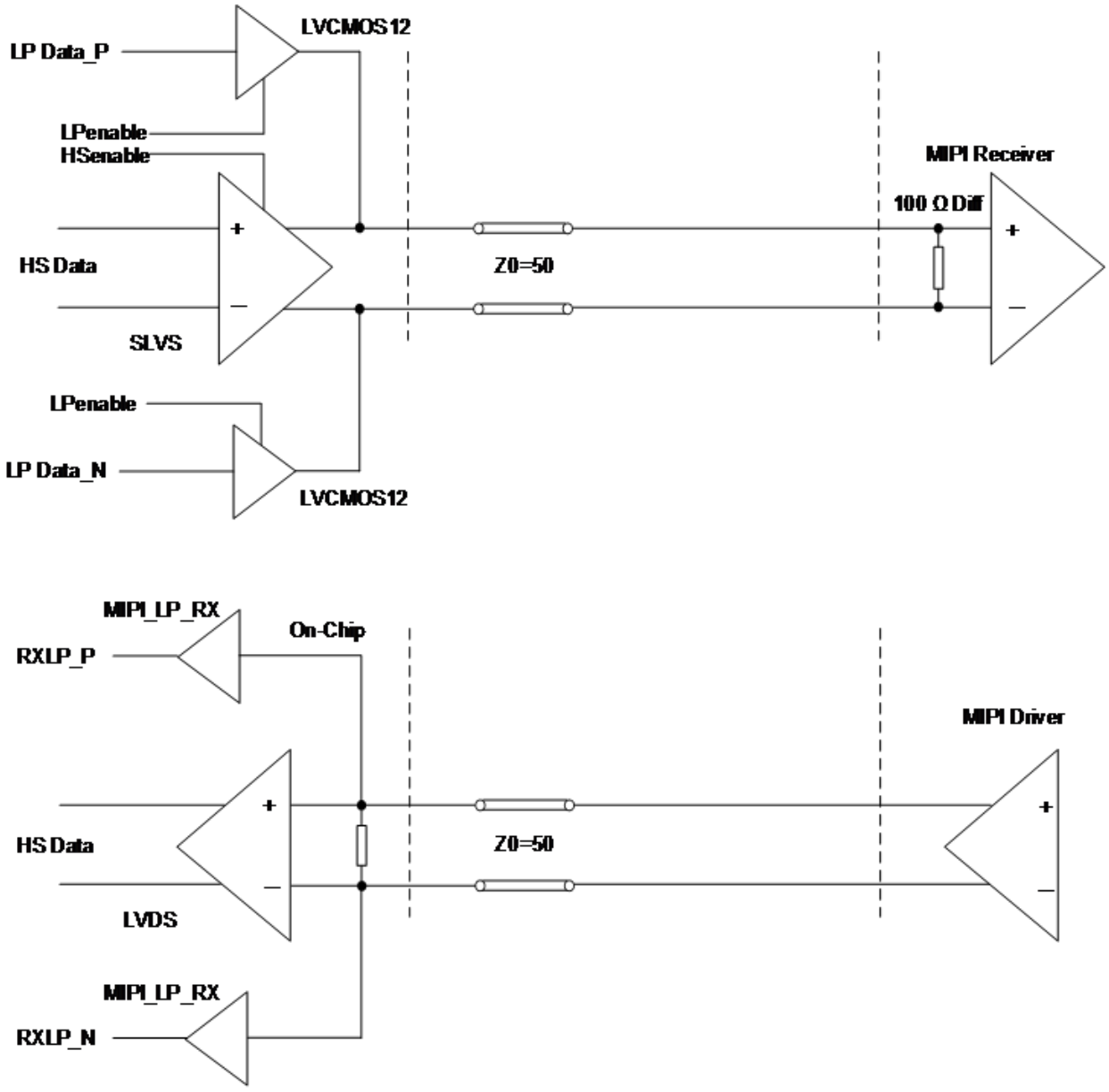


Figure 3.6. MIPI Interface

Table 3.25 Soft D-PHY Input Timing and Levels

Symbol	Description	Conditions	Min	Typ	Max	Unit
High Speed (Differential) Input DC Specifications						
$V_{CMRX(DC)}$	Common-mode Voltage in High Speed Mode	—	70	—	330	mV
V_{IDTH}	Differential Input HIGH Threshold	—	70	—	—	mV
V_{IDTL}	Differential Input LOW Threshold	—	—	—	–70	mV
V_{IHHS}	Input HIGH Voltage (for HS mode)	—	—	—	460	mV
V_{ILHS}	Input LOW Voltage	—	–40	—	—	mV
$V_{TERM-EN}$	Single-ended voltage for HS Termination Enable[4]	—	—	—	450	mV
Z_{ID}	Differential Input Impedance	—	80	100	125	Ω
High Speed (Differential) Input AC Specifications						
$\Delta V_{CMRX(HF)}$[1]	Common-mode Interference (>450 MHz)	—	—	—	100	mV
$\Delta V_{CMRX(LF)}$[2, 3]	Common-mode Interference (50 MHz - 450 MHz)	—	–50	—	50	mV
C_{CM}	Common-mode Termination	—			60	pF
Low Power (Single-Ended) Input DC Specifications						
V_{IH}	Low Power Mode Input HIGH Voltage	—	820	—	—	mV
V_{IL}	Low Power Mode Input LOW Voltage	—	—	—	480	mV
V_{IL-ULP}	Ultra Low Power Input LOW Voltage	—	—	—	300	mV
V_{HYST}	Low Power Mode Input Hysteresis	—	25	—	—	mV
e_{SPIKE}	Input Pulse Rejection	—	—	—	300	V·ps
T_{MIN-RX}	Minimum Pulse Width Response	—	20	—	—	ns
V_{INT}	Peak Interference Amplitude	—	—	—	200	mV
f_{INT}	Interference Frequency	—	450	—	—	MHz

Notes:

1. This is peak amplitude of sine wave modulated to the receiver inputs.
2. Input common-mode voltage difference compared to average common-mode voltage on the receiver inputs.
3. Exclude any static ground shift of 50 mV.
4. High Speed Differential RTERM is enabled when both DP and DN are below this voltage.

Table 3.26 Soft D-PHY Output Timing and Levels

Symbol	Description	Conditions	Min	Typ	Max	Unit
High Speed (Differential) Output DC Specifications						
V_{CMTX}	Common-mode Voltage in High Speed Mode	—	150	200	250	mV
$\lvert\Delta V_{CMTX(1,0)}\rvert$	VCMTX Mismatch Between Differential HIGH and LOW	—	—	—	7	mV
$\lvert V_{OD}\rvert$	Output Differential Voltage	|D-PHY-P – D-PHY-N|	130	200	270	mV
$\lvert\Delta V_{OD}\rvert$	VOD Mismatch Between Differential HIGH and LOW	—	—	—	56	mV
V_{OHHS}	Single-Ended Output HIGH Voltage	—	—	—	435	mV
Z_{OS}	Single Ended Output Impedance	—	37.5	50	80	Ω
ΔZ_{OS}	ZOS mismatch	—	—	—	20	%
High Speed (Differential) Output AC Specifications						
$\Delta VC_{MTX(LF)}$	Common-Mode Variation, 50 MHz – 450 MHz	—	—	—	25	mVRMS
$\Delta V_{CMTX(HF)}$	Common-Mode Variation, above 450 MHz	—	—	—	15	mVRMS
t_R	Output 20% - 80% Rise Time	0.08 Gbps ≤ t_R ≤ 1.00 Gbps	—	—	0.30	UI
t_F	Output 80% - 20% Fall Time	0.08 Gbps ≤ t_F ≤ 1.00 Gbps	—	—	0.45	UI
Low Power (Single-Ended) Output DC Specifications						
V_{OH}	Low Power Mode Output HIGH Voltage	0.08 Gbps – 1.5 Gbps	1.07	1.2	1.3	V
V_{OL}	Low Power Mode Input LOW Voltage	—	–50	—	50	mV
Z_{OLP}	Output Impedance in Low Power Mode	—	110	—	—	Ω
Low Power (Single-Ended) Output AC Specifications						
t_{RLP}	15% - 85% Rise Time	—	—	—	25	ns
t_{FLP}	85% - 15% Fall Time	—	—	—	25	ns
t_{REOT}	HS – LP Mode Rise and Fall Time, 30% - 85%	—	—	—	35	ns
$T_{LP-PULSE-TX}$	Pulse Width of the LP Exclusive-OR Clock	First LP XOR clock pulse after STOP state or Last pulse before STOP state	40	—	—	ns
		All other pulses	20	—	—	ns
$T_{LP-PER-TX}$	Period of the LP Exclusive-OR Clock	—	90	—	—	ns
C_{LOAD}	Load Capacitance	—	0	—	70	pF

Table 3.27 Soft D-PHY Clock Signal Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
Clock Signal Specification						
UI Instantaneous	UI_{INST}	—	—	—	12.5	ns
UI Variation	ΔUI	UI ≥ 1 ns	–10%	—	10%	UI
		0.667 ns < UI < 1 ns	–5%	—	5%	UI

Table 3.28 Soft D-PHY Data-Clock Timing Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
Data-Clock Timing Specifications						
$T_{SKEW[TX]}$	Data to Clock Skew	0.08 Gbps ≤ TSKEW[TX] ≤ 1.00 Gbps	–0.15	—	0.15	UI_{INST}
$T_{SETUP[RX]}$	Input Data Setup Before CLK	0.08 Gbps ≤ TSETUP[RX] ≤ 1.00 Gbps	0.24	—	—	UI
$T_{HOLD[RX]}$	Input Data Hold After CLK	0.08 Gbps ≤ THOLD[RX] ≤ 1.00 Gbps	0.23	—	—	UI

3.12.7 Differential HSTL15D (Output Only)

Differential HSTL outputs are implemented as a pair of complementary single-ended HSTL outputs.

3.12.8 Differential SSTL135D, SSTL15D (Output Only)

Differential SSTL is used for differential clock in DDR3/DDR3L memory interface. All differential SSTL outputs are implemented as a pair of complementary single-ended SSTL outputs. All allowable single-ended output classes (class I and class II) are supported.

3.12.9 Differential HSUL12D (Output Only)

Differential HSUL is used for differential clock in LPDDR2/LPDDR3 memory interface. All differential HSUL outputs are implemented as a pair of complementary single-ended HSUL12 outputs. All allowable single-ended drive strengths are supported.

3.12.10 Differential LVSTLD (Output Only)

Differential LVSTL is used for differential clock in LPDDR4 memory interface. All differential LVSTL outputs are implemented as a pair of complementary single-ended LVSTL outputs. All allowable single-ended drive strengths are supported.

3.12.11 Differential LVCMOS25D, LVCMOS33D, LVTTL33D (Output Only)

Differential LVCMOS and LVTTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output drive strengths are supported.

3.13 Maximum sysI/O Buffer Speed

Over recommended operating conditions.

Table 3.29 Maximum I/O Buffer Speed1, 2, 3, 4, 7

Buffer	Description	Banks	Max	Unit
Maximum sysI/O Input Frequency				
Single-Ended				
LVCMOS33	LVCMOS33, V_{CCIO} = 3.3 V	0, 1, 2, 6, 7	200	MHz
LVTTL33	LVTTL33, V_{CCIO} = 3.3 V	0, 1, 2, 6, 7	200	MHz
LVCMOS25	LVCMOS25, V_{CCIO} = 2.5 V	0, 1, 2, 6, 7	200	MHz
LVCMOS18[5]	LVCMOS18, V_{CCIO} = 1.8 V	0, 1, 2, 6, 7	200	MHz
LVCMOS18H	LVCMOS18, V_{CCIO} = 1.8 V	3, 4, 5	200	MHz
LVCMOS15[5]	LVCMOS15, V_{CCIO} = 1.5 V	0, 1, 2, 6, 7	100	MHz
LVCMOS15H [5]	LVCMOS15, V_{CCIO} = 1.5 V	3, 4, 5	150	MHz
LVCMOS12 [5]	LVCMOS12, V_{CCIO} = 1.2 V	0, 1, 2, 6, 7	50	MHz
LVCMOS12H [5]	LVCMOS12, V_{CCIO} = 1.2 V	3, 4, 5	100	MHz
LVCMOS10 [5]	LVCMOS 1.0, V_{CCIO} = 1.2 V	0, 1, 2, 6, 7	50	MHz
LVCMOS10H [5]	LVCMOS 1.0, V_{CCIO} = 1.0 V	3, 4, 5	50	MHz
LVCMOS10R	LVCMOS 1.0, V_{CCIO} independent	3, 4, 5	50	MHz
SSTL15_I, SSTL15_II	SSTL_15, V_{CCIO} = 1.5 V	3, 4, 5	1066	Mbps
SSTL135_I, SSTL135_II	SSTL_135, V_{CCIO} = 1.35 V	3, 4, 5	1066	Mbps
LVSTL_I, LVSTL_II	LVSTL, V_{CCIO} = 1.1 V	3, 4, 5	1066	Mbps
HSUL12	HSUL_12, V_{CCIO} = 1.2 V	3, 4, 5	1066	Mbps
HSTL15	HSTL15, V_{CCIO} = 1.5 V	3, 4, 5	250	Mbps
MIPI D-PHY (LP Mode)	MIPI, Low Power Mode, V_{CCIO} = 1.2 V	3, 4, 5	10	Mbps
Differential				
LVDS	LVDS, V_{CCIO} independent, Wire Bond package	3, 4, 5	1250	Mbps
subLVDS	subLVDS, V_{CCIO} independent, Wire Bond package	3, 4, 5	1250	Mbps
SLVS	SLVS similar to MIPI HS, V_{CCIO} independent Wire Bond package	3, 4, 5	1250	Mbps
MIPI D-PHY (HS Mode)	MIPI, High Speed Mode, V_{CCIO} = 1.2 V[3] Wire Bond package	3, 4, 5	1250	Mbps
SSTL15D	Differential SSTL15, V_{CCIO} independent	3, 4, 5	1066	Mbps
SSTL135D	Differential SSTL135, V_{CCIO} independent	3, 4, 5	1066	Mbps

Buffer	Description	Banks	Max	Unit
LVSTLD_I, LVSTLD_II	Differential LVSTL, V_{CCIO} independent	3, 4, 5	1066	Mbps
HUSL12D	Differential HSUL12, V_{CCIO} independent	3, 4, 5	1066	Mbps
HSTL15D	Differential HSTL15, V_{CCIO} independent	3, 4, 5	250	Mbps
Maximum sysI/O Output Frequency				
Single-Ended				
LVCMOS33 (all drive strengths)	LVCMOS33, V_{CCIO} = 3.3 V	0, 1, 2, 6, 7	200	MHz
LVCMOS33 (RS50)	LVCMOS33, V_{CCIO} = 3.3 V, RSERIES = 50 Ω	0, 1, 2, 6, 7	200	MHz
LVTTL33 (all drive strengths)	LVTTL33, V_{CCIO} = 3.3 V	0, 1, 2, 6, 7	200	MHz
LVTTL33 (RS50)	LVTTL33, V_{CCIO} = 3.3 V, RSERIES = 50 Ω	0, 1, 2, 6, 7	200	MHz
LVCMOS25 (all drive strengths)	LVCMOS25, V_{CCIO} = 2.5 V	0, 1, 2, 6, 7	200	MHz
LVCMOS25 (RS50)	LVCMOS25, V_{CCIO} = 2.5 V, RSERIES = 50 Ω	0, 1, 2, 6, 7	200	MHz
LVCMOS18 (all drive strengths)	LVCMOS18, V_{CCIO} = 1.8 V	0, 1, 2, 6, 7	200	MHz
LVCMOS18 (RS50)	LVCMOS18, V_{CCIO} = 1.8 V, RSERIES = 50 Ω	0, 1, 2, 6, 7	200	MHz
LVCMOS18H (all drive strengths)	LVCMOS18, V_{CCIO} = 1.8 V	3, 4, 5	200	MHz
LVCMOS18H (RS50)	LVCMOS18, V_{CCIO} = 1.8 V, RSERIES = 50 Ω	3, 4, 5	200	MHz
LVCMOS15 (all drive strengths)	LVCMOS15, V_{CCIO} = 1.5 V	0, 1, 2, 6, 7	100	MHz
LVCMOS15H (all drive strengths)	LVCMOS15, V_{CCIO} = 1.5 V	3, 4, 5	150	MHz
LVCMOS12 (all drive strengths)	LVCMOS12, V_{CCIO} = 1.2 V	0, 1, 2, 6, 7	50	MHz
LVCMOS12H (all drive strengths)	LVCMOS12, V_{CCIO} = 1.2 V	3, 4, 5	100	MHz
LVCMOS10H (all drive strengths)	LVCMOS12, V_{CCIO} = 1.2 V	3, 4, 5	50	MHz
SSTL15_I, SSTL15_II	SSTL_15, V_{CCIO} = 1.5 V	3, 4, 5	1066	Mbps
SSTL135_I, SSTL135_II	SSTL_135, V_{CCIO} = 1.35 V	3, 4, 5	1066	Mbps
LVSTL_I, LVSTL_II	LVSTL, V_{CCIO} = 1.1 V	3, 4, 5	1066	Mbps
HSUL12 (all drive strengths)	HSUL_12, V_{CCIO} = 1.2 V	3, 4, 5	1066	Mbps
HSTL15	HSTL15, V_{CCIO} = 1.5 V	3, 4, 5	250	Mbps
MIPI D-PHY (LP Mode)	MIPI, Low Power Mode, V_{CCIO} = 1.2 V	3, 4, 5	10	Mbps
Differential				
LVDS	LVDS, V_{CCIO} = 1.8 V Wire Bond package	3, 4, 5	1250	Mbps
LVDS25E[6]	LVDS25, Emulated, V_{CCIO} = 2.5 V	0, 1, 2, 6, 7	400	Mbps
SubLVDSE[6]	subLVDS, Emulated, V_{CCIO} = 1.8 V	0, 1, 2, 6, 7	400	Mbps
SubLVDSEH[6]	subLVDS, Emulated, V_{CCIO} = 1.8 V	3, 4, 5	800	Mbps
SLVS	SLVS similar to MIPI, V_{CCIO} = 1.2 V Wire Bond package	3, 4, 5	1250	Mbps
MIPI D-PHY (HS Mode)	MIPI, High Speed Mode, V_{CCIO} = 1.2 V[3] Wire Bond package	3, 4, 5	1250	Mbps

Buffer	Description	Banks	Max	Unit
SSTL15D	Differential SSTL15, V_{CCIO} = 1.5 V	3, 4, 5	1066	Mbps
SSTL135D	Differential SSTL135, V_{CCIO} = 1.35 V	3, 4, 5	1066	Mbps
LVSTLD	Differential LVSTL, V_{CCIO} = 1.1 V	3, 4, 5	1066	Mbps
HUSL12D	Differential HSUL12, V_{CCIO} = 1.2 V	3, 4, 5	1066	Mbps
HSTL15D	Differential HSTL15, V_{CCIO} = 1.5 V	3, 4, 5	250	Mbps

Notes:

1. Maximum I/O speed is the maximum switching rate of the I/O operating within the guidelines of the defining standard. The actual interface speed performance using the I/O also depends on other factors, such as internal and external timing.
2. These numbers are characterized but not tested on every device.
3. Performance is specified in MHz, as defined in clock rate when the sysI/O is used as pin. For data rate performance, this can be converted to Mbps, which equals to 2 times the clock rate.
4. LVCMOS and LVTTL are measured with load specified in Table 3.50.
5. These LVCMOS inputs can be placed in different VCCIO voltage. Performance may vary. Please refer to Lattice Design software.
6. These emulated outputs performance is based on externally properly terminated as described in the 3.12.2 LVDS25E (Output Only) and SubLVDSE/SubLVDSEH (Output Only) sections.
7. All speeds are measured with fast slew.
8. Subject to verification when package becomes available.

3.14 Typical Building Block Function Performance

Following building block functions (Table 3.30 and Table 3.31) can be generated using Lattice Design Software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.

Table 3.30 Pin-to-Pin Performance

Function	Typ. @ VCC = 1.0 V	Unit
16-bit Decoder (I/O configured with LVCMOS18, Left and Right Banks)	5.5	ns
16-bit Decoder (I/O configured with HSTL15_I, Bottom Banks)	5.1	ns
16:1 Mux (I/O configured with LVCMOS18, Left and Right Banks)	6	ns
16:1 Mux (I/O configured with HSTL15_I, Bottom Banks)	6.1	ns

Note: These functions are generated using Lattice Radiant Design Software. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.

Table 3.31. Register-to-Register Performance [1,3,4]

Function	Typ. @ VCC = 1.0 V	Unit
Basic Functions		
16-bit Adder	500[2]	MHz
32-bit Adder	496	MHz
16-bit Counter	402	MHz
32-bit Counter	371	MHz
Embedded Memory Functions		
512 × 36 Single Port RAM, with Output Register	500[2]	MHz
1024 × 18 True-Dual Port RAM using same clock, with EBR Output Registers	500[2]	MHz
1024 × 18 True-Dual Port RAM using asynchronous clocks, with EBR Output Registers	500[2]	MHz
Large Memory Functions		
32 k × 32 Single Port RAM, with Output Register	375	MHz
32 k × 32 Single Port RAM with ECC, with Output Register	350	MHz
32 k × 32 True-Dual Port RAM using same clock, with Output Registers	200	MHz
Distributed Memory Functions		
16 × 4 Single Port RAM (One PFU)	500[2]	MHz
16 × 2 Pseudo-Dual Port RAM (One PFU)	500[2]	MHz
16 × 4 Pseudo-Dual Port (Two PFUs)	500[2]	MHz
DSP Functions		
9 × 9 Multiplier with Input/Output Registers	340	MHz
18 × 18 Multiplier with Input/Output Registers	260	MHz
36 × 36 Multiplier with Input/Output Registers	184	MHz
MAC 18 × 18 with Input/Output Registers	189	MHz
MAC 18 × 18 with Input/Pipelined/Output Registers	260	MHz
MAC 36 × 36 with Input/Output Registers	111	MHz
MAC 36 × 36 with Input/Pipelined/Output Registers	145	MHz

Notes:

1. The Clock port is configured with LVDS I/O type. Performance Grade: 8_High-Performance_1.0V.
2. Limited by the Minimum Pulse Width of the component
3. These functions are generated using Lattice Radiant design software. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.
4. For the Pipelined designs, the number of pipeline stages used are 2.

3.15 Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Lattice Radiant design software are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process can be much better than the values given in the tables. The Lattice Radiant design software can provide logic timing numbers at a particular temperature and voltage.

3.16 External Switching Characteristics

Over recommended Lattice Automotive/ Frontgrade Space PEM QD operating conditions.

Table 3.32 External Switching Characteristics (VCC = 1.0 V)

Parameter	Description	–8		Unit
		Min	Max	
Clocks				
Primary Clock				
f_{MAX_PRI}	Frequency for Primary Clock	—	325.2	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	1.325	—	ns
t_{SKEW_PRI5}	Primary Clock Skew Within a Device	—	554	ps
Edge Clock				
f_{MAX_EDGE}	Frequency for Edge Clock Tree	—	650.4	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	0.65	—	ns
t_{SKEW_EDGE5}	Edge Clock Skew Within a Device	—	148	ps
Generic SDR Input				
General I/O Pin Parameters Using Dedicated Primary Clock Input without PLL				
t_{CO}	Clock to Output - PIO Output Register	—	8.76	
t_{SU}	Clock to Data Setup - PIO Input Register	0	—	ns
t_{H} (LTR)	Clock to Data Hold - PIO Input Register	4.01	—	ns
t_{H} (Bottom)	Clock to Data Hold - PIO Input Register	4.92	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	1.86	—	ns
t_{H_DEL}(LTR)	Clock to Data Hold - PIO Input Register with Data Input Delay	0.27	—	ns
t_{H_DEL}(Bottom)	Clock to Data Hold - PIO Input Register with Data Input Delay	1.86	—	ns
General I/O Pin Parameters Using Dedicated Primary Clock Input with PLL				
t_{COPLL}	Clock to Output - PIO Output Register	—	4.72	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	1.41	—	ns
t_{HPLL} (LTR)	Clock to Data Hold - PIO Input Register	1.22	—	ns
t_{HPLL} (Bottom)	Clock to Data Hold - PIO Input Register	1.98	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	4.99	—	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Data Input Delay	0	—	ns

Parameter	Description	–8		Unit
		Min	Max	
General I/O Pin Parameters Using Dedicated Edge Clock Input without PLL				
t_{CO}	Clock to Output - PIO Output Register	—	—	ns
t_{SU}	Clock to Data Setup - PIO Input Register	0	—	ns
t_{HD}	Clock to Data Hold - PIO Input Register	—	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	—	—	ns
General I/O Pin Parameters Using Dedicated Edge Clock Input with PLL				
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Data Input Delay	0	—	ns
t_{COPLL}	Clock to Output - PIO Output Register	—	—	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	—	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	—	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	—	—	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Data Input Delay	0	—	ns
Generic DDR Input/Output				
Generic DDRX1 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX1_RX/TX.SCLK.Centered) using PCLK Clock Input – Bank0, 1, 2, 6, 7 – Figure 3.7 and Figure 3.9				
t_{SU_GDDR1}	Input Data Setup Before CLK	0.917	—	ns
		0.275	—	UI
t_{HO_GDDR1}	Input Data Hold After CLK	0.917	—	ns
t_{DVB_GDDR1}	Output Data Valid Before CLK Output	0.905	—	ns
		–0.762	—	ns + ½UI
t_{DQVA_GDDR1}	Output Data Valid After CLK Output	0.905	—	ns
		–0.762	—	ns + ½UI
f_{DATA_GDDRX1}	Input/Output Data Rate	—	300	Mbps
f_{MAX_GDDRX1}	Frequency of PCLK	—	150	MHz
½ UI	Half of Data Bit Time, or 90 degrees	1.667	—	ns
Output TX to Input RX Margin per Edge		0.191	—	ns
Generic DDRX1 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX1_RX/TX.SCLK.Aligned) using PCLK Clock Input – Bank0, 1, 2, 6, 7 – Figure 3.8 and Figure 3.10				
t_{DVA_GDDR1}	Input Data Valid After CLK	—	–0.917	ns + ½UI
		—	0.75	ns
		—	0.225	UI
t_{DVE_GDDR1}	Input Data Hold After CLK	0.917	—	ns + ½UI
		2.583	—	ns
		0.775	—	UI
t_{DIA_GDDR1}	Output Data Invalid After CLK Output	—	0.559	ns
t_{DIB_GDDR1}	Output Data Invalid Before CLK Output	—	0.559	ns

Parameter	Description	–8		Unit
		Min	Max	
f_{DATA_GDDRX1}	Input/Output Data Rate	—	300	Mbps
f_{MAX_GDDRX1}	Frequency for PCLK	—	150	MHz
½ UI	Half of Data Bit Time, or 90 degrees	1.667	—	ns
Output TX to Input RX Margin per Edge		0.191	—	ns
Generic DDRX1 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX1_RX/TX.SCLK.Centered) using PCLK Clock Input – Bank3, 4, 5 – Figure 3.7 and Figure 3.9				
t_{SU_GDDR1}	Input Data Setup Before CLK	0.917	—	ns
		0.275	—	UI
t_{HO_GDDR1}	Input Data Hold After CLK	0.917	—	ns
$f_{DATA\_IN\_GDDRX1}$	Input Data Rate	—	300	Mbps
t_{DVB_GDDR1}	Output Data Valid Before CLK Output	1.278	—	ns
		–0.389	—	ns + ½UI
t_{DQVA_GDDR1}	Output Data Valid After CLK Output	1.294	—	ns
		–0.373	—	ns + ½UI
$f_{DATA\_OUT\_GDDRX1}$	Output Data Rate	—	300	Mbps
f_{MAX_GDDRX1}	Frequency of PCLK	—	150	MHz
½ UI	Half of Data Bit Time, or 90 degrees	1.667	—	ns
Output TX to Input RX Margin per Edge		0.377	—	ns
Generic DDRX1 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX1_RX/TX.SCLK.Aligned) using PCLK Clock Input – Bank3, 4, 5 – Figure 3.8 and Figure 3.10				
t_{DVA_GDDR1}	Input Data Valid After CLK	—	–0.917	ns + ½UI
		—	0.75	ns
		—	0.225	UI
t_{DVE_GDDR1}	Input Data Hold After CLK	0.917	—	ns + ½UI
		2.583	—	ns
		0.775	—	UI
$f_{DATA\_IN\_GDDRX1}$	Input Data Rate	—	300	Mbps
t_{DIA_GDDR1}	Output Data Invalid After CLK Output	—	0.373	ns
t_{DIB_GDDR1}	Output Data Invalid Before CLK Output	—	0.373	ns
$f_{DATA\_OUT\_GDDRX1}$	Output Data Rate	—	300	Mbps
f_{MAX_GDDRX1}	Frequency for PCLK	—	150	MHz
½ UI	Half of Data Bit Time, or 90 degrees	1.667	—	ns
Output TX to Input RX Margin per Edge		0.377	—	ns
Generic DDRX2 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX2_RX/TX.ECLK.Centered) using PCLK Clock Input –Figure 3.7 and Figure 3.9				
t_{SU_GDDRX2}	Data Setup before CLK Input	0.270	—	ns
		0.162	—	UI
t_{HO_GDDRX2}	Data Hold after CLK Input	0.270	—	ns
t_{DVB_GDDRX2}	Output Data Valid Before CLK Output	0.684	—	ns
		–0.149	—	ns + ½UI

Parameter	Description	–8		Unit
		Min	Max	
t_{DQVA_GDDRX2}	Output Data Valid After CLK Output	0.684	—	ns
		– 0.149	—	ns + ½UI
f_{DATA_GDDRX2}	Input/Output Data Rate	—	600	Mbps
f_{MAX_GDDRX2}	Frequency for ECLK	—	300	MHz
½ UI	Half of Data Bit Time, or 90 degrees	0.833	—	ns
f_{PCLK}	PCLK frequency	—	247.52	MHz
Output TX to Input RX Margin per Edge		0.434	—	ns
Generic DDRX2 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX2_RX/TX.ECLK.Aligned) using PCLK Clock Input – Figure 3.8 and Figure 3.10				
t_{DVA_GDDRX2}	Input Data Valid After CLK	—	–0.458	ns + ½UI
		—	0.375	ns
		—	0.225	UI
t_{DVE_GDDRX2}	Input Data Hold After CLK	0.458	—	ns + ½UI
		1.292	—	ns
		0.775	—	UI
t_{DIA_GDDRX2}	Output Data Invalid After CLK Output	—	0.149	ns
t_{DIB_GDDRX2}	Output Data Invalid Before CLK Output	—	0.149	ns
f_{DATA_GDDRX2}	Input/Output Data Rate	—	600	Mbps
f_{MAX_GDDRX2}	Frequency for ECLK	—	300	MHz
½ UI	Half of Data Bit Time, or 90 degrees	0.833	—	ns
f_{PCLK}	PCLK frequency	—	247.52	MHz
Output TX to Input RX Margin per Edge		0.226	—	ns
Generic DDRX4 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX4_RX/TX.ECLK.Centered) using PCLK Clock Input – Figure 3.7 and Figure 3.9				
t_{SU_GDDRX4}	Input Data Set-Up Before CLK	0.253	—	ns
		0.253	—	UI
t_{HO_GDDRX4}	Input Data Hold After CLK	0.239	—	ns
t_{DVB_GDDRX4}	Output Data Valid Before CLK Output	0.351	—	ns
		–0.149	—	UI
t_{DQVA_GDDRX4}	Output Data Valid After CLK Output	0.351	—	ns
		–0.149	—	UI
f_{DATA_GDDRX4}	Input/Output Data Rate	—	1000	Mbps
f_{MAX_GDDRX4}	Frequency for ECLK	—	500	MHz
½ UI	Half of Data Bit Time, or 90 degrees	0.5	—	ns
f_{PCLK}	PCLK frequency	—	125	MHz
Output TX to Input RX Margin per Edge		0.151	—	ns
Generic DDRX4 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX4_RX/TX.ECLK.Aligned) using PCLK Clock Input, Left and Right sides Only – Figure 3.8 and Figure 3.10				
t_{DVA_GDDRX4}	Input Data Valid After CLK	—	–0.275	ns + ½UI

Parameter	Description	–8		Unit
		Min	Max	
		—	0.225	ns
		—	0.225	UI
t_{DVE_GDDRX4}	Input Data Hold After CLK	0.275	—	ns + ½UI
		0.775	—	ns
		0.775	—	UI
t_{DIA_GDDRX4}	Output Data Invalid After CLK Output	—	0.149	ns
t_{DIB_GDDRX4}	Output Data Invalid Before CLK Output	—	0.149	ns
f_{DATA_GDDRX4}	Input/Output Data Rate	—	1000	Mbps
f_{MAX_GDDRX4}	Frequency for ECLK	—	500	MHz
½ UI	Half of Data Bit Time, or 90 degree	0.5	—	ns
f_{PCLK}	PCLK frequency	—	125	MHz
Output TX to Input RX Margin per Edge		0.076	—	ns
Generic DDRX5 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX5_RX/TX.ECLK.Centered) using PCLK Clock Input – Figure 3.7 and Figure 3.9				
t_{SU_GDDRX5}	Input Data Set-Up Before CLK	0.233	—	ns
		0.233	—	UI
t_{HO_GDDRX5}	Input Data Hold After CLK	0.245	—	ns
$t_{WINDOW\_GDDRX5C}$	Input Data Valid Window	0.4	—	ns
t_{DVB_GDDRX5}	Output Data Valid Before CLK Output	0.351	—	ns
		–0.149	—	ns + ½UI
t_{DQVA_GDDRX5}	Output Data Valid After CLK Output	0.351	—	ns
		–0.149	—	ns + ½UI
f_{DATA_GDDRX5}	Input/Output Data Rate	—	1000	Mbps
f_{MAX_GDDRX5}	Frequency for ECLK	—	500	MHz
½ UI	Half of Data Bit Time, or 90 degrees	0.500	—	ns
f_{PCLK}	PCLK frequency	—	100	MHz
Output TX to Input RX Margin per Edge		0.151	—	ns
Generic DDRX5 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX5_RX/TX.ECLK.Aligned) using PCLK Clock Input – Figure 3.8 and Figure 3.10				
t_{DVA_GDDRX5}	Input Data Valid After CLK	—	–0.275	ns + ½UI
		—	0.225	ns
		—	0.225	UI
t_{DVE_GDDRX5}	Input Data Hold After CLK	0.275	—	ns + ½UI
		0.775	—	ns
		0.775	—	UI
$t_{WINDOW\_GDDRX5A}$	Input Data Valid Window	0.550	—	ns
t_{DIA_GDDRX5}	Output Data Invalid After CLK Output	—	0.149	ns
t_{DIB_GDDRX5}	Output Data Invalid Before CLK Output	—	0.149	ns
f_{DATA_GDDRX5}	Input/Output Data Rate	—	1000	Mbps

Parameter	Description	–8		Unit
		Min	Max	
f_{MAX_GDDRX5}	Frequency for ECLK	—	500	MHz
½ UI	Half of Data Bit Time, or 90 degrees	0.500	—	ns
f_{PCLK}	PCLK frequency	—	100	MHz
Output TX to Input RX Margin per Edge		0.076	—	ns
Soft D-PHY DDRX4 Inputs/Outputs with Clock and Data Centered at Pin, using PCLK Clock Input				
$t_{SU\_GDDRX4\_MP}$	Input Data Set-Up Before CLK	0.240	—	ns
		0.240	—	UI
$t_{HO\_GDDRX4\_MP}$	Input Data Hold After CLK	0.230	—	ns
$t_{DVB\_GDDRX4\_MP}$	Output Data Valid Before CLK Output	0.300	—	ns
		0.300	—	UI
$t_{DQVA\_GDDRX4\_MP}$	Output Data Valid After CLK Output	0.300	—	ns
		0.300	—	UI
$f_{DATA\_GDDRX4\_MP}$	Input Data Bit Rate for MIPI PHY	—	1000	Mbps
½ UI	Half of Data Bit Time, or 90 degrees	0.500	—	ns
f_{PCLK}	PCLK frequency	—	125	MHz
Output TX to Input RX Margin per Edge		0.100	—	ns
Video DDRX71 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX71_RX.ECLK) using PLL Clock Input – Figure 3.12 and Figure 3.13				
t_{RPBi_DVA}	Input Valid Bit "i" switch from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	0.237	UI
		—	–0.278	ns+(½+i)×UI
t_{RPBi_DVE}	Input Hold Bit "i" switch from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	0.748	—	UI
		0.262	—	ns+(½+i)×UI
t_{TPBi_DOV}	Data Output Valid Bit "i" switch from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	0.159	ns+i×UI
t_{TPBi_DOI}	Data Output Invalid Bit "i" switch from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	–0.159	—	ns+(i+ 1) ×UI
$t_{TPBi\_skew\_UI}$	TX skew in UI	—	0.15	UI
t_B	Serial Data Bit Time, = 1UI	1.058	—	ns
f_{DATA_TX71}	DDR71 Serial Data Rate	—	945	Mbps
f_{MAX_TX71}	DDR71 ECLK Frequency	—	473	MHz
f_{CLKIN}	7:1 Clock (PCLK) Frequency	—	133.7	MHz
Output TX to Input RX Margin per Edge		0.159	—	ns
Memory Interface				
DDR3/DDR3L/LPDDR2/LPDDR3 READ (DQ Input Data are Aligned to DQS) – Figure 3.8				
t_{DVBDQ_DDR3} t_{DVBDQ_DDR3L} t_{DVBDQ_LPDDR2} t_{DVBDQ_LPDDR3}	Data Output Valid before DQS Input	—	–0.235	ns + ½UI
t_{DVADQ_DDR3} t_{DVADQ_DDR3L} t_{DVADQ_LPDDR2} t_{DVADQ_LPDDR3}	Data Output Valid after DQS Input	0.235	—	ns + ½UI
f_{DATA_DDR3} f_{DATA_DDR3L} fDATA_LPDDR2 fDATA_LPDDR3	DDR Memory Data Rate	—	1066	Mbps
$f_{MAX\_ECLK\_DDR3}$ $f_{MAX\_ECLK\_DDR3L}$	DDR Memory ECLK Frequency	—	533	MHz

Parameter	Description	–8		Unit
		Min	Max	
$f_{MAX\_ECLK\_LPDDR2}$ $f_{MAX\_ECLK\_LPDDR3}$				
$f_{MAX\_SCLK\_DDR3}$ $f_{MAX\_SCLK\_DDR3L}$ $f_{MAX\_SCLK\_LPDDR2}$ $f_{MAX\_SCLK\_LPDDR3}$	DDR Memory SCLK Frequency	—	133.3	MHz
DDR3/DDR3L/LPDDR2/LPDDR3 WRITE (DQ Output Data are Centered to DQS) – Figure 3.11				
t_{DQVBS_DDR3} t_{DQVBS_DDR3L} t_{DQVBS_LPDDR2} t_{DQVBS_LPDDR3}	Data Output Valid before DQS Output	—	–0.235	ns + ½UI
t_{DQVAS_DDR3} t_{DQVAS_DDR3L} t_{DQVAS_LPDDR2} t_{DQVAS_LPDDR3}	Data Output Valid after DQS Output	0.235	—	ns + ½UI
f_{DATA_DDR3} f_{DATA_DDR3L} f_{DATA_LPDDR2} f_{DATA_LPDDR3}	DDR Memory Data Rate	—	1066	Mbps
$f_{MAX\_ECLK\_DDR3}$ $f_{MAX\_ECLK\_DDR3L}$ $f_{MAX\_ECLK\_LPDDR2}$ $f_{MAX\_ECLK\_LPDDR3}$	DDR Memory ECLK Frequency	—	533	MHz
$f_{MAX\_SCLK\_DDR3}$ $f_{MAX\_SCLK\_DDR3L}$ $f_{MAX\_SCLK\_LPDDR2}$ $f_{MAX\_SCLK\_LPDDR3}$	DDR Memory SCLK Frequency	—	133.3	MHz
LPDDR4				
f_{DATA_LPDDR4}	DDR Memory Data Rate	—	1066	Mb/s
$f_{MAX\_ECLK\_LPDDR4}$	DDR Memory ECLK Frequency	—	533	MHz
$f_{MAX\_SCLK\_LPDDR4}$	DDR Memory SCLK Frequency	—	133.3	MHz

Notes:

1. Lattice Automotive/ Frontgrade Space PEM QD timing numbers are shown.
2. General I/O timing numbers are based on LVCMOS18, 1.8 V, 8 mA, Fast Slew Rate, 0 pF load.
   Generic DDR timing are numbers based on LVDS I/O.
   DDR3 timing numbers are based on SSTL15.
   LPDDR2 and LPDDR3 timing numbers are based on HSUL12.
   Uses LVDS I/O standard for measurements.
3. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
4. All numbers are generated with the Lattice Radiant software.
5. This clock skew is not the internal clock network skew. The Nexus family devices have very low internal clock network skew that can be approximated to 0 ps. These tSKEW values measured externally at system level includes additional skew added by the I/O, wire bonding and package ball.

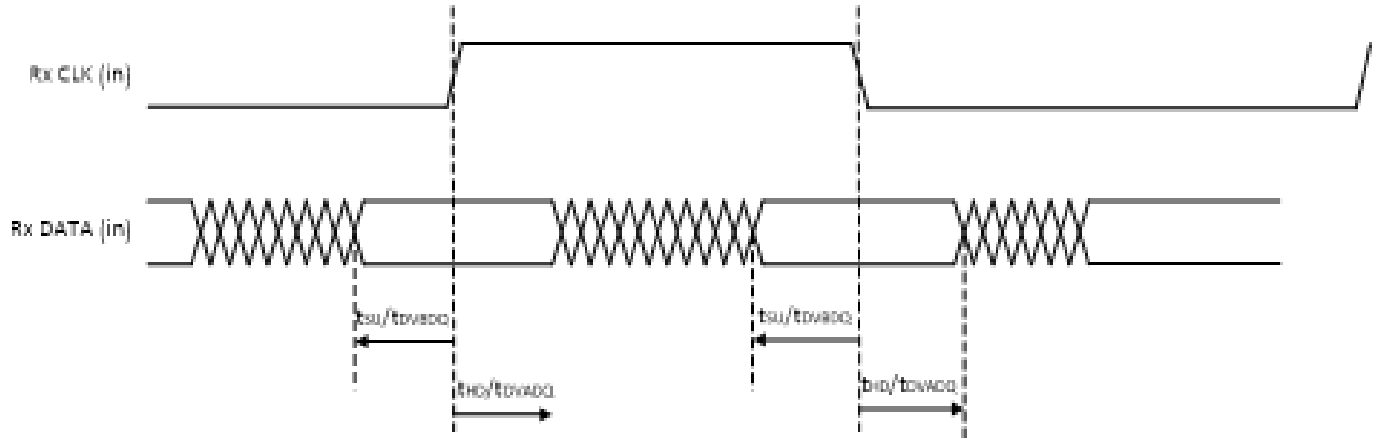


Figure 3.7. Receiver RX.CLK.Centered Waveforms

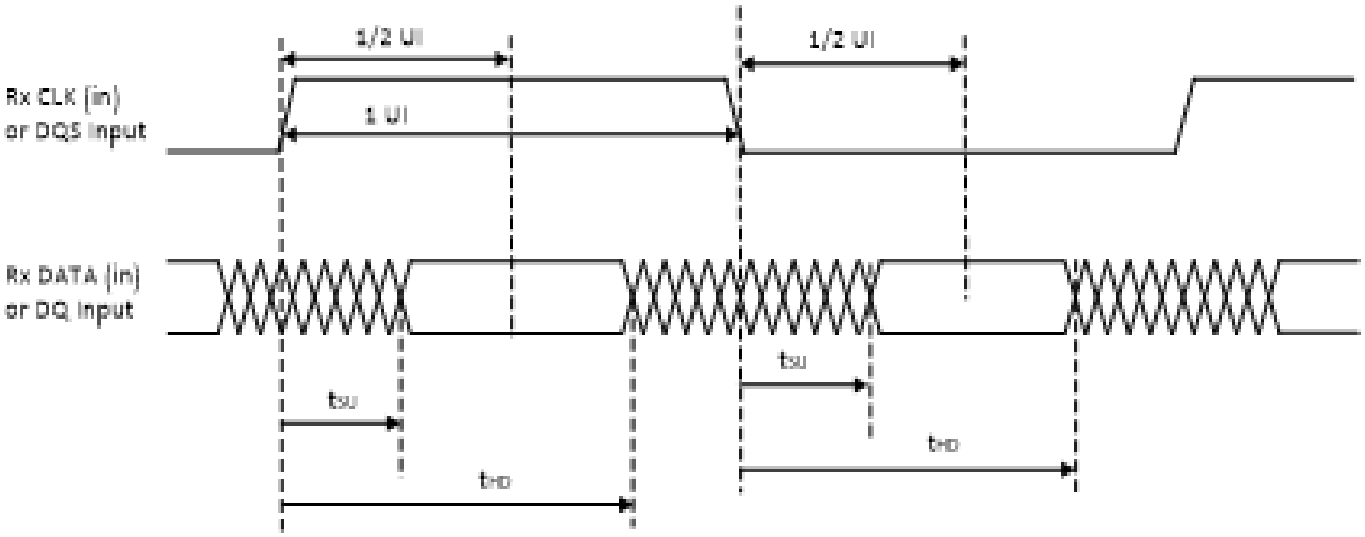


Figure 3.8. Receiver RX.CLK.Aligned and DDR Memory Input Waveforms

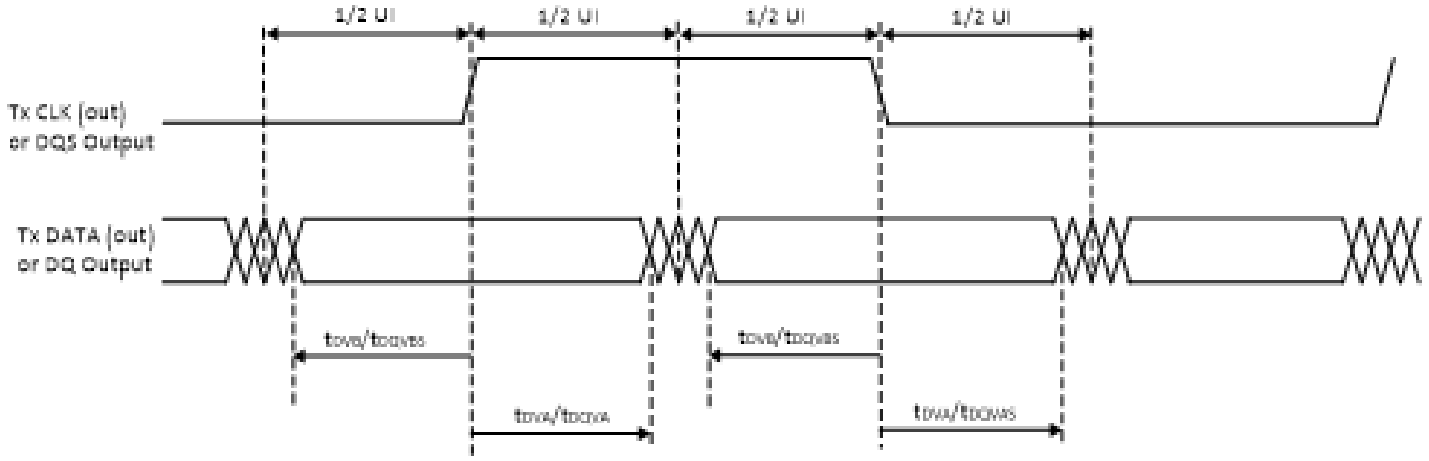


Figure 3.9. Transmit TX.CLK.Centered and DDR Memory Output Waveforms

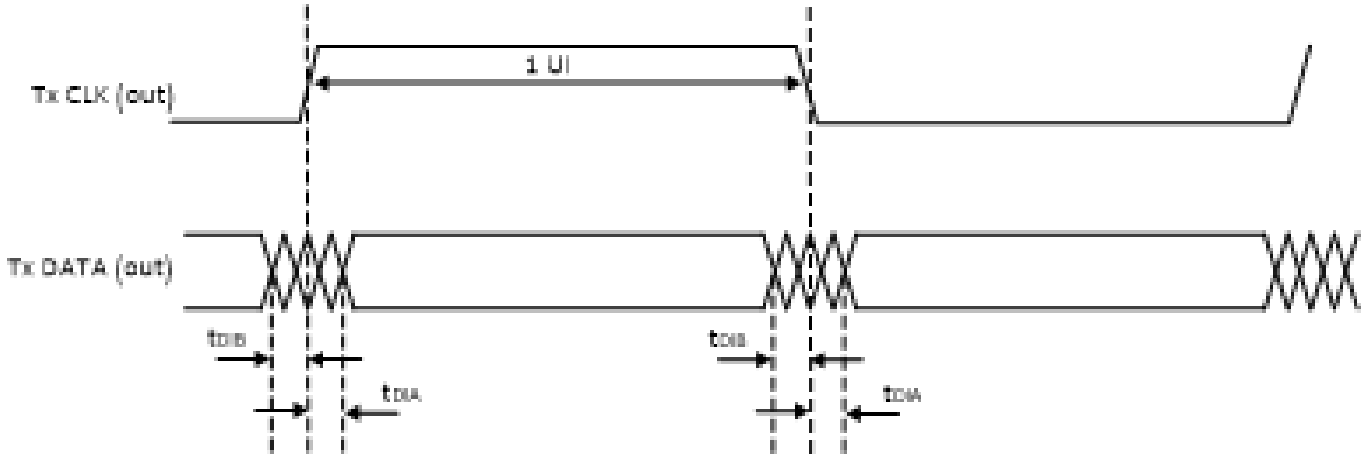


Figure 3.10. Transmit TX.CLK.Aligned Waveforms

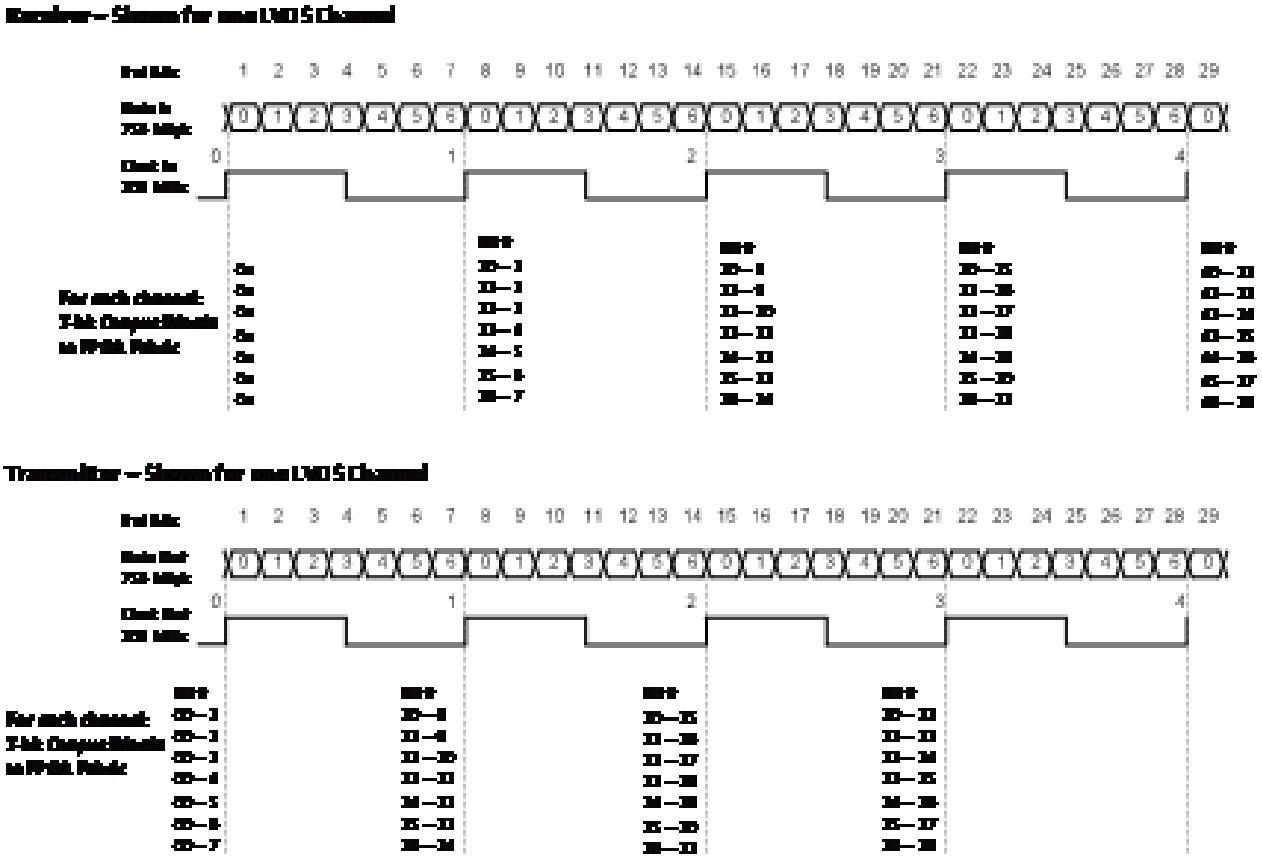


Figure 3.11. DDRX71 Video Timing Waveforms

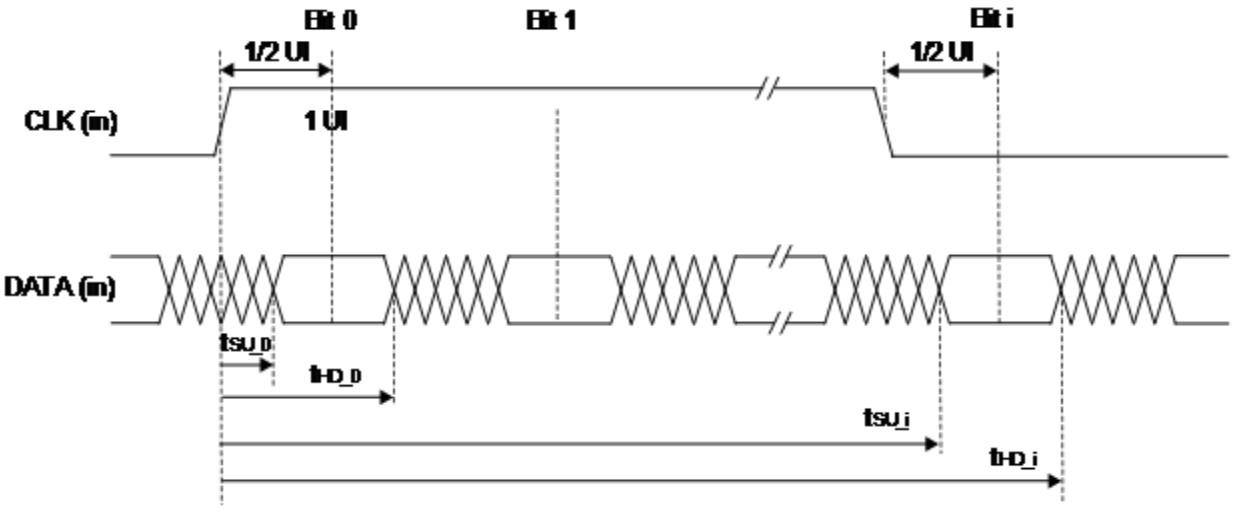


Figure 3.12. Receiver DDRX71_RX Waveforms

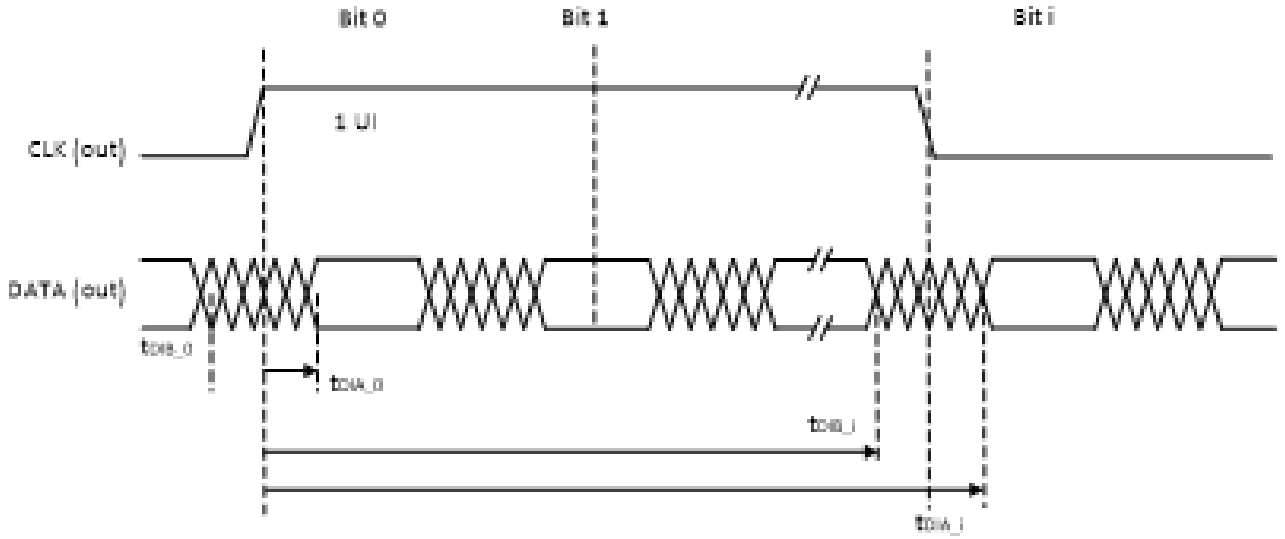


Figure 3.13. Transmitter DDRX71_TX Waveforms

3.17 sysCLOCK PLL Timing (VCC = 1.0 V)

Over recommended operating conditions.

Table 3.33 sysCLOCK PLL Timing (VCC = 1.0 V)

Parameter	Descriptions	Conditions	Min	Typ.	Max	Unit
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	—	18	—	500	MHz
f_{OUT}	Output Clock Frequency	—	6.25	—	800	MHz
f_{VCO}	PLL VCO Frequency	—	800	—	1600	MHz
f_{PFD}	Phase Detector Input Frequency	Without Fractional-N Enabled	18	—	500	MHz
		With Fractional-N Enabled	18	—	100	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	—	45	—	55	%
t_{PH}[4]	Output Phase Accuracy	—	–5	—	5	%
t_{OPJIT}[1]	Output Clock Period Jitter	$f_{OUT} \geq 200$ MHz	—	—	250	ps p-p
		$f_{OUT} < 200$ MHz	—	—	0.05	UIPP
	Output Clock Cycle-to-Cycle Jitter	$f_{OUT} \geq 200$ MHz	—	—	250	ps p-p
		$f_{OUT} < 200$ MHz	—	—	0.05	UIPP
	Output Clock Phase Jitter	$f_{PFD} \geq 200$ MHz	—	—	250	ps p-p
		60 MHz ≤ f_{PFD} < 200 MHz	—	—	400	ps p-p
		30 MHz ≤ f_{PFD} < 60 MHz	—	—	500	ps p-p
		18 MHz ≤ f_{PFD} < 30 MHz	—	—	725	ps p-p
	Output Clock Period Jitter (Fractional-N)	$f_{OUT} \geq 200$ MHz	—	—	350	ps p-p
		$f_{OUT} < 200$ MHz	—	—	0.07	UIPP

Parameter	Descriptions	Conditions	Min	Typ.	Max	Unit
	Output Clock Cycle-to-Cycle Jitter (Fractional-N)	f_{OUT} ≥ 200 MHz	—	—	400	ps p-p
		f_{OUT} < 200 MHz	—	—	0.08	UIPP
f_{BW}[3]	PLL Loop Bandwidth	—	0.45	—	13	MHz
t_{LOCK}[2]	PLL Lock-in Time	—	—	—	10	ms
t_{UNLOCK}	PLL Unlock Time (from RESET goes HIGH)	—	—	—	50	ns
t_{IPJIT}	Input Clock Period Jitter	f_{PFD} ≥ 20 MHz	—	—	500	ps p-p
		f_{PFD} < 20 MHz	—	—	0.01	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	—	ns
t_{RST}	RST/ Pulse Width	—	1	—	—	ms
f_{SSC_MOD}	Spread Spectrum Clock Modulation Frequency	—	20	—	200	kHz
$f_{SSC\_MOD\_AMP}$	Spread Spectrum Clock Modulation Amplitude Range	—	0.25	—	2.00	%
$f_{SSC\_MOD\_STEP}$	Spread Spectrum Clock Modulation Amplitude Step Size	—	—	0.25	—	%

Notes:

1. Jitter sample is taken over 10,000 samples for Period jitter, and 1,000 samples for Cycle-to-Cycle jitter of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after tLOCK for PLL reset and dynamic delay adjustment.
3. Result from Lattice Radiant software.
4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency.

3.18 Internal Oscillators Characteristics

Table 3.34 Internal Oscillators (VCC = 1.0 V)

Symbol	Parameter Description	Min	Typ	Max	Unit
f_{CLKHF}	HFOSC Clock Frequency	418.5	450	481.5	MHz
f_{CLKLF}	LFOSC Clock Frequency	18.2	32	45.8	kHz
DCH_{CLKHF}	HFOSC Duty Cycle (Clock High Period)	43	50	57	%
DCH_{CLKLF}	LFOSC Duty Cycle (Clock High Period)	45	50	55	%

3.19 User I²C Characteristics

Table 3.35 User I²C Specifications (VCC = 1.0 V)

Symbol	Parameter Description	STD Mode			FAST Mode			FAST Mode Plus2			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{scl}	SCL Clock Frequency	—	—	100	—	—	400	—	—	1000	kHz
T_{DELAY}	Optional delay through delay block	—	62	—	—	62	—	—	62	—	ns

Notes:

1. Refer to the I²C Specification for timing requirements. User design should set constraints in Lattice Design Software to meet this industrial I²C Specification.
2. Fast Mode Plus maximum speed may be achieved by using external pull up resistor on I²C bus. Internal pull up may not be sufficient to support the maximum speed.

3.20 Analog-Digital Converter (ADC) Block Characteristics

Table 3.36 ADC Specifications1

Symbol	Description	Condition	Min	Typ	Max	Unit
V_{REFINT_ADC}	ADC Internal Reference Voltage	—	1.14[2]	1.2	1.26[2]	V
V_{REFEXT_ADC}	ADC External Reference Voltage	—	1.0	—	1.8	V
N_{RES_ADC}	ADC Resolution	—	—	12	—	bit
ENOBADC	Effective Number of Bits	—	9.9	11	—	bit
V_{SR_ADC}	ADC Input Range	Bipolar Mode, Internal VREF	V_{CM_ADC} — $V_{REFINT\_ADC}/4$	V_{CM_ADC}	V_{CM_ADC} + $V_{REFINT\_ADC}/4$	V
		Bipolar Mode, External VREF	V_{CM_ADC} – $V_{REFEXT\_ADC}/4$	V_{REFEXT_ADC}	V_{CM_ADC} + $V_{REFEXT\_ADC}/4$	V
		Uni-polar Mode, Internal VREF	0	—	V_{REFINT_ADC}	V
		Uni-polar Mode, External VREF	0	—	V_{REFEXT_ADC}	V
V_{CM_ADC}	ADC Input Common Mode Voltage (for fully differential signals)	Internal VREF	—	½VREFINT_ADC	—	V
		External VREF	—	½VREFEXT_ADC	—	V
f_{CLK_ADC}	ADC Clock Frequency	—	—	25	40	MHz
DC_{CLK_ADC}	ADC Clock Duty Cycle	—	48	50	52	%
f_{INPUT_ADC}	ADC Input Frequency	—	—	—	500	kHz
FS_{ADC}	ADC Sampling Rate	—	—	1	—	MS/s
N_{TRACK_ADC}	ADC Input Tracking Time	—	4	—	—	cycle[3]
R_{IN_ADC}	ADC Input Equivalent Resistance	1 MS/s, Sampled @ 2 clock cycles	—	116	—	KΩ
t_{CAL_ADC}	ADC Calibration Time	—	—	—	6500	cycle[3]
L_{OUTPUT_ADC}	ADC Conversion Time	Includes minimum tracking time of four cycles	25	—	—	cycle[3]

Symbol	Description	Condition	Min	Typ	Max	Unit
DNL_{ADC}	ADC Differential Nonlinearity	—	–1	—	1	LSB
INL_{ADC}	ADC Integral Nonlinearity	—	–2	—	2.21	LSB
$SFDR_{ADC}$	ADC Spurious Free Dynamic Range	—	65.8	77	—	dBc
THD_{ADC}	ADC Total Harmonic Distortion	—	—	–76	–66.4	dB
SNR_{ADC}	ADC Signal to Noise Ratio	—	61.6	68	—	dB
$SNDR_{ADC}$	ADC Signal to Noise Plus Distortion Ratio	—	61.5	67	—	dB
ERR_{GAIN_ADC}	ADC Gain Error	—	–0.5	—	0.5	% FS_{ADC}
ERR_{OFFSET_ADC}	ADC Offset Error	—	–2	—	2	LSB
C_{IN_ADC}	ADC Input Equivalent Capacitance	—	—	2	—	pF

Notes:

1. ADC is available in select speed grades. See ordering information.
2. Not tested; guaranteed by design.
3. ADC Sample Clock cycles. See ADC User Guide for Nexus Platform (FPGA-TN-02129) for more details.

3.21 Comparator Block Characteristics

Table 3.37 Comparator Specifications

Symbol	Description	Min	Typ	Max	Unit
f_{IN_COMP}	Comparator Input Frequency	—	—	10	MHz
V_{IN_COMP}	Comparator Input Voltage	0	—	$V_{CCADC18}$	V
V_{OFFSET_COMP}	Comparator Input Offset	–34.3	—	36.44	mV
V_{HYST_COMP}	Comparator Input Hysteresis	10	—	31.62	mV
$V_{LATENCY\_COMP}$	Comparator Latency	—	—	31.24	ns

3.22 Digital Temperature Readout Characteristics

Digital temperature Readout (DTR) is implemented in one of the internal Analog-Digital-Converter (ADC) channel.

Table 3.38 DTR Specifications [1,2]

Symbol	Description	Condition	Min	Typ	Max	Unit
DTR_{RANGE}	DTR Detect Temperature Range	—	–40	—	125	°C
$DTR_{ACCURACY}$	DTR Accuracy	with external voltage reference range of 1.0 V to 1.8 V	–16	±6	16	°C
$DTR_{RESOLUTION}$	DTR Resolution	with external voltage reference	–0.3	—	0.3	°C

Notes:

1. External voltage reference (VREF) should be 0.1% accurate or better. DTR sensitivity to VREF is -4.1 °C per VREF per-cent (for example, if the VREF is 1 % low, then the DTR will read +4.1 °C high).
2. DTR is available in select speed grades. See ordering information.

3.23 SerDes High-Speed Data Transmitter

Table 3.39 Serial Output Timing and Levels

Symbol	Description	Condition	Min	Typ	Max	Unit
Transmitter 5 Gbps						
$V_{TX-DIFF-PP}$	Peak-Peak Differential voltage on selected amplitude [1, 2]	—	800	1000	1200	mV, p-p
$V_{TX-CM-DC}$	Output common mode voltage [1, 2]	—	400	500	600	mV, p-p
V_{TX-EH}	Transmitter Eye Height [1, 2]	—	630	740	—	mV, p-p
V_{TX-EW}	Transmitter Eye width (all jitter sources)	—	170	180	—	ps
T_{TX-R}	Transmitter Eye Rise time (20% to 80%)	—	56	—	66	ps
T_{TX-F}	Transmitter Eye Fall time (80% to 20%)	—	56	—	66	ps
Transmitter 1.25 Gbps						
$V_{TX-DIFF-PP}$	Peak-Peak Differential voltage on selected amplitude [1, 2]	—	800	1000	1200	mV, p-p
$V_{TX-CM-DC}$	Output common mode voltage [1, 2]	—	400	500	600	mV, p-p
V_{TX-EH}	Transmitter Eye Height [1, 2]	—	645	800	—	mV, p-p
V_{TX-EW}	Transmitter Eye width (all jitter sources)	—	770	780	—	ps
T_{TX-R}	Transmitter Eye Rise time (20% to 80%)	—	65	—	80	ps
T_{TX-F}	Transmitter Eye Fall time (80% to 20%)	—	63	—	80	ps
Transmitter All Rates						
$T_{TX-CM-AC-P}$	RMS AC peak common-mode output voltage	—	—	—	20	mV
$Z_{TX\_DIFF-DC}$	DC Differential Impedance	—	80	—	120	Ω
RL_{TX_DIFF}	Tx Differential Return Loss (with package included)	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
		2.5 GHz < freq < 4 GHz	4	—	—	dB
		4GHz < freq <= 5 GHz	4	—	—	dB
RL_{TX_COM}	Tx Common mode Return Loss (with package included)	50 MHz < freq < 2.5 GHz	6	—	—	dB
		2.5 GHz < freq <= 4 GHz	3	—	—	dB
		4GHz < freq <= 5 GHz	3	—	—	dB

Notes:

1. Measured with 50 Ω Tx Driver impedance at VCCHTX±5%. Fixture de-embedded.
2. Refer to CertusPro-NX SerDes/PCS Usage Guide (FPGA-TN-02245) for settings of Tx amplitude.

Table 3.40 Channel Output Jitter

Symbol	Description	Min	Typ	Max	Unit
Transmitter 5 Gbps[3]					
T_{TX-DJ}	5 Gbps Transmitter Deterministic Jitter3	—	—	22	ps, p-p
T_{TX-RJ}	5 Gbps Transmitter Random Jitter3	—	—	1	ps, RMS
T_{TX-TJ}	5 Gbps Transmitter Total Jitter3	—	—	38	ps, p-p
Transmitter 3.125 Gbps[3]					
T_{TX-DJ}	3.125 Transmitter Gbps Deterministic Jitter3	—	—	20	ps, p-p
T_{TX-RJ}	3.125 Transmitter Gbps Random Jitter3	—	—	1	ps, RMS
T_{TX-TJ}	3.125 Transmitter Gbps Total Jitter3	—	—	40	ps, p-p
Transmitter 2.5 Gbps[3]					
T_{TX-DJ}	2.5 Transmitter Gbps Deterministic Jitter3	—	—	20	ps, p-p
T_{TX-RJ}	2.5 Transmitter Gbps Random Jitter3	—	—	1	ps, RMS
T_{TX-TJ}	2.5 Transmitter Gbps Total Jitter3	—	—	40	ps, p-p
Transmitter 1.25 Gbps[3]					
T_{TX-DJ}	1.25 Transmitter Gbps Deterministic Jitter3	—	—	20	ps, p-p
T_{TX-RJ}	1.25 Transmitter Gbps Random Jitter3	—	—	1	ps, RMS
T_{TX-TJ}	1.25 Transmitter Gbps Total Jitter3	—	—	40	ps, p-p

Notes:

3. All other rates were taken with the DCA-J at PRBS 2N^7 - 1.

3.24 SerDes High-Speed Data Receiver

Table 3.41 Serial Input Data Specifications

Symbol	Description	Condition	Min	Typ	Max	Unit
$V_{RX-DIFF-S}$	Differential input sensitivity1	—	100	—	1200	mV, p-p
V_{RX-IN}	Input levels	—	25	—	1300	mV, p-p
RX_SSC	JTOL BER with SSC (.5%Dev 33 kHz Triangle Down Conv.)	—	—	—	–5000	ppm
$Z_{RX-DIFF-DC}$	Receiver DC differential impedance	—	80	—	120	Ω
$Z_{RX-HIGH\_IMP-DC}$	Receiver DC differential impedance when powered down	termination_at_-150mv	1K	—	—	KΩ
		termination_at_0V	10K	—	—	KΩ
		termination_at_200mv	20K	—	—	KΩ
$RL_{RX-DIFF}$	Receiver differential Return Loss, package plus silicon	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
		2.5 GHz < freq < 4 GHz	5	—	—	dB
		4 GHz < freq <= 5 GHz	4	—	—	dB
RL_{RX-CM}	Receiver common mode Return Loss, package plus silicon	50 MHz < freq < 2.5 GHz	6	—	—	dB
		2.5 GHz < freq <= 4 GHz	5	—	—	dB
		4.0 GHz < freq <= 5 GHz	4	—	—	dB

Symbol	Description	Condition	Min	Typ	Max	Unit
V_{RX-LOS}[3]	Loss of signal Detect Threshold	50 MHz < freq <= 1.25 GHz	0.06	—	0.175	V, p-p
		1.25 GHz < freq < 1.5 GHz	0.065	—	0.175	V, p-p

Notes:

1. Measured into 50 Ω Tx impedance at ±5%. With EQ but no stressors added. Fixture de-embedded for 10.3125 Gbps. This is a fixed BER Test with 26% margin.
2. Refer to PCIe RX stress test.
3. Loss of signal Detect Threshold has a frequency dependency that effects threshold voltage at temperature dependency where –40 °C is the worst case therefore the two conditions.

3.25 Input Data Jitter Tolerance

The receiver ability to tolerate incoming signal jitter is very dependent on jitter type. High-speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

Table 3.42 Receiver Total Jitter Tolerance Specification

Protocol	Description	Frequency	Condition	Min	Typ	Max	Unit
PCIe	Deterministic	5 Gbps	See PCIe Spec	—	—	—	UI
	Random		See PCIe Spec	—	—	—	ps, RMS
	Total		See PCIe Spec	—	—	0.4	UI
	Deterministic	2.5 Gbps	400 mV differential eye	—	—	—	UI
	Random		400 mV differential eye	—	—	—	ps, RMS
	Total		400 mV differential eye	—	—	0.4	UI
Ethernet	Deterministic	6.25 Gbps	See RXAUI Spec, PRBS31	—	—	—	UI
	Random		See RXAUI Spec, PRBS31	—	—	—	ps, RMS
	Total		See RXAUI Spec, PRBS31	—	—	0.4	UI
	Deterministic	5 Gbps	—	—	—	—	UI
	Random		—	—	—	—	ps, RMS
	Total		—	—	—	—	UI
	Deterministic	3.125 Gbps	See XAUI Spec, CJPAT	—	—	—	UI
	Random		See XAUI Spec, CJPAT	—	—	—	ps, RMS
	Total		See XAUI Spec, CJPAT	—	—	0.35	UI
	Deterministic	1.25 Gbps	400 mV differential eye	—	—	—	UI
	Random		400 mV differential eye	—	—	—	ps, RMS
	Total		400 mV differential eye	—	—	0.7	UI
SLVS_EC	Deterministic	5 Gbps	400 mV differential eye	—	—	—	UI
	Random		400 mV differential eye	—	—	—	ps, RMS
	Total		400 mV differential eye	—	—	0.5	UI
	Deterministic	2.5 Gbps	400 mV differential eye	—	—	—	UI
	Random		400 mV differential eye	—	—	—	ps, RMS

Protocol	Description	Frequency	Condition	Min	Typ	Max	Unit
	Total		400 mV differential eye	—	—	0.62	UI
	Deterministic		400 mV differential eye	—	—	—	UI
	Random	1.25 Gbps	400 mV differential eye	—	—	—	ps, RMS
	Total		400 mV differential eye	—	—	0.7	UI
	Deterministic		—	—	—	—	UI
	Random	6.25 Gbps	—	—	—	—	ps, RMS
	Total		—	—	—	—	UI
	Deterministic		400 mV differential eye	—	—	—	UI
	Random	5 Gbps	400 mV differential eye	—	—	—	ps, RMS
	Total		400 mV differential eye	—	—	0.4	UI
	Deterministic		400 mV differential eye	—	—	—	UI
CoaXPress	Random	3.125 Gbps	400 mV differential eye	—	—	—	ps, RMS
	Total		400 mV differential eye	—	—	0.35	UI
	Deterministic		400 mV differential eye	—	—	—	UI
	Random	2.5 Gbps	400 mV differential eye	—	—	—	ps, RMS
	Total		400 mV differential eye	—	—	0.4	UI
	Deterministic		400 mV differential eye	—	—	—	UI
	Random	1.25 Gbps	400 mV differential eye	—	—	—	ps, RMS
	Total		400 mV differential eye	—	—	0.7	UI
	Deterministic		—	—	—		UI
	Random	5.4 Gbps	—	—	—	—	ps, RMS
	Total		—	—	—	0.636	UI
	Deterministic		—	—	—	—	UI
DP/eDP	Random	2.7 Gbps	—	—	—	—	ps, RMS
	Total		—	—	—	0.548	UI
	Deterministic		—	—	—	—	UI
	Random	1.62 Gbps	—	—	—	—	ps, RMS
	Total		—	—	—	0.778	UI

Note: Jitter tolerance measurements are done with protocol compliance tests: 3.125 Gbps - XAUI Standard, 8/5/2.5 Gbps - PCIe Standard, 1.25 Gbps SGMII Standard.

3.26 SerDes External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. Tables 3.43 and 3.44 specify the reference clock requirements, over the full range of operating conditions. For other characteristics like jitter, the clock requirements of the target protocol should be used when determining the reference clock source.

Table 3.43 External Reference Clock Specification for SDQx_REFCLKP/N[1]

Symbol	Description	Min	Type	Max	Unit
F_{REF}	Frequency range	74.25	100	162	MHz
$F_{REF-PPM}$	Frequency tolerance	–300	—	300	ppm
$V_{REF-IN-DIFF}$	Input swing, differential clock	300	—	—	mV, p-p differential
V_{REF-IN}	DC Input levels	–0.3	—	1.15	V
D_{REF}	Duty cycle	40	—	60	%
$Z_{REF-IN-TERM-DIFF}$[2]	Differential input termination	—	—	—	Ω

Notes:

1. Support HCSL I/O standard, DC coupling only.
2. No termination.

Table 3.44 External Reference Clock Specification for SD_EXTx_REFCLKP/N[1]

Symbol	Description	Min	Type	Max	Unit
F_{REF}	Frequency range	74.25	—	162	MHz
$F_{REF-PPM}$	Frequency tolerance	–300	—	300	ppm
$V_{REF-IN-DIFF}$	Input swing, differential clock	200	—	2 × VCCAUX	mV, p-p differential
V_{REF-IN}	DC Input levels	0	—	2	V
D_{REF}	Duty cycle	40	—	60	%
T_{REF-R}	Rise time (20% to 80%)	200	500	1000	ps
T_{REF-F}	Fall time (80% to 20%)	200	500	1000	ps
$Z_{REF-IN-TERM-DIFF}$[2]	Differential input termination	70	100	130	Ω

Notes:

1. Support LVDS and HCSL I/O standards.
2. Can be configured as HiZ.

3.27 PCI Express Electrical and Timing Characteristics

3.27.1 PCIe (2.5 Gbps)

Over recommended operating conditions.

Table 3.45 PCIe (2.5 Gbps)

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Transmitter[1]						
UI	Unit Interval	—	399.88	400	400.12	ps
BW_{TX}	Tx PLL bandwidth	—	1.5	—	22	MHz
PKG_{TX}	Tx PLL Peaking	—	—	—	3	dB
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	—	0.8	—	1.2	Vp-p
$V_{TX-DIFF-PP-LOW}$	Low power differential p-p Tx voltage swing	—	0.4	—	1.2	Vp-p
$V_{TX-DE-RATIO-3.5dB}$	Tx de-emphasis level ratio at 3.5 dB	—	3	—	4	dB
$T_{TX-RISE-FALL}$	Transmitter rise and fall time	—	0.125	—	—	UI
T_{TX-EYE}	Transmitter Eye, including all jitter sources	—	0.75	—	—	UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Max. time between jitter median and max deviation from the median	—	—	—	0.125	UI
$RL_{TX-DIFF}$	Tx Differential Return Loss, including pkg and silicon	—	10	—	—	dB
RL_{TX-CM}	Tx Common Mode Return Loss, including pkg and silicon	50 MHz < freq < 2.5 GHz	6	—	—	dB
$Z_{TX-DIFF-DC}$	DC differential Impedance	—	80	—	120	Ω
$V_{TX-CM-AC-P}$	Tx AC peak common mode voltage, RMS	—	—	—	20	mV, RMS
$I_{TX-SHORT}$	Transmitter short-circuit current	—	—	—	90	mA
$V_{TX-DC-CM}$	Transmitter DC common-mode voltage	—	0	—	1.2	V
$V_{TX-IDLE-DIFF-AC-p}$	Electrical Idle Output peak voltage	—	—	—	20	mV
$V_{TX-RCV-DETECT}$	Voltage change allowed during Receiver Detect	—	—	—	600	mV
$T_{TX-IDLE-MIN}$	Min. time in Electrical Idle	—	20	—	—	ns
$T_{TX-IDLE-SET-TO-IDLE}$	Max. time from EI Order Set to valid Electrical Idle	—	—	—	8	ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Max. time from Electrical Idle to valid differential output	—	—	—	8	ns
Receiver[2]						
UI	Unit Interval	—	399.88	400	400.12	ps
$V_{RX-DIFF-PP}$	Differential Rx peak-peak voltage	—	0.175	—	1.2	Vp-p
T_{RX-EYE}[3]	Receiver eye opening time	—	0.4	—	—	UI

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$[3]	Max time delta between median and deviation from median	—	—	—	0.3	UI
$RL_{RX\text{-}DIFF}$	Receiver differential Return Loss, package plus silicon	—	10	—	—	dB
$RL_{RX\text{-}CM}$	Receiver common mode Return Loss, package plus silicon	—	6	—	—	dB
$Z_{RX\text{-}DC}$	Receiver DC single ended impedance	—	40	—	60	Ω
$Z_{RX\text{-}DIFF\text{-}DC}$	Receiver DC differential impedance	—	80	—	120	Ω
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	Receiver DC single ended impedance when powered down	—	200k	—	—	Ω
$V_{RX\text{-}CM\text{-}AC\text{-}P3}$	Rx AC peak common mode voltage	—	—	—	150	mV, peak
$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}PP}$	Electrical Idle Detect Threshold	—	65	—	175	mVp-p

Notes:

1. Refer to PCI Express Base Specification Revision 3.0 Table 4.18 test condition and requirement for respective parameters.
2. Refer to PCI Express Base Specification Revision 3.0 Table 4.24 test condition and requirement for respective parameters.
3. Spec compliant requirement.

3.27.2 PCIe (5 Gbps)

Over recommended operating conditions.

Table 3.46 PCIe (5 Gbps)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Transmit[1]						
UI	Unit Interval	—	199.94	200	200.06	ps
$BW_{TX\text{-}PKG\text{-}PLL1}$	Tx PLL bandwidth corresponding to PKGTX-PLL1	—	8	—	16	MHz
$BW_{TX\text{-}PKG\text{-}PLL2}$	Tx PLL bandwidth corresponding to PKGTX-PLL2	—	5	—	16	MHz
$PKG_{TX\text{-}PLL1}$	Tx PLL Peaking corresponding to PKGTX-PLL1	—	—	—	3	dB
$PKG_{TX\text{-}PLL2}$	Tx PLL Peaking corresponding to PKGTX-PLL2	—	—	—	1	dB
$V_{TX\text{-}DIFF\text{-}PP}$	Differential p-p Tx voltage swing	—	0.8	—	1.2	V, p-p
$V_{TX\text{-}DIFF\text{-}PP\text{-}LOW}$	Low power differential p-p Tx voltage swing	—	0.4	—	1.2	V, p-p
$V_{TX\text{-}DE\text{-}RATIO\text{-}3.5dB}$	Tx de-emphasis level ratio at 3.5 dB	—	3	—	4	dB
$V_{TX\text{-}DE\text{-}RATIO\text{-}6dB}$	Tx de-emphasis level ratio at 6 dB	—	5.5	—	6.5	dB
$T_{MIN\text{-}PULSE}$	Instantaneous lone pulse width	—	0.9	—	—	UI
$T_{TX\text{-}RISE\text{-}FALL}$	Transmitter rise and fall time	—	0.15	—	—	UI

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
T_{TX-EYE}	Transmitter Eye, including all jitter sources	—	0.75	—	—	UI
$_{TTX-DJ}$	Tx deterministic jitter > 1.5 MHz	—	—	—	0.15	UI
T_{TX-RJ}	Tx RMS jitter < 1.5 MHz	—	—	—	3	ps, RMS
$T_{RF-MISMATCH}$	Tx rise/fall time mismatch	—	—	—	0.1	UI
$RL_{TX-DIFF}$	Tx Differential Return Loss, including package and silicon	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
RL_{TX-CM}	Tx Common Mode Return Loss, including package and silicon	50 MHz < freq < 2.5 GHz	6	—	—	dB
$Z_{TX-DIFF-DC}$	DC differential Impedance	—	—	—	120	Ω
$V_{TX-CM-AC-PP}$	Tx AC peak common mode voltage, peak-peak	—	—	—	150	mV, p-p
$I_{TX-SHORT}$	Transmitter short-circuit current	—	—	—	90	mA
$V_{TX-DC-CM}$	Transmitter DC common-mode voltage	—	0	—	1.2	V
$V_{TX-IDLE-DIFF-DC}$	Electrical Idle Output DC voltage	—	0	—	5	mV
$V_{TX-IDLE-DIFF-AC-p}$	Electrical Idle Differential Output peak voltage	—	—	—	20	mV
$V_{TX-RCV-DETECT}$	Voltage change allowed during Receiver Detect	—	—	—	600	mV
$T_{TX-IDLE-MIN}$	Min. time in Electrical Idle	—	20	—	—	ns
$T_{TX-IDLE-SET-TO-IDLE}$	Max. time from EI Order Set to valid Electrical Idle	—	—	—	8	ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Max. time from Electrical Idle to valid differential output	—	—	—	8	ns
$L_{TX-SKEW}$	Lane-to-lane output skew	—	—	—	500 + 4 UI	ps
Receive[2]						
UI	Unit Interval	—	199.94	200	200.06	ps
$V_{RX-DIFF-PP}$	Differential Rx peak-peak voltage	—	0.343	—	1.2	V, p-p
$T_{RX-RJ-RMS}$	Receiver random jitter tolerance (RMS)	1.5 MHz – 100 MHz Random noise	—	—	4.2	ps, RMS
T_{RX-DJ}	Receiver deterministic jitter tolerance	—	—	—	88	ps
$RL_{RX-DIFF}$	Receiver differential Return Loss, package plus silicon	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
RL_{RX-CM}	Receiver common mode Return Loss, package plus silicon	—	6	—	—	dB
Z_{RX-DC}	Receiver DC single ended impedance	—	40	—	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Receiver DC single ended impedance when powered down	—	200k	—	—	Ω
$V_{RX-CM-AC-P}$[3]	Rx AC peak common mode voltage	—	—	—	150	mV, peak

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
$V_{RX-IDLE-DET-DIFF-PP}$	Electrical Idle Detect Threshold	—	65	—	1753	mV, p-p
$L_{RX-SKEW}$	Receiver lane-lane skew	—	—	—	8	ns

Notes:

1. Refer to PCI Express Base Specification Revision 3.0 Table 4.18 test condition and requirement for respective parameters.
2. Refer to PCI Express Base Specification Revision 3.0 Table 4.24 test condition and requirement for respective parameters.
3. Spec compliant requirement.

3.28 SGMII Characteristics

3.28.1 SGMII Specifications

Over recommended operating conditions.

Table 3.47 SGMII

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
f_{DATA}	SGMII Data Rate	—	—	1250	—	MHz
f_{REFCLK}	SGMII Reference Clock Frequency (Data Rate / 10)	—	—	125	—	MHz
J_{TOL_DET}	Jitter Tolerance, Deterministic	Periodic jitter < 300 kHz		—	0.1[1]	UI
J_{TOL_TOL}	Jitter Tolerance, Total	Periodic jitter < 300 kHz		—	0.3[1]	UI
Δf/f	Data Rate and Reference Clock Accuracy	—	–300	—	300	ppm

Note:

1. J_{TOT} can meet the following jitter mask specifications:

- 0 to 3.5 kHz: 10 UI;
- 3.5 to 700 kHz: log-log slope 10 UI to 0.05 UI;
- above 700 kHz: 0.05 UI.

3.29 sysCONFIG Port Timing Specifications

Over recommended operating conditions.

Table 3.48 sysCONFIG Port Timing Specifications

Symbol	Parameter	Device	Min	Typ.	Max	Unit
Master SPI POR/REFRESH Timing						
t_{ICFG}	REFRESH command executed, to the rising edge of INITN	—	—	—	5	µs
t_{VMC}	Time from rising edge of INITN to the valid Master MCLK	—	—	—	5	µs
f_{MCLK_DEF}	Default MCLK frequency (Before MCLK frequency selection in bitstream)	—	—	3.5	—	MHz
t_{ICFG_POR}	Time during POR, from VCC, VCCAUX, VCCIO0, or VCCIO1 (whichever is the last) pass POR trip voltage, to the rising edge if INITN	—	—	—	5	ms
Slave SPI/ I²C /I3C POR/REFRESH Timing						
t_{MSPI_INH}	Time during POR, from VCC, VCCAUX, VCCIO0 or VCCIO1 (whichever is the last) pass POR trip voltage, or REFRESH command executed, to pull PROGRAMN LOW to prevent entering MSPI mode	—	—	—	1	µs
$t_{ACT\_PROGRAMN\_H}$	Minimum time driving PROGRAMN HIGH after last activation clock	—	50	—	—	ns
t_{CONFIG_CCLK}	Minimum time to start driving CCLK (SSPI) after PROGRAMN HIGH	—	50	—	—	ns
t_{CONFIG_SCL}	Minimum time to start driving SCL (I2C/I3C) after PROGRAMN HIGH	—	50	—	—	ns
PROGRAMN Configuration Timing						
$t_{PROGRAMN}$	PROGRAMN LOW pulse accepted	—	50	—	—	ns
$t_{PROGRAMN\_RJ}$	PROGRAMN LOW pulse rejected	—	—	—	25	ns
t_{INIT_LOW}	PROGRAMN LOW to INITN LOW	—	—	—	100	ns
t_{INIT_HIGH}	PROGRAMN LOW to INITN HIGH	—	—	40	—	µs
t_{DONE_LOW}	PROGRAMN LOW to DONE LOW	—	—	—	55	µs
t_{DONE_HIGH}	PROGRAMN HIGH to DONE HIGH	—	—	—	2	s
t_{IODISS}	PROGRAMN LOW to I/O Disabled	—	—	—	125	ns
Master SPI						
f_{MCLK1}	Max selected MCLK output frequency	—	—	112.5	124	MHz
f_{MCLK_DC}	MCLK output clock duty cycle	—	40	—	60	%
t_{MCLKH}	MCLK output clock pulse width HIGH	—	3.5	—	—	ns
t_{MCLKL}	MCLK output clock pulse width LOW	—	3.5	—	—	ns
t_{SU_MSI}	MSI to MCLK setup time	—	3	—	—	ns

Symbol	Parameter	Device	Min	Typ.	Max	Unit
t_{HD_MSI}	MSI to MCLK hold time	—	0.5	—	—	ns
t_{CO_MSO}	MCLK to MSO delay	—	—	—	12	ns
Slave SPI						
f_{CCLK}	CCLK input clock frequency	—	—	—	135	MHz
t_{CCLKH}	CCLK input clock pulse width HIGH	—	3.5	—	—	ns
t_{CCLKL}	CCLK input clock pulse width LOW	—	3.5	—	—	ns
t_{VMC_SLAVE}	Time from rising edge of INITN to Slave CCLK	—	50	—	—	ns
t_{VMC_MASTER}	CCLK input clock duty cycle	—	40	—	60	%
t_{SU_SSI}	SSI to CCLK setup time	—	3.2	—	—	ns
t_{HD_SSI}	SSI to CCLK hold time	—	1.9	—	—	ns
t_{CO_SSO}	CCLK falling edge to valid SSO output	—	—	—	30	ns
t_{EN_SSO}	CCLK falling edge to SSO output enabled	—	—	—	30	ns
t_{DIS_SSO}	CCLK falling edge to SSO output disabled	—	—	—	30	ns
t_{HIGH_SCSN}	SCSN HIGH time	—	74	—	—	ns
t_{SU_SCSN}	SCSN to CCLK setup time	—	3.5	—	—	ns
t_{HD_SCSN}	SCSN to CCLK hold time	—	1.6	—	—	ns
I^2C/I3C						
f_{SCL_I2C}	SCL input clock frequency for I^2C	—	—	—	1	MHz
f_{SCL_I3C}	SCL input clock frequency for I3C	—	—	—	12	MHz
t_{SCLH_I2C}	SCL input clock pulse width HIGH for I^2C	—	400	—	—	ns
t_{SCLL_I2C}	SCL input clock pulse width LOW for I^2C	—	400	—	—	ns
$t_{SU\_SDA\_I2C}$	SDA to SCL setup time for I^2C	—	250	—	—	ns
$t_{HD\_SDA\_I2C}$	SDA to SCL hold time for I^2C	—	50	—	—	ns
$t_{SU\_SDA\_I3C}$	SDA to SCL setup time for I3C	—	30	—	—	ns
$t_{HD\_SDA\_I3C}$	SDA to SCL hold time for I3C	—	30	—	—	ns
t_{CO_SDA}	SCL falling edge to valid SDA output	—	—	—	200	ns
t_{EN_SDA}	SCL falling edge to SDA output enabled	—	—	—	200	ns
t_{DIS_SDA}	SCL falling edge to SDA output disabled	—	—	—	200	ns
Wake-Up Timing						
t_{DONE_HIGH}	Last configuration clock cycle to DONE going HIGH	—	—	—	60	µs
t_{FIO_EN}	User I/O enabled in Fast I/O Mode	—	—	38.096	—	Mcycle
t_{IOEN}	Configure clock to user I/O enabled	—	150	—	—	ns
t_{MCLKZ}	Master MCLK to Hi-Z	—	—	—	2.5	µs

Note:

1. f_{MCLK} has a dependency on HFOSC and is 1/3 of fCLKHF.

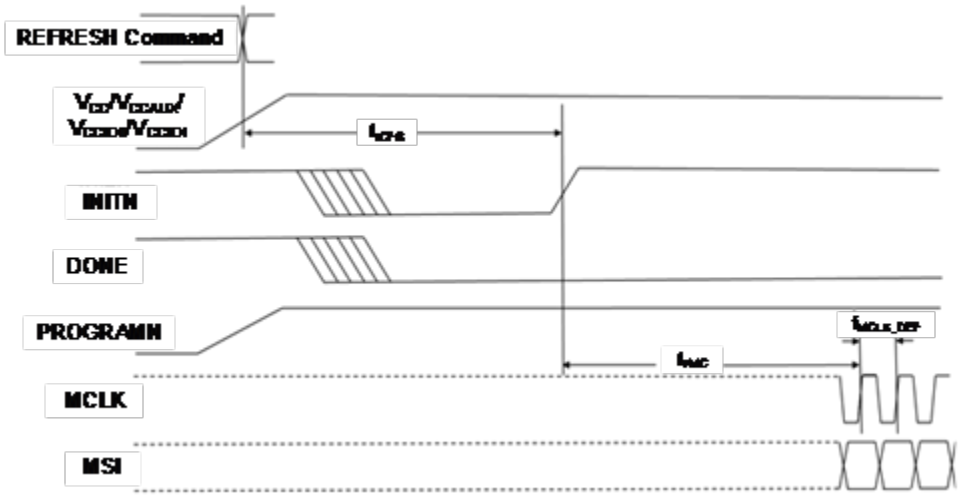


Figure 3.14. Master SPI POR/REFRESH Timing

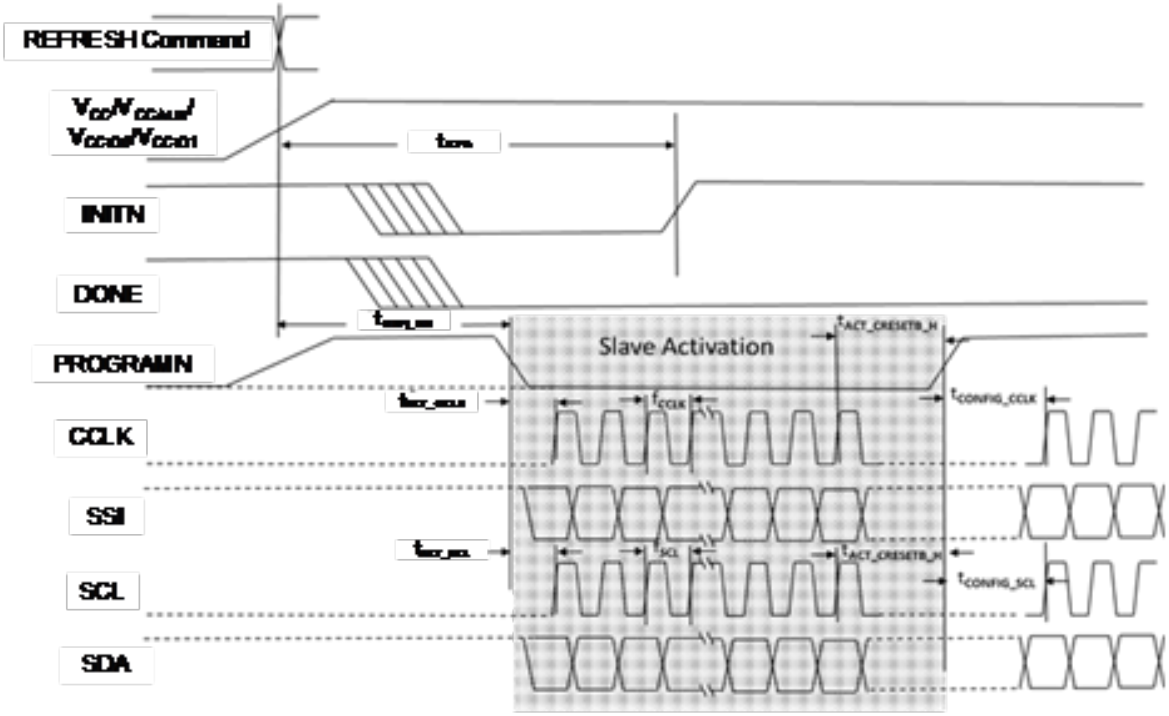


Figure 3.15. Slave SPI/ I²C /I3C POR/REFRESH Timing

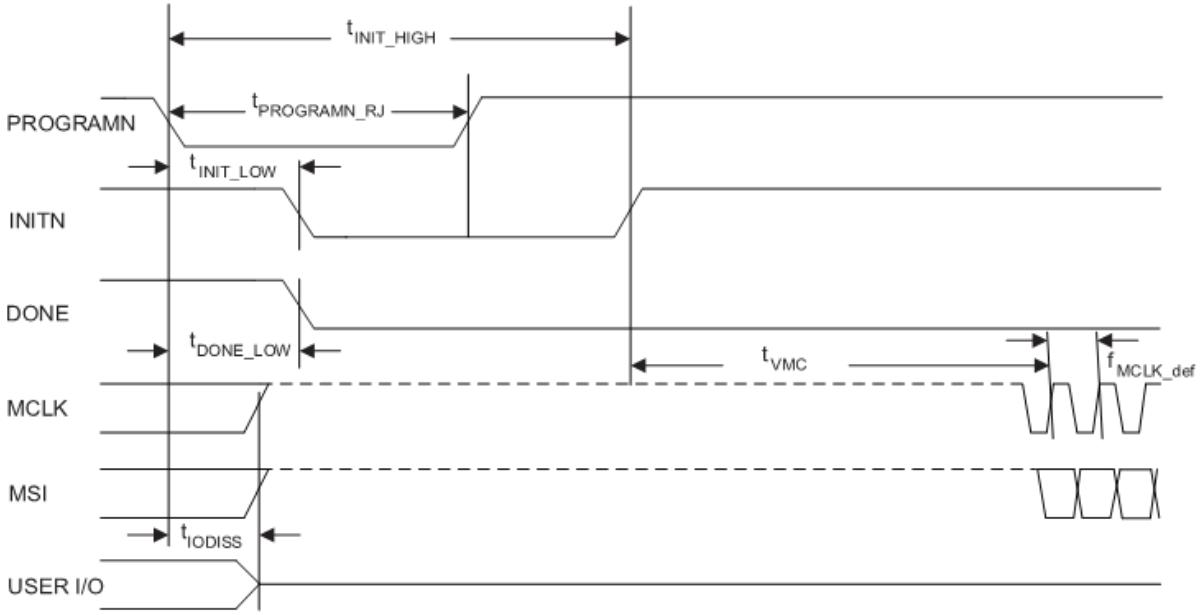


Figure 3.16. Master SPI PROGRAMN Timing

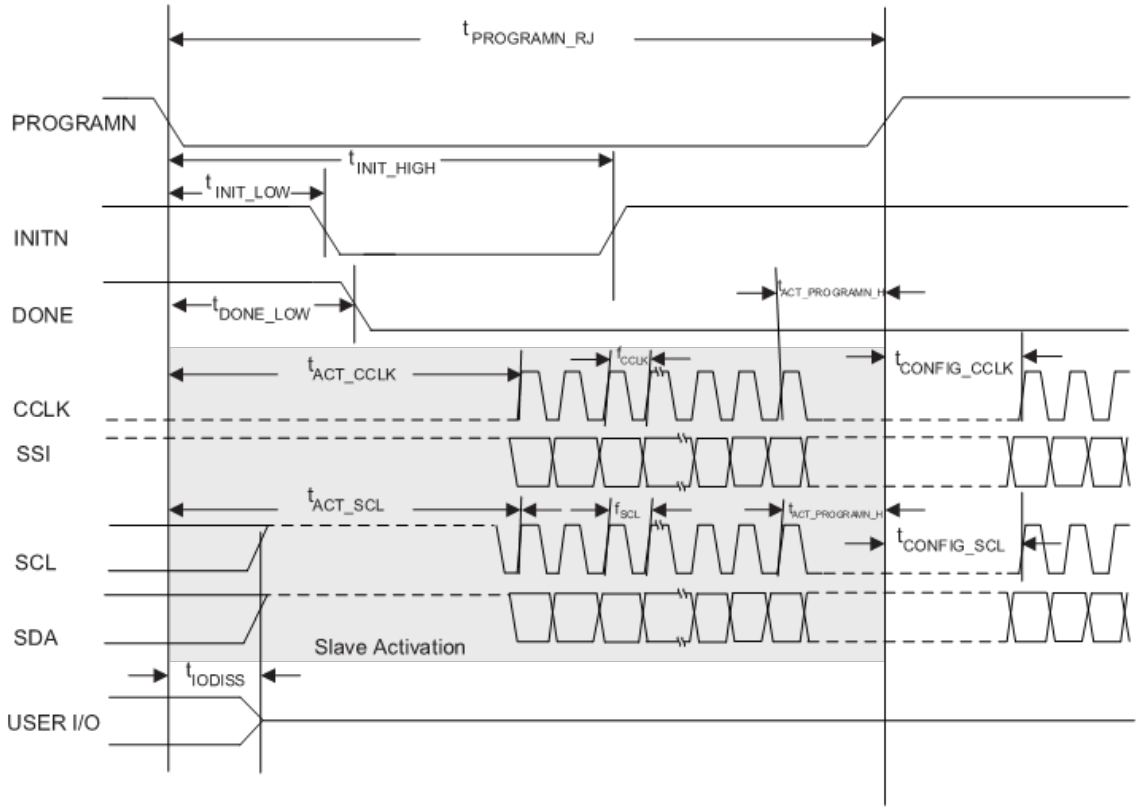


Figure 3.17. Slave SPI/ I²C /I3C PROGRAMN Timing

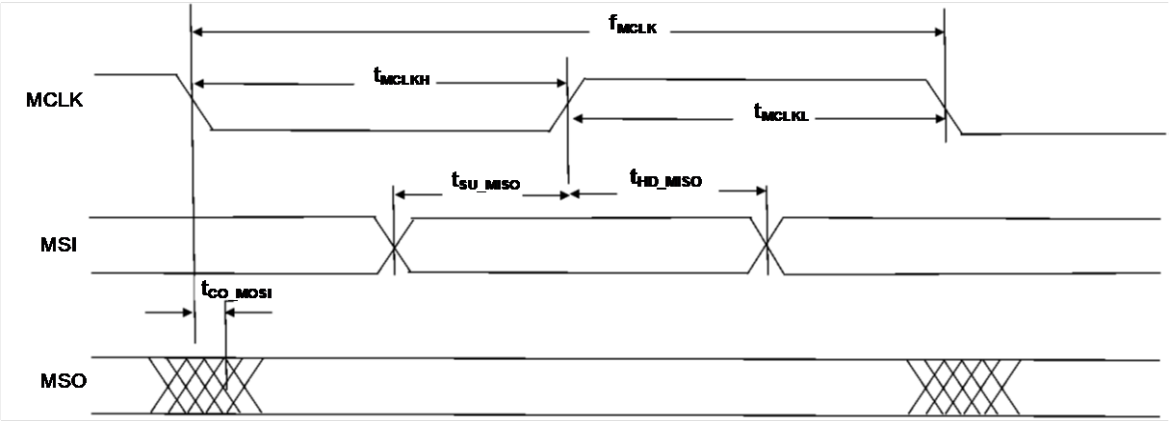


Figure 3.18. Master SPI Configuration Timing

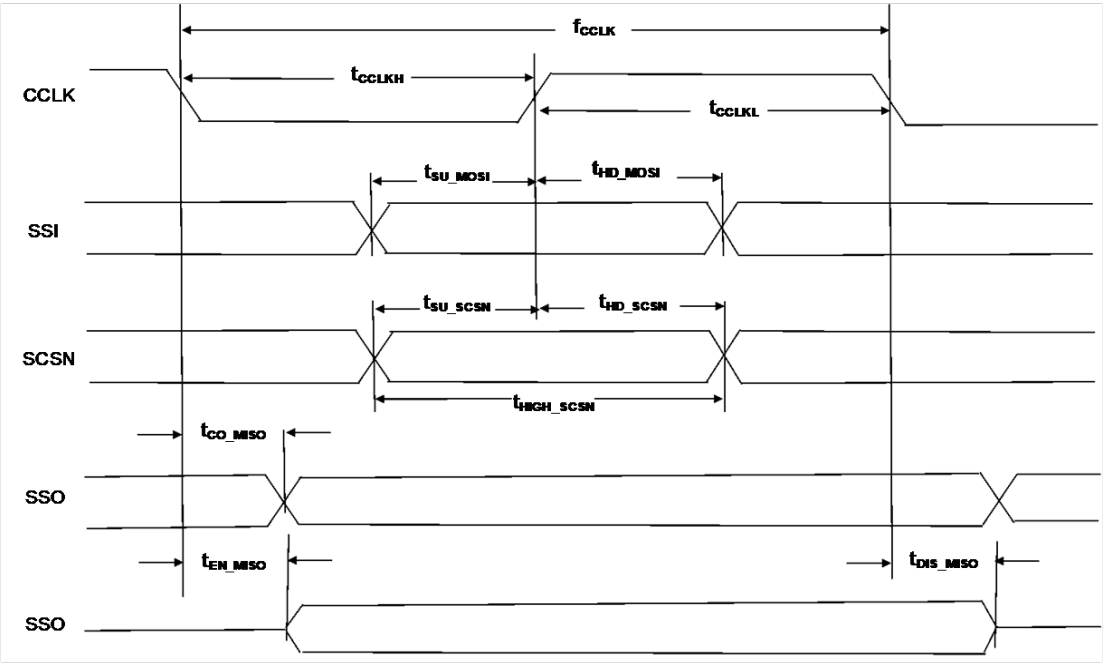


Figure 3.19. Slave SPI Configuration Timing

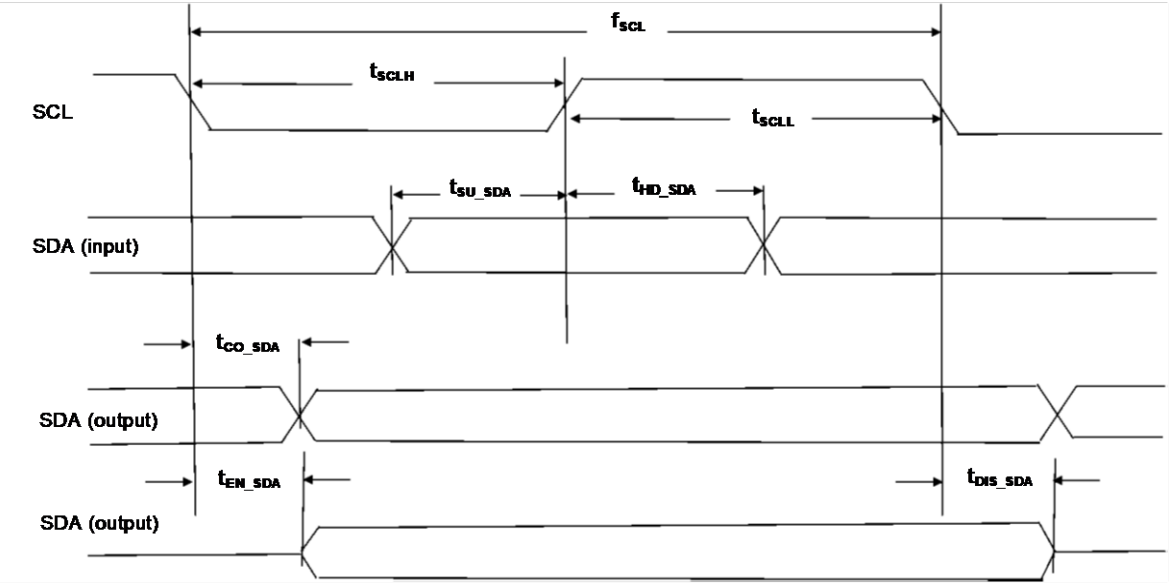


Figure 3.20. I²C /I3C Configuration Timing

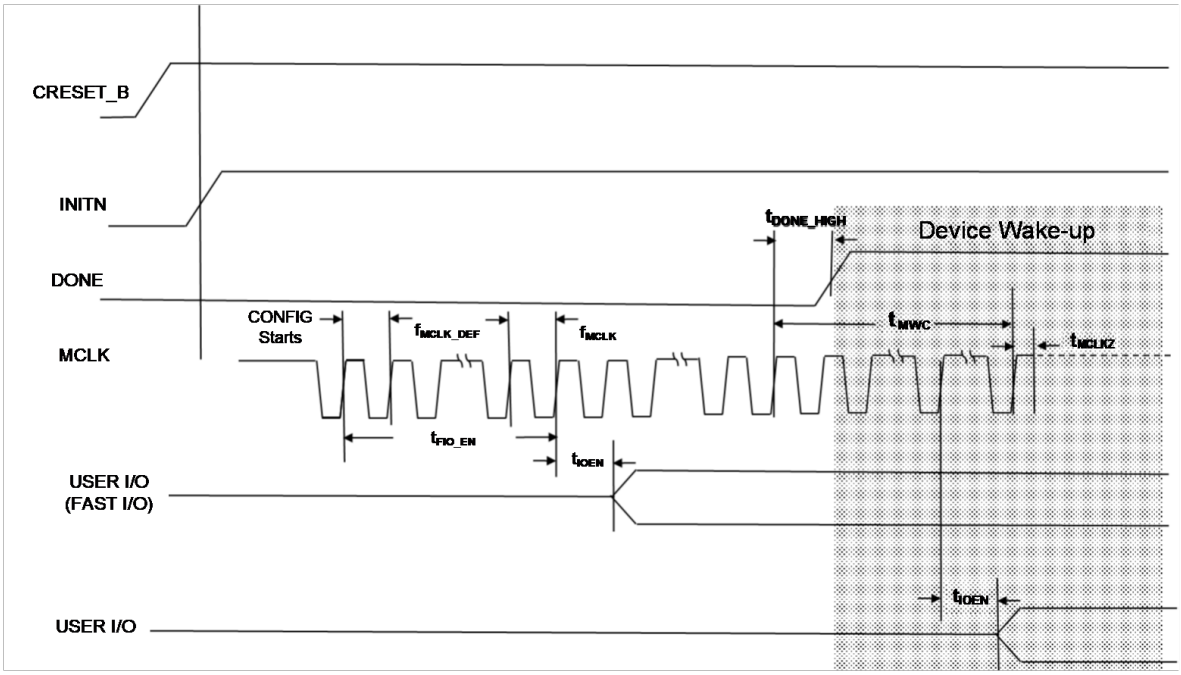


Figure 3.21. Master SPI Wake-Up Timing

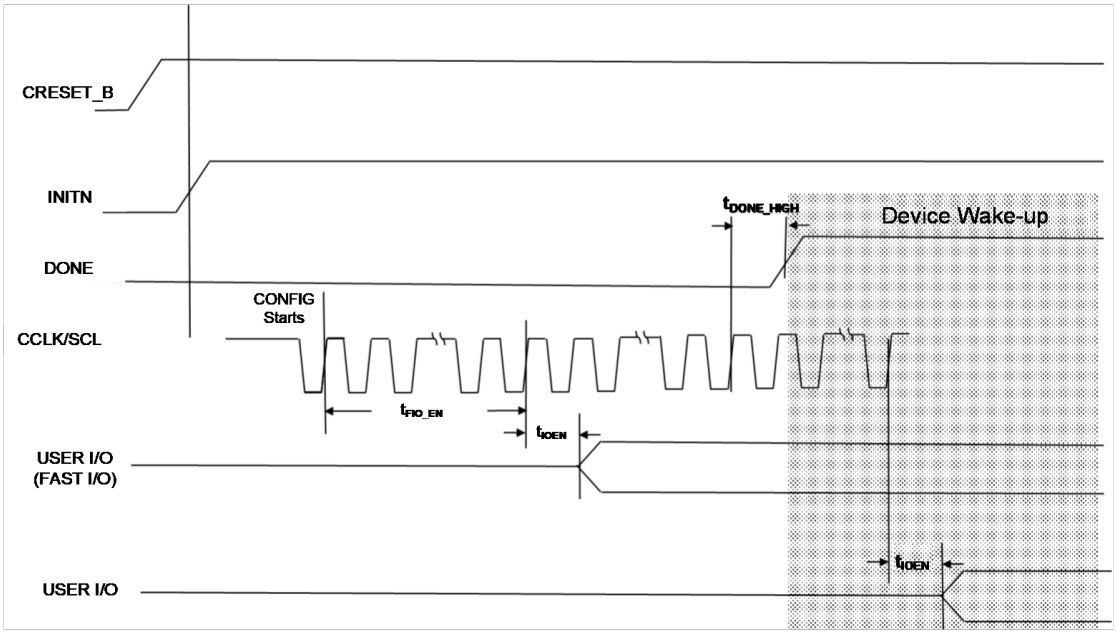


Figure 3.22. Slave SPI/ I²C /I3C Wake-Up Timing

3.30 JTAG Port Timing Specifications

Over recommended operating conditions.

Table 3.49 JTAG Port Timing Specifications

Symbol	Parameter	Min	Typ.	Max	Unit
f_{MAX}	TCK clock frequency	—	—	25	MHz
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	—	ns
t_{BTS}	TCK [BSCAN] setup time	5	—	—	ns
t_{BTH}	TCK [BSCAN] hold time	5	—	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time[1]	100	—	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	—	14	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	—	14	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	—	14	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	—	25	ns

Note:

1. Based on default I/O setting of slow slew rate.

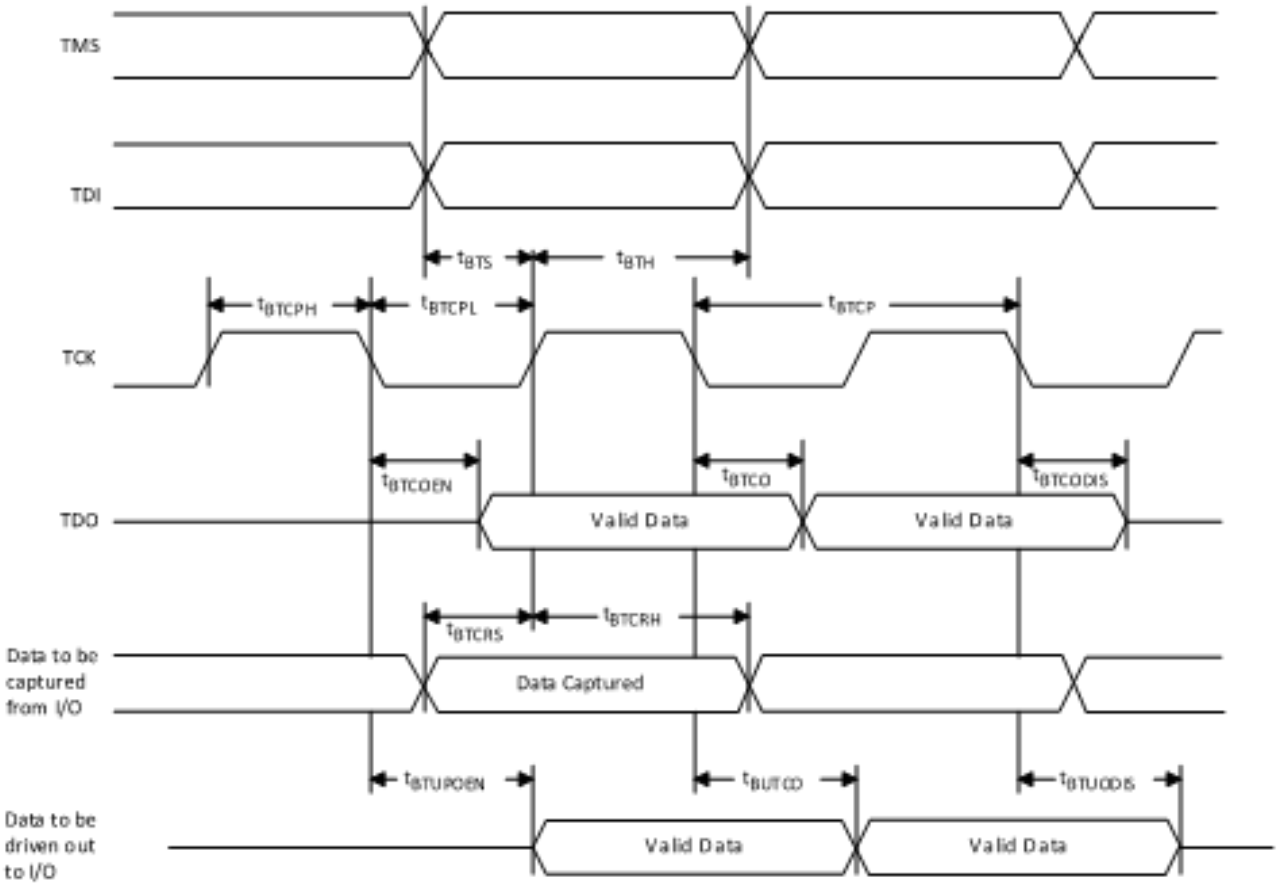


Figure 3.23. JTAG Port Timing Waveforms

3.31 Switching Test Conditions

Figure 3.24 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 3.50.

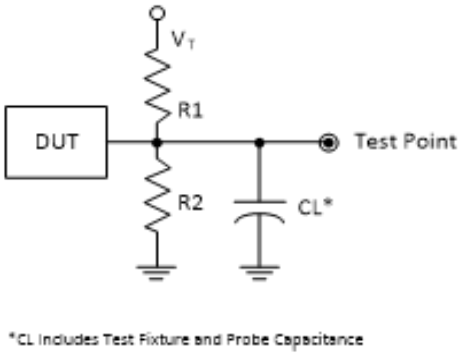


Figure 3.24. Output Test Load, LVTTL and LVCMOS Standards

Table 3.50 Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R1	R2	CL	Timing Ref.	VT
LVTTL and other LVCMOS settings (L ≥ H, H ≥ L)	▪	▪	0 pF	LVCMOS 3.3 = 1.5 V	—
				LVCMOS 2.5 = V_{CCIO}/2	—
				LVCMOS 1.8 = V_{CCIO} /2	—
				LVCMOS 1.5 = V_{CCIO} /2	—
				LVCMOS 1.2 = V_{CCIO} /2	—
LVCMOS 2.5 I/O (Z ≥ H)	▪	1 MΩ	0 pF	V_{CCIO} /2	—
LVCMOS 2.5 I/O (Z ≥ L)	1 MΩ	▪	0 pF	V_{CCIO} /2	V_{CCIO}
LVCMOS 2.5 I/O (H ≥ Z)	▪	100	0 pF	V_{OH} – 0.10	—
LVCMOS 2.5 I/O (L ≥ Z)	100	▪	0 pF	V_{OL} + 0.10	V_{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

4. Pinout Information

4.1 Signal Descriptions

Signal Name	Bank	Type	Description
Power and GND			
V_{SS}	—	GND	Ground for internal FPGA logic and I/O.
V_{SSSD}	—	GND	Ground for the SerDes block.
V_{SSADC}	—	GND	Ground for ADC block.
$V_{CC, VCCECLK}$	—	Power	Power supply pins for core logic. VCC is connected to 1.0 V (nom.) supply voltage. Power On Reset (POR) monitors this supply voltage.
V_{CCAUXA}	—	Power	Auxiliary power supply pin for internal analog circuitry. This supply is connected to 1.8 V (nom.) supply voltage. POR monitors this supply voltage.
V_{CCAUX}	—	Power	Auxiliary power supply pin for I/O Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7. This supply is connected to 1.8 V (nom.) supply voltage, and is used for generating stable drive current for the I/O.
$V_{CCAUXHx}$	3–5	Power	Auxiliary power supply pin for I/O Bank 3, Bank 4, and Bank 5. This supply is connected to 1.8 V (nom.) supply voltage, and is used for generating stable current for the differential input comparators and stable drive current for the I/O.
V_{CCIOx}	0–7	Power	Power supply pins for I/O bank x. For x = 0, 1, 2, 6, and 7, VCCIO can be connected to (nom.) 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V. For x = 3, 4, and 5, VCCIO can be connected to (nom.) 1.0 V, 1.2 V, 1.35 V, 1.5 V, or 1.8 V. There are dedicated and shared configuration pins in Bank 0 and Bank 1. POR monitors these banks supply voltages.
$V_{CCADC18}$	—	Power	1.8 V (nom.) power supply for the ADC block.
V_{CCSDx}	—	Power	1.0 V (nom.) power supply for the SerDes block.
V_{CCSDCK}	—	Power	1.0 V (nom.) power supply for SerDes clock buffer.
$V_{CCPLLSDx}$	—	Power	1.8 V (nom.) power supply for the PLL in the SerDes block.
$V_{CCAUXSDQx}$	—	Power	1.8 V (nom.) auxiliary power supply for the SerDes block.
Dedicated Pins			
Dedicated Configuration I/O Pin			
JTAG_EN	1	Input	LVCMOS input pin. This input selects the JTAG shared GPIO to be used for JTAG 0 = GPIO 1 = JTAG
Dedicated ADC I/O Pins			
ADC_REFA, ADC_REFB	—	Input	ADC reference voltage, for each of the two ADC converters. If not used, tie to ground.
ADC_DP/NA, ADC_DP/NB	—	Input	Dedicated ADC input pairs, for each of the two ADC converters. If not used, tie to ground.
Dedicated SerDes I/O Pins			
SDx_RXDP/N	—	Input	SerDes data differential input pairs.
SDx_TXDP/N	—	Output	SerDes data differential output pairs.

Signal Name	Bank	Type	Description
SDQy_REFCLKP/N	—	Input	SerDes reference clock differential input pairs for Quad y.
SD_EXTy_REFCLKP/N	—	Input	Shared SerDes external reference clock input pairs.
SDx_REXT	—	Input	SerDes external reference resistor input. Resistor connects between to this pin and SDx_REFRET pin. This is used to adjust the on-chip differential termination impedance, based on the external resistance value: REXT = 909 Ω, RDIFF = 80 Ω REXT = 976 Ω, RDIFF = 85 Ω REXT = 1.02 kΩ, RDIFF = 90 Ω REXT = 1.15 kΩ, RDIFF = 100 Ω
SDx_REFRET	—	Input	SerDes reference return input. These pins should be AC coupled to the VCCPLLSDx supply.
Misc Pins			
NC		—	No connect.
RESERVED		—	This pin is reserved and should not be connected to anything on the board.
General Purpose I/O Pins			
P[T/B/L/R] [Number]_[A/B]	T = 0 R = 1, 2 B = 3, 4, 5 L = 6. 7	Input, Output, Bi-Dir	Programmable User I/O: [T/B/L/R] indicates the package pin/ball is in: T (Top), B (Bottom), L (Left), or R (Right) edge of the device. [Number] identifies the PIO [A/B] pair. [A/B] shows the package pin/ball is A or B signal in the pair. PIOs A and B are grouped as a pair. Each A/B pair in the bottom banks supports true differential input and output buffers. When configured as differential input, differential termination of 100 Ω can be selected. Each A/B pair in the top, left and right banks does not support true differential input or output buffer. It supports all single-ended inputs and outputs, and can be used for emulated differential output buffer. Some of these user-programmable I/O are used during configuration, depending on the configuration mode. You need to make appropriate connection on the board to isolate the two different functions before/after configuration. Some of these user-programmable I/O are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/O for user logic. During configuration, the user-programmable I/O are tri-stated with an internal weak pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tri-stated and defaults to have weak pull-down enabled after configuration.

Signal Name	Bank	Type	Description
Shared Configuration Pins [1, 2] 1. These pins can be used for configuration during configuration mode. When configuration is completed, these pins can be used as GPIO, or shared function in GPIO. When these pins are used in dual function, you need to isolate the signal paths for the dual functions on the board. 2. The pins used are defined by the configuration modes detected. Slave SPI or I^2C /I3C modes are detected during slave activation. Pins that are not used in the selected configuration mode are tri-stated during configuration, and can connect directly as GPIO in user function.			
PRxxx/SDA/USER_SDA	1	Input, Output, Bi-Dir	Configuration: I^2C /I3C Mode: SDA signal User Mode: PRxxx: GPIO User_SDA: SDA signal for I^2C /I3C interface
PRxxx/SCL/USER_SCL	1	Input, Output, Bi-Dir	Configuration: I^2C /I3C Mode: SCL signal User Mode: PRxxx: GPIO User_SDA: SCL signal for I^2C /I3C interface
PRxxx/TDO/SSO	1	Input, Output, Bi-Dir	Configuration: Slave SPI Mode: Slave serial output User Mode: PRxxx: GPIO TDO: When JTAG_EN = 1, used as TDO signal for JTAG
PRxxx/TDI/SSI	1	Input, Output, Bi-Dir	Configuration: Slave SPI Mode: Slave serial input User Mode: PRxxx: GPIO TDI: When JTAG_EN = 1, used as TDI signal for JTAG
PRxxx/TMS/SCSN	1	Input, Output, Bi-Dir	Configuration: Slave SPI Mode: Slave chip select User Mode: PRxxx: GPIO TMS: When JTAG_EN = 1, used as TMS signal for JTAG
PRxxx/TCK/SCLK	1	Input, Output, Bi-Dir	Configuration: Slave SPI Mode: Slave clock input User Mode: PRxxx: GPIO TCK: When JTAG_EN = 1, used as TCK signal for JTAG
PTxxx/MCSNO	0	Input, Output, Bi-Dir	Configuration: Master SPI Mode: Chip select output User Mode: PTxxx: GPIO
PTxxx/MD3	0	Input, Output, Bi-Dir	Configuration: Master Quad SPI Mode: I/O3 User Mode: PTxxx: GPIO
PTxxx/MD2	0	Input, Output, Bi-Dir	Configuration: Master Quad SPI Mode: I/O2 User Mode:

Signal Name	Bank	Type	Description
			PTxxx: GPIO
PTxxx/MSI/MD1	0	Input, Output, Bi-Dir	Configuration: Master SPI Mode: Master serial input Master Quad SPI Mode: I/O1 User Mode: PTxxx: GPIO
PTxxx/MSO/MD0	0	Input, Output, Bi-Dir	Configuration: Master SPI Mode: Master serial output Master Quad SPI Mode: I/O0 User Mode: PTxxx: GPIO
PTxxx/MCSN/PCLKT0_1	0	Input, Output, Bi-Dir	Configuration: Master SPI Mode: Master chip select output User Mode: PTxxx: GPIO PCLKT0_0: Top PCLK input
PTxxx/MCLK/PCLKT0_0	0	Input, Output, Bi-Dir	Configuration: Master SPI Mode: Master clock output User Mode: PTxxx: GPIO PCLKT0_1: Top PCLK input
PTxxx/PROGRAMN	0	Input, Output, Bi-Dir	Configuration: PROGRAMN: Initiate configuration sequence when asserted LOW. User Mode: PTxxx: GPIO
PTxxx/INITN	0	Input, Output, Bi-Dir	Configuration: INITN: Open Drain I/O pin. This signal is driven to LOW when configuration sequence is started, to indicate the device is in initialization state. This signal is released after the initialization is completed, and the configuration download can start. You can keep driving this signal LOW to delay configuration download to start. User Mode: PTxxx: GPIO
PTxxx/DONE	0	Input, Output, Bi-Dir	Configuration: DONE: Open Drain I/O pin. This signal is driven to LOW during configuration time. It is released to indicate the device has completed configuration. You can keep driving this signal LOW to delay the device to wake up from configuration. User Mode: PTxxx: GPIO

Shared User GPIO Pins [1, 2, 3, 4]

1. Shared User GPIO pins are pins that can be used as GPIO, or functional pins that connect directly to specific functional blocks, when device enters into User Mode.
2. Declaring on assigning the pin as GPIO or specific functional pin is done by configuration bitstream, except JTAG pins.
3. JTAG pins are controlled by JTAG_EN signal. When JTAG_EN = 1, the pins are used for JTAG interface. When JTAG = 0, the pins are used as GPIO or specific functional pin defined by configuration bitstream.
4. Refer to package pin file.

Signal Name	Bank	Type	Description
Shared JTAG Pins			
PRxxx/TDO/ yyyy	1	Input, Output, Bi-Dir	User Mode: PRxxx: GPIO TDO: When JTAG_EN = 1, used as TDO signal for JTAG. yyyy: Other possible selectable specific functional pin.
PRxxx/TDI/yyyy	1	Input, Output, Bi-Dir	User Mode: PRxxx: GPIO TDI: When JTAG_EN = 1, used as TDI signal for JTAG. yyyy: Other possible selectable specific functional pin.
PRxxx/TMS/ yyyy	1	Input, Output, Bi-Dir	User Mode: PRxxx: GPIO TMS: When JTAG_EN = 1, used as TMS signal for JTAG. yyyy: Other possible selectable specific functional pin.
PRxxx/TCK/ yyyy	1	Input, Output, Bi-Dir	User Mode: PRxxx: GPIO TCK: When JTAG_EN = 1, used as TCK signal for JTAG. Yyyy: Other possible selectable specific functional pin.
Shared CLOCK Pins [1] 1. Some PCLK pins can also be used as GPLL reference clock input pin. Refer to sysCLOCK PLL Design and Usage Guide for Nexus Platform (FPGA-TN-02095).			
PBxxx/PCLK[T,C][3,4,5]_[0-3]/yyyy	3, 4, 5	Input, Output, Bi-Dir	User Mode: PBxxx: GPIO PCLK: Primary clock or GPLL Refclk signal. [T,C] = True/Complement when using differential signaling. [3,4,5] = Bank [0-3] Up to 4 signals in the bank. yyyy: Other possible selectable specific functional pin.
PTxxx/PCLKT0_[0-1]/yyyy	0	Input, Output, Bi-Dir	User Mode: PTxxx: GPIO PCLKT: Primary clock or GPLL Refclk signal (only single-ended). [0-1] Up to two signals in the bank. yyyy: Other possible selectable specific functional pin.
PRxxx/PCLKT[1,2]_[0-2]/yyyy	1, 2	Input, Output, Bi-Dir	User Mode: PRxxx: GPIO PCLKT: Primary clock or GPLL Refclk signal (only single-ended). [0-2] Up to three signals in the bank. yyyy: Other possible selectable specific functional pin.
PLxxx/PCLKT[6,7]_[0-2]/yyyy	6, 7	Input, Output, Bi-Dir	User Mode: PLxxx: GPIO PCLKT: Primary Clock or GPLL Refclk signal (only single-ended). [0-2] Up to three signals in the bank. yyyy: Other possible selectable specific functional pin.
PBxxx/LRC_GPLL[T,C]_IN/yyyy	3	Input, Output, Bi-Dir	User Mode: PBxxx: GPIO LRC_GPLL: Lower Right GPLL Refclk signal (PLLCK). [T,C] = True/Complement when using differential signaling. yyyy: Other possible selectable specific functional pin.

Signal Name	Bank	Type	Description
PBxxx/LLC_GPLL[T,C]_IN/yyyy	5	Input, Output, Bi-Dir	User Mode: PBxxx: GPIO LLC_GPLL: Lower Left GPLL Refclk signal (PLLCK). [T,C] = True/Complement when using differential signaling. yyyy: Other possible selectable specific functional pin.
PLxxx/ULC_GPLLT_IN/yyyy	7	Input, Output, Bi-Dir	User Mode: PLxxx: GPIO ULC_GPLL: Upper Left GPLL Refclk signal (only single-ended) (PLLCK). yyyy: Other possible selectable specific functional pin.
PRxxx/URC_GPLLT_IN/yyyy	1	Input, Output, Bi-Dir	User Mode: PRxxx: GPIO URC_GPLL: Upper Right GPLL Refclk signal (Only Single Ended) (PLLCK). yyyy: Other possible selectable specific functional.
PRxxx/yyyy	1	Input, Output, Bi-Dir	User Mode: PRxxx: GPIO yyyy: Other possible selectable specific functional pin.
Shared VREF Pins			
PBxxx/VREF[3,4,5]_[1-2]/yyyy	3, 4, 5	Input, Output, Bi-Dir	User Mode: PBxxx: GPIO VREF: Reference voltage for DDR memory function. [3,4,5] = Bank [1-2] Up to VREFs for each bank. yyyy: Other possible selectable specific functional pin.
Shared ADC Pins			
PBxxx/ADC_C[P,N]nn/yyyy	3, 4, 5	Input, Output, Bi-Dir	User Mode: PBxxx: GPIO ADC_C: ADC channel inputs. [P,N] = Positive or Negative input. nn = ADC Channel number (0 – 15). yyyy: Other possible selectable specific functional pin.
Shared Comparator Pins			
PBxxx/COMP[1-3][P,N]/yyyy	3, 5	Input, Output, Bi-Dir	User Mode: PBxxx: GPIO COMP: Differential comparator input. [P,N] = Positive or Negative input. [1-3] = Input to comparators 1-3. yyyy: Other possible selectable specific functional pin.
Shared SGMII Pins			
PBxxx/SGMII_RX[P,N][0-1]/yyyy	3, 5	Input, Output, Bi-Dir	User Mode: PBxxx: GPIO SGMII_RX: Differential SGMII RX input. [P,N] = Positive or Negative input. [0-1] = Input to SGMII RX0 or RX1 yyyy: Other possible selectable specific functional pin.

Note: Not all signals are available as external pins in all packages. Refer to the Pinout List file for various package details.

4.2 CertusPro-NX-RT Pin Information Summary

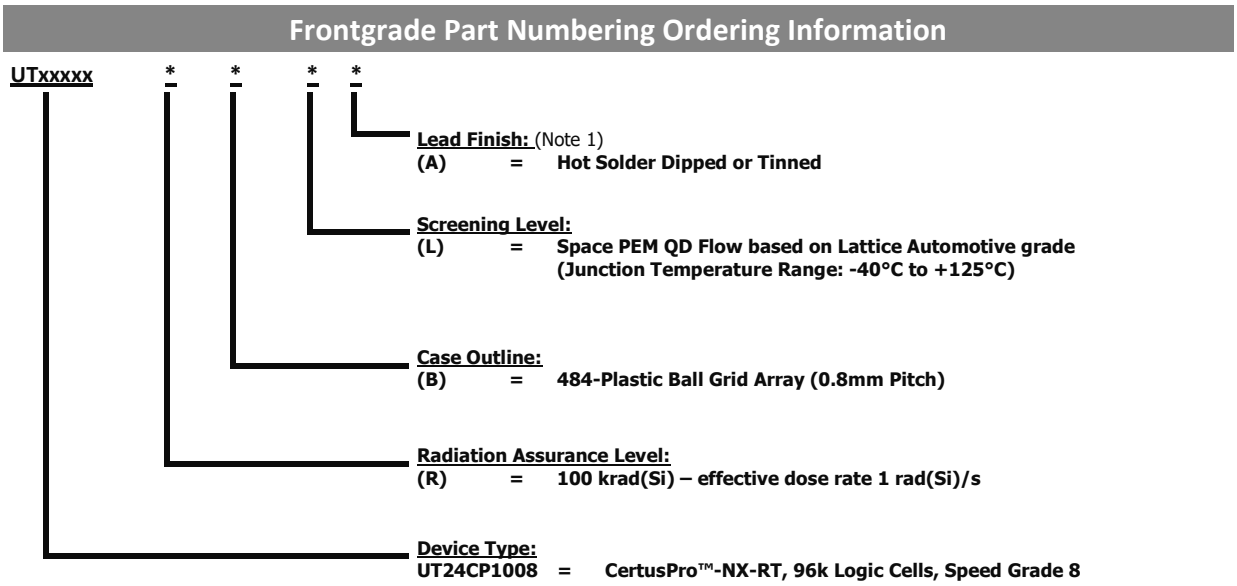
Pin Information Summary		LFCPNX-100
		BBG484
General Purpose Inputs/Outputs per Bank	Bank 0	24
	Bank 1	39
	Bank 2	32
	Bank 3	48
	Bank 4	48
	Bank 5	36
	Bank 6	32
	Bank 7	40
Total Single-Ended User I/O		299
Differential Input / Output Pairs	Bank 0	12
	Bank 1	19
	Bank 2	16
	Bank 3	24
	Bank 4	24
	Bank 5	18
	Bank 6	16
	Bank 7	20
Total Differential I/O		149
$V_{CC, VCCECLK}$		10
V_{CCAUXA}		1
V_{CCAUX}		2
$V_{CCAUXHx}$		3
$V_{CCAUXSDQx}$		2
V_{CCIO}	Bank 0	1
	Bank 1	2
	Bank 2	1
	Bank 3	3
	Bank 4	3
	Bank 5	2
	Bank 6	1
	Bank 7	2
V_{CCSDx}		9
$V_{CCPLLSDx}$		8
$V_{CCADC18}$		1
Total Power Pins		51
V_{SS}		23

Pin Information Summary		LFCPNX-100
		BBG484
V_{SSADC}		1
V_{SSSDQ}		47
Total GND Pins		71
Dedicated ADC Channels (pairs)		2
Dedicated ADC Reference Voltage Pins		2
Dedicated SerDes Pins		56
JTAGEN		1
NC		0
RESERVED		0
Total Dedicated Pins		63
Shared Configuration Pins	Bank 0	10
	Bank 1	6
	Bank 2	0
	Bank 3	0
	Bank 4	0
	Bank 5	0
	Bank 6	0
	Bank 7	0
Shared JTAG Pins	Bank 0	0
	Bank 1	4
	Bank 2	0
	Bank 3	0
	Bank 4	0
	Bank 5	0
	Bank 6	0
	Bank 7	0
Shared PCLK Pins	Bank 0	2
	Bank 1	3
	Bank 2	3
	Bank 3	8
	Bank 4	8
	Bank 5	8
	Bank 6	3
	Bank 7	3
Shared GPLL Pins	Bank 0	2
	Bank 1	0
	Bank 2	0
	Bank 3	2
	Bank 4	0

Pin Information Summary		LFCPNX-100
		BBG484
	Bank 5	2
	Bank 6	0
	Bank 7	2
Shared VREF Pins	Bank 0	0
	Bank 1	0
	Bank 2	0
	Bank 3	2
	Bank 4	2
	Bank 5	2
	Bank 6	0
	Bank 7	0
Shared ADC Channels (pairs)	Bank 0	0
	Bank 1	0
	Bank 2	0
	Bank 3	8
	Bank 4	4
	Bank 5	4
	Bank 6	0
	Bank 7	0
Shared Comparator Channels (pairs)	Bank 0	0
	Bank 1	0
	Bank 2	0
	Bank 3	3
	Bank 4	0
	Bank 5	3
	Bank 6	0
	Bank 7	0
Shared SGMII Channels (pairs)	Bank 0	0
	Bank 1	0
	Bank 2	0
	Bank 3	0
	Bank 4	0
	Bank 5	2
	Bank 6	0
	Bank 7	0

5. Ordering Information

Ordering Information



NOTES: Frontgrade Space PEM QD devices only (based on Lattice Automotive grade)

Lattice Semiconductor has published Product Change Notices (PCN) 01A-23 and 01B-23 indicating that an issue has been identified and documented in the Automotive grade wafer/die currently used in Frontgrade's UT24CP1008 CertusProTM-NX-RT FPGA.

Refer to https://www.latticesemi.com/Support/PCN.aspx to download the subject PCNs.

The issue identified pertains to SERDES functional capability limitation when channel 3 of either of the two SERDES Quads in the device is used and the PMA clock divider is set to >=2.

Lattice Semiconductor intends to utilize an alternate qualified mask set on future versions of the wafer/die.

Future UT24CP1008 device product versions/Lot IDs may utilize either of the qualified mask sets.

If you currently use UT24CP1008 AND utilize Channel 3 with PMA clock divider >=2, please contact Frontgrade to determine availability of future versions/Lot ID of the UT24CP1008 with the new mask set.

UT24CP1008 device product versions marked with Lot ID = B3112T03 (shown in diagrams below) are affected by this limitation.

Device Identification

(example to show ID location)

Device Marking

(example to show ID location)

References

For more information, refer to the following documents:

- sysCLOCK PLL Design and Usage Guide for Nexus Platform (FPGA-TN-02095)
- sysDSP Usage Guide for Nexus Platform (FPGA-TN-02096)
- sysCONFIG Usage Guide for Nexus Platform (FPGA-TN-02099)
- CertusPro-NX SerDes/PCS Usage Guide (FPGA-TN-02245)
- sysI/O Usage Guide for Nexus Platform (FPGA-TN-02067)
- Soft Error Detection (SED)/Correction (SEC) Usage Guide for Nexus Platform (FPGA-TN-02076)
- Memory Usage Guide for Nexus Platform (FPGA-TN-02094)
- ADC Usage Guides for Nexus Platform (FPGA-TN-02129)
- CertusPro-NX High-Speed I/O Interface (FPGA-TN-02244)
- Power Management and Calculation for CertusPro-NX Devices (FPGA-TN-02257)
- CertusPro-NX 50k Pinout File (FPGA-SC-02023)
- CertusPro-NX 100k Pinout File (FPGA-SC-02022)
- Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039)
- sub-LVDS Signaling Using Lattice Devices (FPGA-TN-02028)
- Multi-Boot Usage Guide for Nexus Platform (FPGA-TN-02145)
- I^2C Hardened IP Usage Guide for Nexus Platform (FPGA-TN-02142)

For package information, refer to the following documents:

- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- Solder Reflow Guide for Surface Mount Devices (FPGA-TN-02041)
- Thermal Management (FPGA-TN-02044)
- Package Diagrams (FPGA-DS-02053)
- High-Speed PCB Design Considerations (FPGA-TN-02148)
- Advanced Configuration Security Usage Guide for Nexus Platform (FPGA-TN-02176)
- CertusPro-NX Hardware Checklist (FPGA-TN-02255)

For further information on interface standards, refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL) – www.jedec.org
- PCI – www.pcisig.com

Revision History

Date	Revision #	Author	Change Description	Page #
02/27/2023	2.0.0	--	Initial Release.	
06/30/23	2.0.1 (JGB)	JGB	Initial Release in Frontgrade template format. Section 6.2 removed to eliminate industrial proto offering. Fixed header to: CertusPro-NX-RT. Removed all references to SerDes speeds above 6.25Gbps. Removed all references to flip chip package.	
12/5/23	2.0.2 (JGB)	JGB	Add language to the effect "Lot date code subject to Lattice's PCN 01A-23 and PCN 01B-23": • Ordering table section of datasheet • SERDES section 2.21 of this datasheet Updated notes and tables in section 3 to document scope of parameter tests for Frontgrade device.	

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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The following United States (U.S.) Department of Commerce statement shall be applicable if these commodities, technology, or software are exported from the U.S.: These commodities, technology, or software were exported from the United States in accordance with the Export Administration Regulations. Diversion contrary to U.S. law is prohibited.