DATASHEET

Smart Power Switch Controller

UT05PFD103

Case Temperature	Radiation Immunity
-55°C to +125°C	TID >300k rad(Si) SEL immune < 100 MeV-cm^2/mg SEU Rate < 1E-10 errors/b-d SET onset > 37 MeV-cm^2/mg

1 Features

- 4.5V-5.5V eFUSE Power Switch Controller
- Source Power Switching with Inrush current limiting
- Forward Overcurrent and Short Circuit Protection
  - <500ns typical short circuit break response
- Optional OR_FET with Reverse Current Protection
- Line and Load Side Voltage Monitor and Protection
- Optional Digital Voltage and Current Telemetry
  - 10-bit VIN/VOUT/IDS Telemetry (via PMBus™)
- Latching/Retriggerable/Pulsing Power FET Control
- Package Options:
  - 47-Lead Dual Flatpack
  - 16.1 x 10.75 mm, 0.635 mm pitch
  - Mass = 2.3gm
- Standard Microcircuit Drawing: 5962-20215

2 Introduction

The UT05PFD103 Smart Power Switch Controller (SPSC) is an intelligent PowerMOSFET controller with load-side inrush current limiting and eFuse protection of current faults. An optional Ideal Diode (OR FET) facilitates redundant power architectures such as uninterruptable power supplies. The SPSC accommodates protection of the PowerFET SOA while providing flexible power switching control for a wide range of space applications.

3 Applications

- 5V Power Distribution with Short Circuit Protection
- SpaceVPX – SpaceUM VS3 (+5V) Power Switching
- Subsystem Power Electronics Input Switching
- 5V Uninterruptable Power Supplies
- SEL Fault Protection

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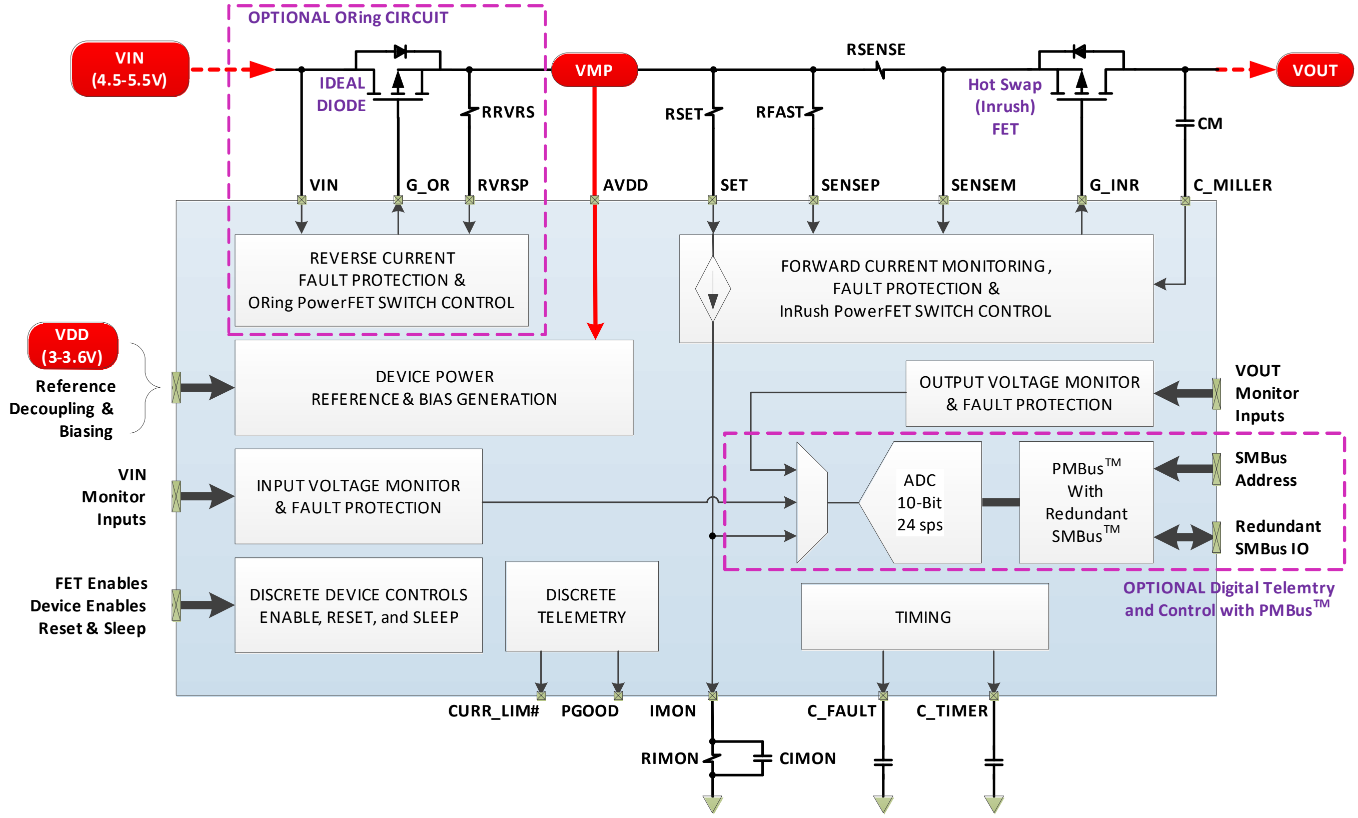

Figure 1-1. UT05PFD103 Block Diagram

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4 Pinout Package Arrangement

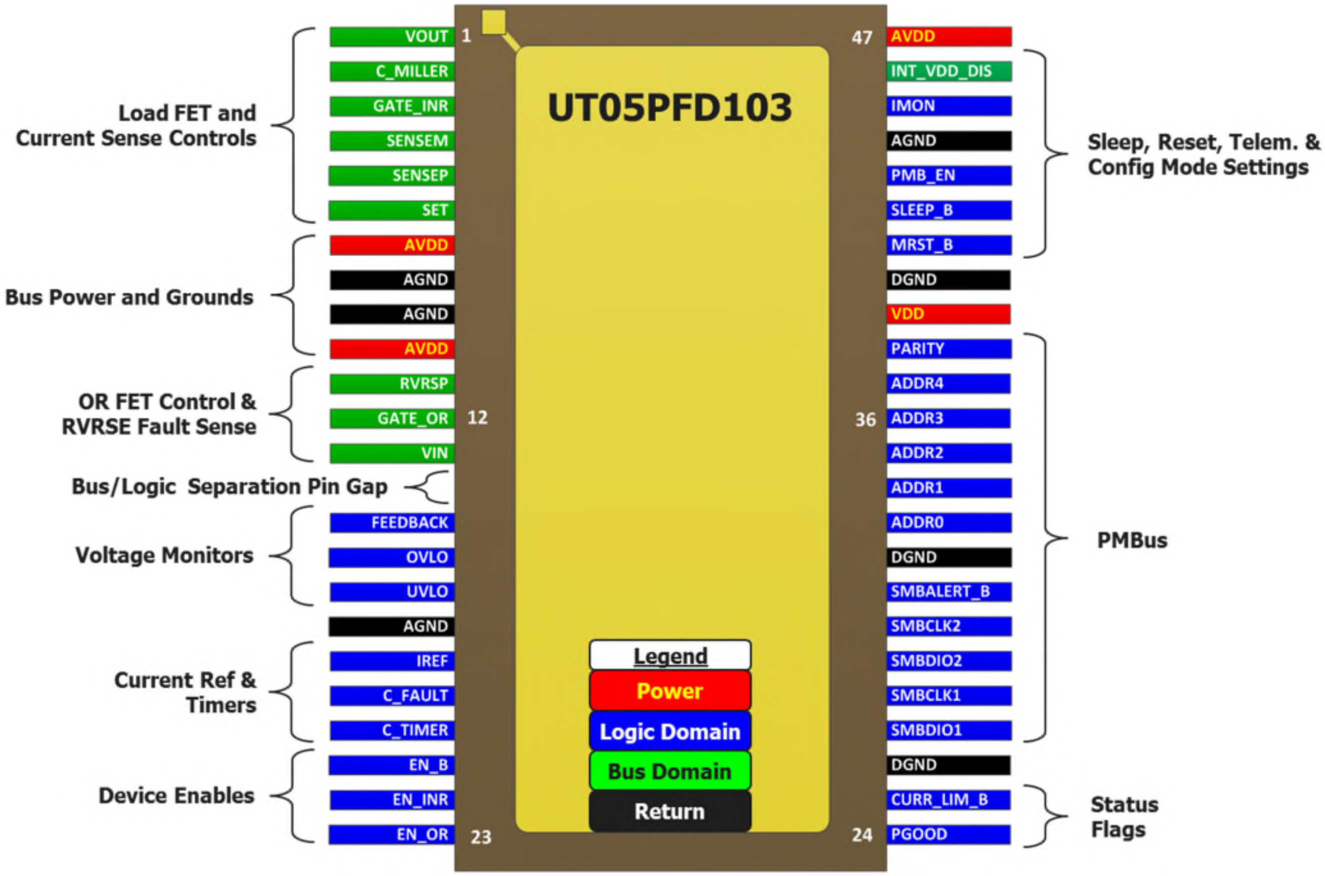


Figure 4-1. Package Pinout with Signal Groupings

5 Pinlist

Table 5-1: Pin Type Legend

Abbreviation	Description
IPU	CMOS Input with Internal Pull-Up
I	CMOS Compatible Input
I	CMOS Compatible Input
OD	Open Drain Output
SMIO	SMBus IO
SMI	SMBus Input
SMO	SMBus Output
TERN	Ternary Inputs
AI	Analog Input
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
P	Power

Table 5-2: Pin Definitions (Note 1)

Number	Name	Type	Active	Description
26, 32, 40	DGND	P		Digital ground return pins. All pins must be connected on the PCB.
8, 9, 17, 44	AGND	P		Analog ground return pins. These pins need to be connected to a quiet ground plane on the PCB. All pins must be connected on the PCB.
7, 10, 47	AVDD	P (Reference to AGND)	-	4.5V-5.5V High voltage input power supply to chip provided from VIN power line in single FET power switching application or SOURCE terminal of ORing FET in ORing applications. All pins must be connected on the PCB.
39	VDD/CBYP	P (Reference to DGND)	-	Bypass capacitor and VDD pin. A bypass capacitor must be connected from this pin to GND if internal 3.3V regulator is enabled. VDD must be connected to external 3.3V power supply if internal regulator is disabled i.e. INT_VDD_DIS is forced to AVDD
46	INT_VDD_DIS	I (Power domain VZ5_LS reference to DGND)	-	Internal 3.3V regulator disable pin. Connecting this pin to AVDD pin will disable the internal 3.3V regulator. If this pin is tied to GND the internal 3.3V regulator is enabled. A bypass capacitor will be required from VDD/CBYP pin to DGND.
18	IREF	AI (Power domain VDD reference to AGND)	-	A nominally 1V reference pin that sets the device's precision bias current when a 24.9KΩ resistor is connected from this pin to AGND. This pin also represents 50% of the ADC voltage reference.
5	SENSEP	AI (Power domain AVDD reference to VZ5_HS)	-	Fast trip sense pin for very high current limit. External resistor is connected from positive terminal of sense resistor to this pin.
6	SET	AI (Power domain AVDD reference to VZ5_HS)	-	Current limit programming pin. External resistor is connected from positive terminal of sense resistor to this pin.
4	SENSEM	AI (Power domain AVDD reference to VZ5_HS)	-	Negative terminal of sense resistor and source of load PCH_MOSFET
3	GATE_INR	AO (Power domain AVDD reference to VZ13P5_HS)	-	Gate driver output for external inrush switch PCH_MOSFET
2	C_MILLER	AO (Power domain AVDD reference to VZ13P5_HS)	-	Slew-rate limiting miller capacitor
11	RVRSP	AI (Power domain AVDD reference to VZ5_HS)	-	Positive reverse current detection pin. External resistor is connected from positive terminal of sense resistor / source of ORing PCH power FET to this pin.

Number	Name	Type	Active	Description
12	GATE_OR	AO (Power domain AVDD reference to VZ13P5_HS)	-	Gate driver output for external ORING switch PCH_MOSFET
45	IMON	AIO (Power domain VDD reference to AGND)	-	Analog current monitor and current limit adjustable pin. A 1.6KΩ resistor is connected from this pin to AGND. Ratio of this resistor to SET pin resistor programs the threshold for current limit
24	PGOOD	OD (Power domain VDD reference to DGND)	HIGH	Power GOOD status (active high open drain). True when internal device power domains and VIN, and FEEDBACK (e.g. VOUT) are within their operating range as set by voltage dividers. This pin can be used to drive enable pin for other devices.
25	CURR_LIM_B	OD (Power domain VDD reference to DGND)	LOW	Active low open drain output. When LOW, this pin indicates a current limit fault.
19	C_FAULT	AIO (Power domain VDD reference to AGND)		Adjustable fault timer for over-current timeout. A capacitor connected from this pin to AGND will set the pulse width for the analog current limit timer. This timer gets activated if the over-current limit is detected. When nothing is connected to this pin, then the default timer is set internally.
20	C_TIMER	AIO (Power domain VDD reference to DGND)		Capacitor connected from this pin to DGND will program the clock frequency of a local oscillator to be used in timer circuits.
22	EN_INR	AI (Power domain VDD reference to AGND)	-	Active high input to enable inrush gate driver. This enable input is logically combined with EN_B and PMBUS serial interface operation command register ON/OFF bit 7.
23	EN_OR	AI (Power domain VDD reference to AGND)	-	Active high input to enable ORing gate driver. This enable input is logically combined with the EN_B and PMBUS serial interface operation command register ON/OFF bit 7.
21	EN_B	AI (Power domain VDD reference to AGND)	LOW	Active low master device enable input. The active state of this pin, combined with the active state of EN_INR, EN_OR, and PMBus Operation Register Bit 7 determines if the FET gate controls can be driven active. For Pulse Mode applications: If this pin is tied to AGND the on/off pulsing duration may be controlled by the PMBUS serial interface. If EN_B pin is driven by micro controller open drain output and PMB_EN is tied to AGND, the on/off pulsing duration may be adjusted by external R and C connected to EN_B pin.
13	VIN	AI (Power domain VDD reference to AGND)	-	Source input bus voltage to internal ADC. The voltage on this input is scaled by 20:1 V/V and passed as VOUT telemetry to the 10-bit ADC. Internal measurements of this pin voltage are only accessible through PMBus.

Number	Name	Type	Active	Description
16	UVLO	AI (Power domain VDD reference to AGND)	-	Under Voltage Lock Out pin monitors the voltage VIN (Power supply) for Under Voltage fault. A resistor voltage divider from VIN to AGND is compared with internal VREF. If voltage on UVLO gets below the UVLO threshold level the load FET gate and output will be disabled.
15	OVLO	AI (Power domain VDD reference to AGND)	-	Over Voltage Lock Out pin monitors the voltage VIN (Power supply) for Over Voltage fault. A resistor voltage divider from VIN to AGND to be compared with internal VREF. If voltage on OVLO exceeds the OVLO threshold level the load FET gate and output will be disabled.
1	VOUT	AI (Power domain VDD reference to AGND)	-	Monitor input to the switched load side supply voltage. The voltage on this input is scaled by 20:1 V/V and passed as VOUT telemetry to the 10-bit ADC. Internal measurements of this pin voltage are only accessible through PMBus.
14	FEEDBACK	AI (Power domain VDD reference to AGND)		Output feedback voltage. Resistor divider from LOAD PFET Drain Terminal to this pin determines if the LOAD voltage is above its minimum allowable operating voltage. If the voltage drops below the set value, PGOOD output will fall LOW. If FEEDBACK is under its threshold voltage, no action will be taken to affect the load FET gate driver.
41	MRST_B	I (Power domain VDD reference to DGND)	LOW	Active low master reset pin. When driven low, this pin turns off the external power FETs with a strong driver, clears any faults conditions, and places all internal logic states to their POR condition.
42	SLEEP_B	IPU (Power domain VDD reference to DGND)	LOW	Active low digital input. If SLEEP_B pin is driven LOW, SPSC is put in lowest power sleep mode, disabling some of the internal circuits, and both external power FETs will be disabled. Active analog and PMBUS circuits will be in low power mode. If this pin is set to high digital level, or left floating, SPSC device operates normally, actively controlling inrush and ORing power FETs, based on power good status, voltage monitoring and fault status.
43	PMB_EN	I (Power domain VDD reference to DGND)	HIGH	Active high PMBus Enable pin. If PMB_EN pin is connected to DGND, the PMBus circuitry is disabled and all PMBus oriented functions are blocked from affecting device operation. If PMB_EN pin is connected to VDD; it enables the PMBus and all associated functions to include the SMBus interface.
27	SMBDIO1	SMIO (Power domain VDD reference to DGND)	-	SMBus bi-directional data for side 1. Open drain, 5V tolerant.
28	SMBCLK1	SMI (Power domain VDD reference to DGND)	-	SMBus clock input for side 1. Open drain, 5V tolerant.
31	SMBALERT_B	SMO (Power domain VDD reference to DGND)	LOW	Active low SMBus alert output. Open drain, 5V tolerant.

Number	Name	Type	Active	Description
29	SMBDIO2	SMIO (Power domain VDD reference to DGND)	-	SMBus bi-directional data for side 2. Open drain, 5V tolerant.
30	SMBCLK2	SMI (Power domain VDD reference to DGND)	-	SMBus clock input for side 2. Open drain, 5V tolerant.
37	ADDR4	TERN (Power domain VDD reference to DGND)	-	Ternary address line 4 for device address ID; It has 3 state, connect to digital supply (VDD), DGND, or left floating.
36	ADDR3	TERN (Power domain VDD reference to DGND)	-	Ternary address line 3 for device address ID; It has 3 state, connect to digital supply (VDD), DGND, or left floating.
35	ADDR2	TERN (Power domain VDD reference to DGND)	-	Ternary address line 2 for device address ID; It has 3 state, connect to digital supply (VDD), DGND, or left floating.
34	ADDR1	TERN (Power domain VDD reference to DGND)	-	Ternary address line 1 for device address ID; It has 3 state, connect to digital supply (VDD), DGND, or left floating.
33	ADDR0	TERN (Power domain VDD reference to DGND)	-	Ternary address line 0 for device address ID; It has 3 state, connect to digital supply (VDD), DGND, or left floating.
38	PARITY	ICS (Power domain VDD reference to DGND)	-	Odd parity bit for equivalent terminal address defined by the 5-bit ternary decoder. This parity bit will be evaluated against the ternary set address when the SPSC exits reset. If parity is good and the address is not reserved, the SPSC SMBus will take the pin-programmed address. If parity is bad and/or the address is reserved, the SPSC SMBus address will take on the SMBus special “DEFAULT ADDRESS: 1100001b”.

Note:

1) The SPSC is offered in a 47-Lead Flatpack providing an unpopulated pin gap between pins 13 and 14 to reduce the risk of shorting signals on the high-voltage domain to those on the low-voltage domain. The gap also helps ensure proper device orientation and reference for debug.

6 Functional Overview

The Smart Power Switch Controller (SPSC) provides a single device solution for controlling the gate of P-Channel Power MOSFETs while ensuring they remain within their specified Safe Operating Areas (SOAs). Combining adjustable current and voltage monitoring capability with flexible fault detection, isolation, and recovery, the SPSC integrates many of the critical functions required for power switching applications and often implemented with a number of discrete components. By integrating essential voltage and current monitoring the SPSC is able to reliably enable/disable the Power Switching MOSFET in accordance with detected fault conditions while providing telemetry to the power system manager. The following sections provide a brief summary of the major functional blocks making up the Smart Power Switch Controller.

6.1 Load Slew Rate Control and Inrush Current Limiting

The fundamental responsibility of the power switch controller is to turn a power bus isolating switch ON and OFF when commanded. To this end, the SPSC drives the gate of a P-Channel Power MOSFET (PFET) to establish/break the connection between the power line and a load. The SPSC monitors a variety of sources to determine if the LOAD switch should be ON or OFF.

When commanded to turn the switch ON, a Miller capacitor connected between the C_MILLER pin and PFET DRAIN (LOAD side) terminal will limit the inrush current which results when the input supply charges the load capacitance. By knowing the application overcurrent limit (I_{LIM}) or target peak inrush current, the C_{MILLER} value is calculated as follows:

Rising VOUT: $C_{MILLER} = \left(\left(\frac{V_{GATE}-V_T}{R_{PD}}\right) + I_{BOOT}\right) * \frac{C_{LOAD}}{I_{LIM}}$

Falling VOUT: $C_{MILLER} = \left(\frac{V_T}{R_{PU}} - I_{BOOT}\right) * \frac{C_{LOAD}}{I_{LIM}}$

Where V_T is the threshold voltage of the external PowerFET; V_{GATE}, R_{PD}, R_{PU}, and I_{BOOT} are gate driver characteristics specified in the electrical tables later in this datasheet. C_{LOAD} and I_{LIM} are application dependent.

Alternatively, if you know the rate at which you want to ramp the load voltage, you can calculate C_{MILLER} with the following equation:

Rising VOUT: $C_{MILLER} = \left(\left(\frac{V_{GATE}-V_T}{R_{PD}}\right) + I_{BOOT}\right) * \frac{\Delta t}{\Delta V_{OUT}}$

Falling VOUT: $C_{MILLER} = \left(\frac{V_T}{R_{PU}} - I_{BOOT}\right) * \frac{\Delta t}{\Delta V_{OUT}}$

Normally, the user would select a miller capacitor value that satisfies the desired ramp rate and current limit. Additionally, it is strongly recommended for the user to include a series 1.5k-ohm resistor between the C_MILLER pin and the C_{MILLER} capacitor. This resistor behaves as a current limiter for transient currents that may pass through the miller capacitor into the C_MILLER pin during a rapid, short circuit, eFusing event of the load.

6.2 OR FET Switch

In many applications, especially those that are spaceborne, redundancy and cross strapping systems are extremely important. The SPSC includes the ability to control a second, ORing, PFET to provide an ideal diode function. When enabled and as long as monitored voltage and currents are appropriate, the SPSC will activate the ORing FET. If a reverse current is detected the OR FET will be disabled.

The proper orientation of the ORing PFET is to have common source configuration with the Hot Swap PFET connecting the LOAD side supply (as shown in Figure 1-1). This ensures the highest input line power will reach the Source terminal on the LOAD switch, powering the SPSC while blocking unintentional power to the load and reverse powering a redundant, disabled, or lower voltage line supply.

If the application doesn't require ORing, the feature can be disabled by driving the EN_OR pin low and connecting RVRSP and AVDD to VIN.

6.3 Forward Current Monitoring

By installing a current sensing resistor in series with the input power line and the LOAD PFET Source terminal and by connecting a gain setting resistor from the SET pin to the input power line, the user can measure the line-to-load current through the SPSC. Using the voltage drop across the sense resistor, the SPSC mirrors a proportional current to the IMON pin. With a 1.6KΩ resistor connected between the IMON pin and GND, a voltage proportional to the load current is produced.

To set the desired line-load current limit, the user selects a SET resistor that produces a 1mA current when the voltage drop across the sense resistor is reached at the current limit. In equation form, the SET resistor is determined by:

$$Rset = \frac{Rsense * Ilimit}{1mA}$$

The line-load current limit state occurs when V_{IMON} exceeds 1.6V. This occurs when 1mA flows through the 1.6Kohm resistor from IMON pin to AGND.

The user can either measure the IMON voltage to determine the current through the LOAD FET using the equation:

$$I_{LOAD} = \frac{V_{IMON} * R_{SET}}{R_{IMON} * R_{SENSE}}$$

or by using the PMBus functionality to read the 10-bit digitized representation of the IMON voltage. The full-scale ADC voltage relating IMON is 2V with 1.6V corresponding to the user defined Overcurrent threshold.

6.4 Overcurrent Fault Protection

Internally, the Smart Power Switch Controller compares the IMON voltage to a reference voltage. When the voltage surpasses 1.6V, nominal, the C_FAULT pin begins to charge. The SPSC includes a "hiccup" feature that charges and discharges C_FAULT based on the over/under threshold voltage of IMON. The charge/discharge ratio is 20:1.

If the C_FAULT pin rises to the 1.6V threshold, the device declares an overcurrent fault condition. The SPSC responds by treating the LOAD PFET as an eFuse, switching it off to remove the voltage source from the load. Simultaneously, the CURR_LIM_B output is driven low.

Once a current fault is detected, the GATE_INR controlling the LOAD PFET's gate is latched OFF and a restart command must be received to restore power to the load. A restart command occurs when one of the device control pins (EN_B, EN_INR, MRST_B, SLEEP_B) is toggled or PMBus Operation.7 is set to 1.

Alternatively, the PMBus interface may be used to program the number of allowable restart attempts and the cool-down period before the restart is initiated.

6.5 Short Circuit Break Fault Protection

While the Overcurrent Fault Protection allows the system to trigger a fault based on an arbitrarily long elevated current condition, the Short Circuit Fault Protection circuitry monitors for a significantly higher current condition and rapidly opens (eFuses) the circuit by disabling the LOAD PFET when the user defined threshold is crossed.

With a resistor (R_{FAST}) installed between the SENSEP pin and the bus power side of the current sense resistor (R_{SENSE}), the SPSC's Short-Circuit Fault comparator evaluates the voltage drop across the sense resistor and R_{FAST}. As the load current increases, the voltage drop across R_{SENSE} increases. When the voltage drop across R_{SENSE} becomes large enough, the Short Circuit Fault comparator declares a fault condition; disabling the LOAD PFET within 500ns, typical.

6.6 Voltage Fault Protection

By implementing a voltage divider between the input line voltage and the OVLO, UVLO pins and between the VOUT and FEEDBACK pins, the user can set thresholds for over-voltage (OVLO) and under-voltage (UVLO) faults on the input line voltage and for under-voltage (FEEDBACK) on the load side.

In the event of a fault on either UVLO or OVLO the G_INR pin is driven to AVDD to disable the load PFET, PGOOD is driven low, and fault status information is updated in the PMBus fault response registers if PMBus functionality is enabled. A fault on FEEDBACK only affects the PGOOD output and corresponding PMBus status information.

6.7 Voltage Monitoring

When using the SPSC's PMBus functionality, the voltage on pins VIN and VOUT are digitized to 10-bit with 40.00V being the full-scale voltage range. Operating the UT05PFD103 to switch 5V power busses will only use the low 1/8th of the ADC codes.

PMbus commands READ_VIN and READ_VOUT are used by power management host to obtain this telemetry along with the monitored current.

6.8 PMBus

To get the maximum functionality from the SPSC, the PMBus feature must be utilized. Through the PMBus interface, a remote host controller can

- enable/disable the device
- configure Latched, Retrigger, and Pulsed modes
- obtain status on all fault conditions
- set retrigger and pulse delays
- defined retrigger count limits
- read 10-bit digitized representation of VIN, VLOAD, and IDS (aka IMON)

For spaceborne applications, system fault tolerance is often managed through redundancy. For this purpose, the SPSC provides a redundant SMBus port to access the common PMBus functions. The redundant SMBus implementation is coherent; allowing simultaneous PMBus access from the primary and secondary SMBus ports.

For applications that do not wish to use PMBus, the SPSC provides a PMB_EN control signal to disable the PMBus functionality. The SPSC can perform bus switching, monitoring, and protection tasks without any PMBus involvement.

7 Absolute Maximum Ratings [1, 2]

Table 7-1: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{HV_TECH} (3)	High Voltage Technology Capability	---	+7.2	V
AVDD (4)	Positive High Voltage Supply – Continuous Operation	-0.5	+6.0	V
BUS_IO	BUS IO Group: VIN, VOUT, GATE_INR, GATE_OR, C_MILLER, RVRSP, SET, SENSEP, SENSEM	-0.5	AVDD + 0.5	V
VDD	Positive Low Voltage Supply	-0.5	+6.5	V
LVIO	Low Voltage Digital and Analog I/O within 3.3V Domain	-0.5	VDD + 0.5	V
IO_{DC}	Average Steady State IO Current	-10	+10	mA
P_D (5)	Power Dissipation Permitted @ T_C=125°C	---	3.33	W
T_J	Junction Temperature		+175	°C
θ_{JC}	Thermal Resistance, Junction-to-Case	---	15	°C/W
T_{STG}	Storage Temperature	-65	+150	°C
ESD_{HBM} (6)	ESD Protection all Pins	---	2000	V
ESD_{HBM_SMBUS} (6)	Extended ESD Protection SMBus IO only	---	4000	V

Note:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification are not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2) All absolute voltages referenced to AGND.
3) Technology voltage capability is provided to facilitate system derating requirements. This is not a recommended operating threshold.
4) This absolute maximum rating is limited circuit construction, not by technology capability rating.
5) Per MIL-STD-883, method 1012, section 3.4.1, PD=(TJ(max)-TC(max))/θJC).
6) Per MIL-STD-883, method 3015.

8 Operational Environment

Table 8-1: Operational Environment

Symbol	Parameter	Limit	Units
TID (1)	Total Ionizing Dose	300	krad(Si)
SEL (2)	Single Event Latchup Immunity	≤ 100	MeV-cm²/mg
SEGR (2)	Single Event Gate Rupture Immunity	≤ 55	MeV-cm²/mg
SEB (3)	Single Event Burnout Immunity	≤ 55	MeV-cm²/mg
SEU (4)	Single Event Upset Immune	≤ TBD	MeV-cm²/mg
SER (4)	Soft Error Rate	≤ 1×10^{-10}	err/b-d

Note:

1) For devices procured with a total ionizing dose tolerance guarantee, post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A at an effective dose rate of 1 rad(Si)/sec up to maximum TID level procured.
2) Performed at or above Max VDD & AVDD at 125°C.
3) Performed at or above Max VDD & AVDD at 25°C.
4) Performed at or below Min VDD & AVDD at 25°C.

9 Recommended Operating Conditions (1)

Table 9-1: Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
T_C	Case Operating Temperature Range	-55	+125	°C
AVDD (2)	High Voltage Power Supply	+4.5V	+5.5V	V
VDD	Low Voltage Digital and Analog Power Supply	+3.0	+3.6	V
BUS_IO1	VIN, VOUT, GATE_OR, GATE_INR, & C_MILLER Voltage Range	0	AVDD+0.5	V
BUS_IO2	RVRSP, SET, SENSEM & SENSEP Voltage Range	AVDD-0.5	AVDD+0.5	V
LVIO	Low Voltage Digital and Analog I/O	0	VDD	V
tRF_{DIG}	Digital Input Rise & Fall Time (20%-80% of VDD) Pins: MRST_B, SLEEP_B, PMB_EN, VGS_DRV, PARITY		50	ns
AGND (3)	Analog Ground Return	0		V
DGND (3)	Digital Ground Return	AGND-10	AGND+10	mV

Note:
1) AVDD and VDD are referenced to AGND.
2) 5.5V maximum continuous operation already accounts for 77% de-rating from the 7.2V technology capability.
3) AGND and DGND shall be shorted together at a common point on the user's PCB.

10 Electrical Characteristics (1)

(AVDD = 4.5V to 5.5V, VDD = 3.3V ± 0.3V, -55°C< T_C <+125°C);
Unless otherwise noted, T_C is per the temperature range ordered.

Table 10-1: Power Supply and Reference Characteristics
Unless otherwise noted, the following parameters are tested with VDD = 3.0V

Symbol	Parameter	Conditions	Min	Max	Units
AVDD	Bus Voltage Power Supply	AVDD = 4.5V to 5.5V; Referenced to AGND	+4.5V	+5.5	V
$CBYP_{AVDD}$ (2)	AVDD Bypass Capacitor	Connect between AVDD & AGND; 1 each Per AVDD pin	1		µF
VDD	Low Voltage Power Supply	Referenced to AGND	+3	+3.6	V
$CBYP_{VDD}$	VDD Bypass Capacitor	Connect one each bypass cap from VDD to AGND & VDD to DGND	0.1		µF

Note:
1) All voltages referenced to DGND or AGND as appropriate.
2) CBYPAVDD shall be at least 4x greater than capacitance applied to C_MILLER pin.

Table 10-2: Power Supply Current Consumption Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
Single Supply Current Consumption Test conditions unless otherwise noted: • AVDD = +5.5V; • INT_VDD_DIS, EN_B = Low • EN_INR, EN_OR, MRST_B, SLEEP_B, PMB_EN = High • VIN, SENSEM, VOUT ≈ AVDD • No VOUT current load; No Fault; C_TIMER = Open; 400kHz activity on PMBus IO					
AI_{AVDD1_SNGL}	Active High Voltage Supply Current			2.8	mA
QI_{AVDD_SNGL}	Quiescent High Voltage Supply Current	EN_B=MRST_B=SLEEP_B=High; EN_INR=EN_OR=PMB_EN=Low; VOUT=Float; No PMBus Activity		2.7	mA
SI_{AVDD_SNGL}	Sleep High Voltage Supply Current	SLEEP_B=Low; VOUT=Float		1.4	mA
Dual Supply Current Consumption Test conditions unless otherwise noted: • AVDD = +5.5V; VDD = +3.6V • INT_VDD_DIS = High (AVDD) • EN_B = Low • EN_INR, EN_OR, MRST_B, SLEEP_B, PMBEN = High • VIN, SENSEM, VOUT ≈ AVDD • No VOUT current load; No Fault; C_TIMER = Open; 400kHz activity on PMBus IO					
AI_{AVDD1_DUAL}	Active High Voltage Supply Current			1.7	mA
AI_{VDD1_DUAL}	Active Low Voltage Supply Current			1.7	mA
QI_{AVDD_DUAL}	Quiescent High Voltage Supply Current	EN_B=MRST_B=SLEEP_B=High; EN_INR=EN_OR=PMB_EN=Low; VOUT=Float; No PMBus Activity		1.6	mA
QI_{VDD_DUAL}	Quiescent Low Voltage Supply Current			1.6	mA
SI_{AVDD_DUAL}	Sleep High Voltage Supply Current	SLEEP_B=Low; VOUT=Float		1	mA
SI_{VDD_DUAL}	Sleep Low Voltage Supply Current			250	μA

Note:

1) All voltages referenced to DGND or AGND as appropriate.

Table 10-3: Low Voltage Digital I/O Electrical Characteristics

Unless otherwise noted, the following parameters are tested with AVDD=4.5V and VDD = 3.0V & 3.6V.

Symbol	Parameter	Conditions	Min	Max	Units
Standard Digital Inputs (Referenced to DGND) PARITY, MRST_B, PMB_EN					
V_{IH}	High Level Input Voltage		0.7*VDD		V
V_{IL}	Low Level Input Voltage			0.3*VDD	V
I_{IL}	Input Leakage Current	VDD=3.6V INPUT = 0V or VDD	-1	1	µA
C_{IN} (1)	Input Capacitance			7	pF
Standard Digital Inputs with Pull-Ups (Referenced to DGND) SLEEP_B					
V_{IH}	High Level Input Voltage		0.7*VDD		V
V_{IL}	Low Level Input Voltage			0.3*VDD	V
I_{IL_PU}	Input Leakage Current Pull-Up	VDD=3.6V; INPUT=0V	-20	-5	µA
I_{IL}	Input Leakage Current	VDD=3.6V; INPUT=VDD		2	µA
C_{IN} (1)	Input Capacitance			7	pF
5V Digital Inputs (Referenced to DGND) INT_VDD_DIS					
V_{IH}	High Level Input Voltage		0.7*AVDD		V
V_{IL}	Low Level Input Voltage			0.3*AVDD	V
I_{IL}	Input Leakage Current	AVDD=5.5V; VDD=3.6V; INPUT = 0V or 5.5V	-1	1	µA
C_{IN} (1)	Input Capacitance			7	pF
Ternary Inputs (Referenced to DGND) ADDR0-ADDR4					
V_{IH_TERN}	High Level Input Voltage		VDD-0.3		V
V_{IM_TERN} (4)	Mid Level Input Voltage		VDD/2-0.3	VDD/2+0.3	V
V_{IL_TERN}	Low Level Input Voltage			0.6	V
I_{ILL} (3)	Low Level Input Leakage Current While Latching ADDR4-ADDR0	MRST_B=Low; VDD=3.6V; Pin under test: VADDR[x]=0V;	-100	-20	µA
I_{ILM} (3,4)	Mid Level Input Leakage Current While Latching ADDR4-ADDR0	MRST_B=Low; VDD=3.6V; Pin under test: VADDR[x]=VDD÷2;	3	40	µA
I_{ILH} (3)	High Level Input Leakage Current While Latching ADDR4-ADDR0	MRST_B=Low; VDD=3.6V; Pin under test: VADDR[x]=3.6V;	20	100	µA
C_{IN} (1)	Input Capacitance			7	pF
Open Drain Digital Outputs (Referenced to DGND) PGOOD, CURR_LIM_B					
V_{OL}	Low Level Output Voltage	ISINK = 4mA		0.4	V
I_{SC} (2)	Output Short Circuit Current	VDD=3.6V; OUTPUT=VDD	25	50	mA
I_{OZ}	Output Leakage Current	VDD=3.6V; OUTPUT = 0 or VDD;	-2	2	µA
C_{OUT} (1)	Input Capacitance			7	pF

Symbol	Parameter	Conditions	Min	Max	Units
SMBus I/O with Schmitt Trigger Inputs (Referenced to DGND) SMBCLK1, SMBDIO1, SMBCLK2, SMBDIO2, SMBALERT_B					
V_{T+}	Positive Going Input Threshold Voltage			1.89	V
V_{T-}	Negative Going Input Threshold Voltage		0.8		V
V_H	Threshold Voltage Hysteresis		80	550	mV
V_{OL}	Low Level Output Voltage	ISINK = 12mA		0.4	V
I_{SC1} (2)	Output Short Circuit Current	VDD=3.6V; OUTPUT=VDD	65	125	mA
I_{OZ}	Output Leakage Current	VDD=3.6V; OUTPUT = 0 or VDD;	-2	2	µA
C_{IO} (1)	Input Capacitance			10	pF
C_{SMB_LOAD} (1)	Total SMBus Load Capacitance			800	pF

Note:
1) Guaranteed by characterization; not tested.
2) Provided as applications information only, neither guaranteed nor tested.
3) Guaranteed by design, not tested.
4) For ADDR4, only, the mid point ternary specifications do not apply because only a HIGH and LOW state are required for the address decoding logic.

Table 10-4: Low Voltage Analog I/O Electrical Characteristics

Unless otherwise noted, the following parameters are tested with AVDD=4.5V and VDD = 3.0V & 3.6V.

Symbol	Parameter	Conditions	Min	Max	Units
Current Monitor and Overcurrent Analog Comparator (referenced to AGND) IMON					
V_{IMON_RANGE} (4)	IMON Operating Voltage Range		0	VDD	V
V_{IMON_CL}	IMON Voltage Threshold at Current Limit	Detect by ΔV on C_FAULT Pin	1.6		V
V_{IMON_TOL} (1)	IMON Voltage Threshold Tolerance		-60	60	mV
I_{IMON_CL} (4)	IMON Current at Current Limit	V_{IMON} = 1.6V	-1		mA
I_{IMON_TOL} (2, 4)	IMON Current Tolerance at Current Limit	V_{T_CL} = 25mV	± 1.5		%
		V_{T_CL} = 50mV	± 2		%
		V_{T_CL} = 100mV	± 2.5		%
I_{OZ}	Output Leakage Current	VDD=3.6V; V_{AVDD}=V_{SENSEM} OUTPUT = 0V or VDD	-2	2	µA
R_{IMON} (5)	IMON Shunt Resistor	Recommended 1% Tolerance	1.6		kΩ
C_{IMON} (5)	IMON Low Pass Filter Capacitance	$45kHz\ LPF \approx \frac{1}{2\pi * R_{IMON} * C_{IMON}}$	2.2		nF
C_{IN} (3)	Pin Capacitance			10	pF
Analog Comparator Inputs with Hysteresis (referenced to AGND) EN_B, EN_INR, EN_OR, UVLO, OVLO, FEEDBACK					
V_{T+}	Positive Going Input Threshold Voltage			1.73	V
V_{T-}	Negative Going Input Threshold Voltage		1.43		V
V_H	Threshold Voltage Hysteresis		35	100	mV
I_{IL}	Input Leakage Current	VDD=3.6V 0V ≤ INPUT ≤ VDD;	-2	2	µA
C_{IN} (3)	Pin Capacitance			7	pF
Adjustable Fault Timer (referenced to AGND) C_FAULT					
V_{T_FAULT}	Nominal Input Voltage Threshold	Detect by change on CURR_LIM_B	1.6		V
V_{T_TOL}	Input Threshold Tolerance		-45	45	mV
I_{CHARGE}	Charging Current		-125	-90	µA
$I_{DISCHARGE}$	Discharging Current		4.5	6.0	µA
C_{FAULT_INT} (3)	Internal Pin Capacitance		10		pF
Adjustable Oscillator (referenced to AGND) C_TIMER					
V_{T+}	Positive Going Input Threshold Voltage			1.45	V
V_{T-}	Negative Going Input Threshold Voltage		0.6		V
V_H	Threshold Voltage Hysteresis		225	450	mV
I_{CHARGE}	Charging Current		4.5	6	µA
$I_{DISCHARGE}$	Discharging Current		-6	-4.5	µA
F_{C_TIMER}	Default C_TIMER Frequency	C_TIMER pin capacitance ~7nF	600	1000	kHz
DC_{C_TIMER}	C_Timer Duty Cycle	C_TIMER pin capacitance ~7nF	45	55	%
C_{TIMER_INT} (3)	Internal Pin Capacitance		10		pF
Analog Comparator Error Sources EN_B, EN_INR, EN_OR, UVLO, OVLO, FEEDBACK, IMON, C_FAULT, C_TIMER					
V_{OS} (4,6)	Comparator Offset Voltage	Threshold difference between comparator positive and negative terminals	-10	+10	mV
$V1P6_{REF\_TOL}$ (4,6)	1.6V Reference Voltage Tolerance		-40	+40	mV
Noise (4,6)	Peak-Peak Noise Voltage on AGND		-15	15	mV

Symbol	Parameter	Conditions	Min	Max	Units
Bias Current Generator (reference to AGND) IREF					
R_{IREF} (5)	Required IREF Load Resistor	Connected between IREF and GND	24.9		kΩ
R_{IREF_TOL} (4)	Recommended IREF Load Resistor Tolerance		± 1		%
V_{IREF}	Voltage at IREF Pin		0.925	1.075	V
C_{IREF} (3,7)	IREF Pin External Load Capacitance			20	pF

Note:

1) V_{IMON_TOL} only includes comparator error sources that are specific to the device: Offset Voltage, Reference Accuracy, and Noise. Effective current limit detection tolerance will increase in a Root Sum Square (RSS) fashion with I_{IMON_TOL} and user dependent error sources such as R_{IMON}, R_{SENSE} and R_{SET} tolerances.
2) I_{IMON_TOL} is a function of current sense amplifier error sources (Amplifier Offset Voltage and Gain Error) at the target current limit.
3) Guaranteed by characterization; not tested.
4) Provided as applications information only, neither guaranteed nor tested.
5) Functionally tested only.
6) Effective comparator threshold tolerance can be approximated using root sum square of error sources (e.g. $\sqrt{\%V_{OS}{}^2 + \%V1P6_{REF\_TOL}{}^2 + \%Noise^2 + RSENSE_{TOL}{}^2 + RSET_{TOL}{}^2 + RIMON_{TOL}{}^2}$
7) An external capacitor on the IREF pin is not recommended for normal operation. A probe load up to the specified maximum capacitance is allowed for test and debug purposes.

Table 10-5: Bus Voltage Analog I/O Electrical Characteristics

Unless otherwise noted, the following parameters are tested with AVDD = 4.5V and VDD = 3.0V

Symbol	Parameter	Conditions	Min	Max	Units
PMOS Power FET Gate Driver (referenced to AGND) G_OR, G_INR					
V_{OFF}	Power FET Gate OFF Voltage		AVDD − 0.1	AVDD + 0.1	V
V_{ON}	Power FET Gate ON Voltage	AVDD = 5.5V	0	+0.5	V
R_{PU_FAST}	Fast Gate Driver Pull-Up Resistance	AVDD = 5.5V	3	12	Ω
R_{PU_NORM}	Normal Gate Driver Pull-Up Resistance	AVDD = 5.5V	20K	42K	Ω
R_{PD_INR}	INR Gate Driver Pull-Down Resistance	AVDD = 5.5V	140K	260K	Ω
R_{PD_OR}	OR Gate Driver Pull-Down Resistance	AVDD = 5.5V	70K	130K	Ω
I_{BOOT}	Driver Pull-down Bootstrap Current	AVDD = 5.5V	8	30	µA
C_{OUT} (1)	Pin Capacitance			20	pF
Miller Capacitance (referenced to AGND) C_Miller					
V_{FS} (2)	Full-Scale Voltage Range	AVDD = 5.5V	0	AVDD	V
R_{PU} (2, 3)	Charging/Pull-Up Resistance	MRST_B=LOW	3	12	Ω
		During Short Circuit Break	3	12	Ω
		During Normal Gate Driver Disable	20K	42K	Ω
R_{PD} (2)	Discharging/Pull-Down Resistance		140K	260K	Ω
C_{IN} (1)	Pin Capacitance			10	pF
Input and Output Bus Voltage Monitor (referenced to AGND) VIN, VOUT					
V_{FS} (4)	Full-Scale Voltage Range		0	6.5	V
R_{IN} (2)	Input Resistance		5.5	11	MΩ
I_{IN}	Input Current	AVDD=VIN=VOUT=5.5V	0.575	1.25	µA
C_{IN} (1)	Pin Capacitance			10	pF
Chopper Stabilized High-Side Current Sense Amplifier (referenced to VZ5_HS) SET (-), SENSEM (+) (Inputs); IMON (Output)					
V_{T_CL}	Current Limit Threshold (V_{AVDD}-V_{SENSEM})	G_INR=LOW (≈ 0V) EN_INR=HIGH EN_B=LOW; R_{SET} = 25Ω	22	29	mV
		G_INR=LOW (≈ 0V) EN_INR=HIGH EN_B=LOW; R_{SET} = 50Ω	45	58	mV
		G_INR=LOW (≈ 0V) EN_INR=HIGH EN_B=LOW; R_{SET} = 100Ω	90	110	mV
R_{SET_TOL} (2)	Recommended R_{SET} Tolerance		±0.1		%
V_{OS} (2)	Input Offset Voltage	(V_{AVDD}-V_{SENSEM}) < 5mV	-4.8	4.8	mV
		(V_{AVDD}-V_{SENSEM}) > 5mV	-200	200	µV
G_{ERR} (2)	Gain Error at IMON	@ 20% of V_{T_CL}; V_{T_CL} = 25mV	± 6.9		%
		@ 20% of V_{T_CL}; V_{T_CL} = 50mV	± 3.4		%
		@ 20% of V_{T_CL}; V_{T_CL} = 100mV	± 1.7		%
		@ 100% of V_{T_CL}; V_{T_CL} = 25mV	± 0.6		%
		@ 100% of V_{T_CL}; V_{T_CL} = 50mV	± 1.1		%
		@ 100% of V_{T_CL}; V_{T_CL} = 100mV	± 2.2		%
VCMR (2)	Common Mode Voltage Range		AVDD − 0.5	AVDD + 0.5	V
CMRR (2)	Common Mode Rejection Ratio			-75	dB
PSRR (2)	Power Supply Rejection Ratio			-60	dB
C_{IN} (1)	Internal Pin Capacitance			10	pF

Symbol	Parameter	Conditions	Min	Max	Units
Fast Short Circuit and Reverse Current Detect Comparator (referenced to AGND) SENSEP (+), SENSEM (-) of Short Circuit Comparator and RVRSP (+), VIN (-) of Reverse Current Comparator					
V_{T_SC}	Short Circuit Fault Threshold (V_{AVDD}-V_{SENSEM}) $R_{FAST} * I_{BIAS} = R_{SENSE} * I_{SC}$	R_{FAST} = 875Ω	28	44	mV
		R_{FAST} = 5kΩ	185	230	
		R_{FAST} = 10kΩ	370	460	
R_{FAST} (4)	Recommended Short Circuit Threshold Setting Resistor	Recommended Tolerance ±0.1%	0.875	10	kΩ
V_{T_RVRS}	Reverse Current Fault Threshold (V_{AVDD}-V_{VIN}) $R_{RVRS} * I_{BIAS} = R_{FET\_RDSON} * I_{RVRS}$	R_{RVRSP} = 2.5kΩ	85	115	mV
		R_{RVRSP} = 5kΩ	185	230	
		R_{RVRSP} = 10kΩ	370	460	
R_{RVRSP} (4)	Recommended Reverse Current Fault Threshold Setting Resistor	Recommended Tolerance ±0.1%	2.5	10	kΩ
V_{OS}(2)	Input Offset Voltage		-5	5	mV
I_{BIAS}	SENSEP and RVRSP Input Bias Current		40		µA
I_{BIAS_TOL}	SENSEP and RVRSP Input Bias Current Tolerance		-4	+6	µA
VCMR(2)	Common Mode Voltage Range		1.5	AVDD + 0.1	V
CMRR(2)	Common Mode Rejection Ratio			-60	dB
PSRR(2)	Power Supply Rejection Ratio			-60	dB
C_{IN} (1)	Internal Pin Capacitance			10	pF

Note:

1) Guaranteed by characterization; not tested.
2) Provided as applications information only, neither guaranteed nor tested.
3) The charging (Pull-Up) resistance on the C_MILLER pin depends on the condition commanding the pin to AVDD. During reset (Power-on-reset, and manual reset) and short circuit detection, C_MILLER is charged with an independent pull-up from standard gate driver controls. All other commanded (e.g. EN_INR, EN_OR, etc) and fault driven (e.g. UVLO, Overcurrent, etc.) disabling of G_INR rely on the normal G_INR pull-up resistance to charge C_MILLER to AVDD.
4) Functionally tested only.

Table 10-6: Three Channel Analog-to-Digital Converter Characteristics

Unless otherwise noted, the following parameters are tested with AVDD = 6.5V and VDD = 3.0V & 3.6V

Symbol	Parameter	Conditions	Min	Max	Units
ADC with 3-Channel Analog Mux Functional Characteristics (referenced to AGND)					
ADC_{RES} (3)	ADC Resolution		10		Bits
ADC_{FSV} (4)	ADC Full-Scale Voltage	Can be approximated by V_{IREF} * 2	1.85	2.15	V
ADC_{LSB} (4)	ADC Least Significant Bit		1.81	2.1	mV
ADC_{ACQ_CH} (1)	ADC Channel Acquisition Time	Time to sample and convert any of VOUT, VIN, or IMON		5	ms/s
ADC_{RR_CYCLE} (1)	ADC Round Robin Cycle Time	Time to Convert and Acquire VOUT, VIN, and IMON	65	131	ms/cyc
INL (4)	Integral Non-Linearity	20% FSV ≤ ADC Input ≤ 80% FSV AVDD=6.5V	±5		LSB
DNL (4)	Differential Non-Linearity	20% FSV ≤ ADC Input ≤ 80% FSV	±0.95		LSB
ERR_{OFFSET} (4)	ADC Offset Error		±20		LSB
ERR_{GAIN}	ADC Gain Error	Calculated by: $E_{GAIN} = \frac{V_{SFV}-V_{OFFSET}}{V_{LSB}} - (2^{10} - 2)$	±40		LSB
CMRR (1)	Common Mode Rejection Ratio			-80	dB
PSRR (1)	Power Supply Rejection Ratio	ΔVDD = 300mV		-70	dB
R_{CHNL} (1)	Analog Mux Channel Resistance	0.0V ≤ ADC Input ≤ 2.0V	218	4640	Ω
CH_{ISO} (1)	Channel-to-Channel Isolation	Δ Aggressor Channel = 1V		-80	dB
ADC Telemetry Input Characteristics (referenced to AGND) VIN, VOUT, IMON (Inputs); Results Obtained from PMBus Commands (88h, 8Bh, 8Ch)					
VIN_{FSV} (4)	VIN Full-Scale Voltage	For Code Calculation purposes; AVDD=6.5V	40		V
VIN_{LSB} (4)	VIN Least Significant Bit	$VIN_{LSB} = \frac{ADC_{FSV}}{1024} * 20$	36.13	41.99	mV/bit
VIN_{GAIN} (1)	VIN Gain		0.05		V/V
$VIN_{INACCURACY}$ (1,2,4)	VIN Inaccuracy at ADC Output	Measured at Full-Scale Voltage	±7.5		%
$VOUT_{FSV}$ (4)	VOUT Full-Scale Voltage	For Code Calculation purposes; AVDD=6.5V	40		V
$VOUT_{LSB}$ (4)	VOUT Least Significant Bit	$VOUT_{LSB} = \frac{ADC_{FSV}}{1024} * 20$	36.13	41.99	mV/bit
$VOUT_{GAIN}$ (1)	VOUT Gain		0.05		V/V
$VOUT_{INACCURACY}$ (1,2,4)	VOUT Inaccuracy at ADC Output	Measured at Full-Scale Voltage	±7.5		%
$IMON_{LSB}$ (1)	IMON Least Significant Bit	$IMON_{LSB} = \frac{R_{SET}}{R_{SENSE}} * \frac{ADC_{FS}}{R_{IMON}} * \frac{1}{1024}$	Derived		mA/bit
$IMON_{GAIN}$ (1)	IMON Gain	V_{T_CL} = 25mV	64		V/V
		V_{T_CL} = 50mV	32		V/V
		V_{T_CL} = 100mV	16		V/V
$IMON_{INACCURACY}$ (1,2)	IMON Inaccuracy at ADC Output	@ 20% of V_{T_CL}; V_{T_CL} = 25mV	± 8.3		%
		@ 20% of V_{T_CL}; V_{T_CL} = 50mV	± 5.7		%
		@ 20% of V_{T_CL}; V_{T_CL} = 100mV	± 4.82		%
		@ 100% of V_{T_CL}; V_{T_CL} = 25mV	± 2.82		%
		@ 100% of V_{T_CL}; V_{T_CL} = 50mV	± 2.9		%
		@ 100% of V_{T_CL}; V_{T_CL} = 100mV	± 3.44		%

Note:

1) Provided as applications information only, neither guaranteed nor tested.
2) Accuracy at the ADC output includes all device specific errors sources (e.g. gain errors, offsets, noise, etc.). It does not include the contribution of externally selected user components like resistor tolerances.
3) Functionally tested only.
4) Calculated form best fist least mean squares method.

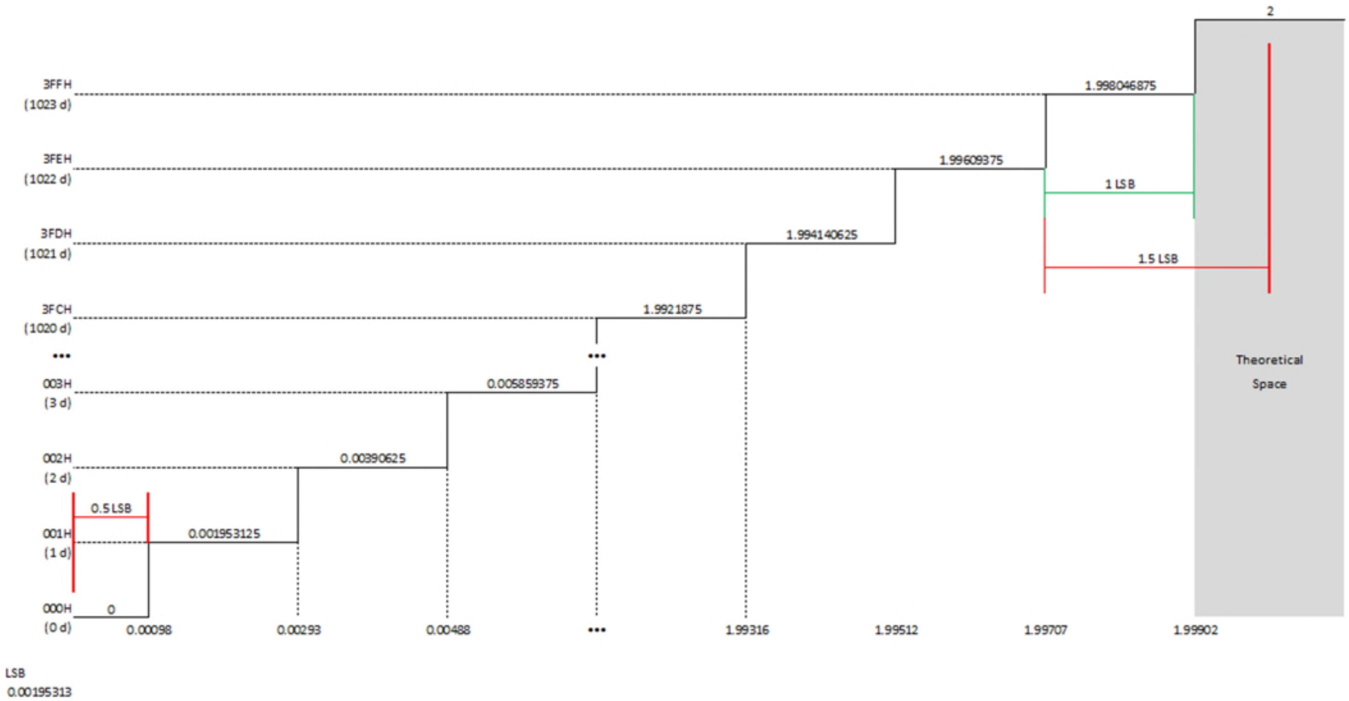


Figure 10-1. ADC Ideal Transfer Function

11 Timing Characteristics

(AVDD = 4.5V to 5.5V, VDD = 3.3V ± 0.3V, -55°C< T_C <+125°C);
Unless otherwise noted, T_C is per the temperature range ordered.

Table 11-1: Current Limit Response Timing

Unless otherwise noted, the following parameters are tested with AVDD = 4.5V & 5.5V and VDD = 3.0V & 3.6V

Symbol	Parameter	Condition	Min	Max	Units
R_{IMON} = 1.6kΩ; C_{IMON} = 2.2nF; C_FAULT = Open (<10pF); EN_B = LOW; MRST_B = SLEEP_B = HIGH; PMB_EN = EN_OR = HIGH or LOW;					
t_{CL2INR} (1)	Current Limit Detection to G_INR HIGH	(V_{AVDD}-V_{SENSEM}) transition from 0V to 1.25*V_{T_CL}		38	µs
$t_{CL2IMON}$	Current Limit Detection to IMON HIGH	(V_{AVDD}-V_{SENSEM}) transition from 0V to 1.25*V_{T_CL}		22	µs
$t_{IMON2FLT}$	IMON HIGH to C_FAULT HIGH	AVDD=4.5V		6	µs
$t_{FLT2CLB}$	C_FAULT HIGH to CURR_LIM_B LOW			10	µs
$t_{FLT2OFF}$ (1)	C_FAULT HIGH to G_INR HIGH	AVDD=4.5V		12	µs
$t_{MRBL2FLTL}$	MRST_B LOW to C_FAULT LOW	AVDD=4.5V		4	µs
t_{CLB_RESET}	CURR_LIM_B Reset Delay	AVDD=4.5V; $R_{PULL-UP}$=1kΩ; C_{LOAD}=50pF		1	µs

Note:
1) Test performed without contribution of Miller Capacitance or Gate Charge on pin under test.

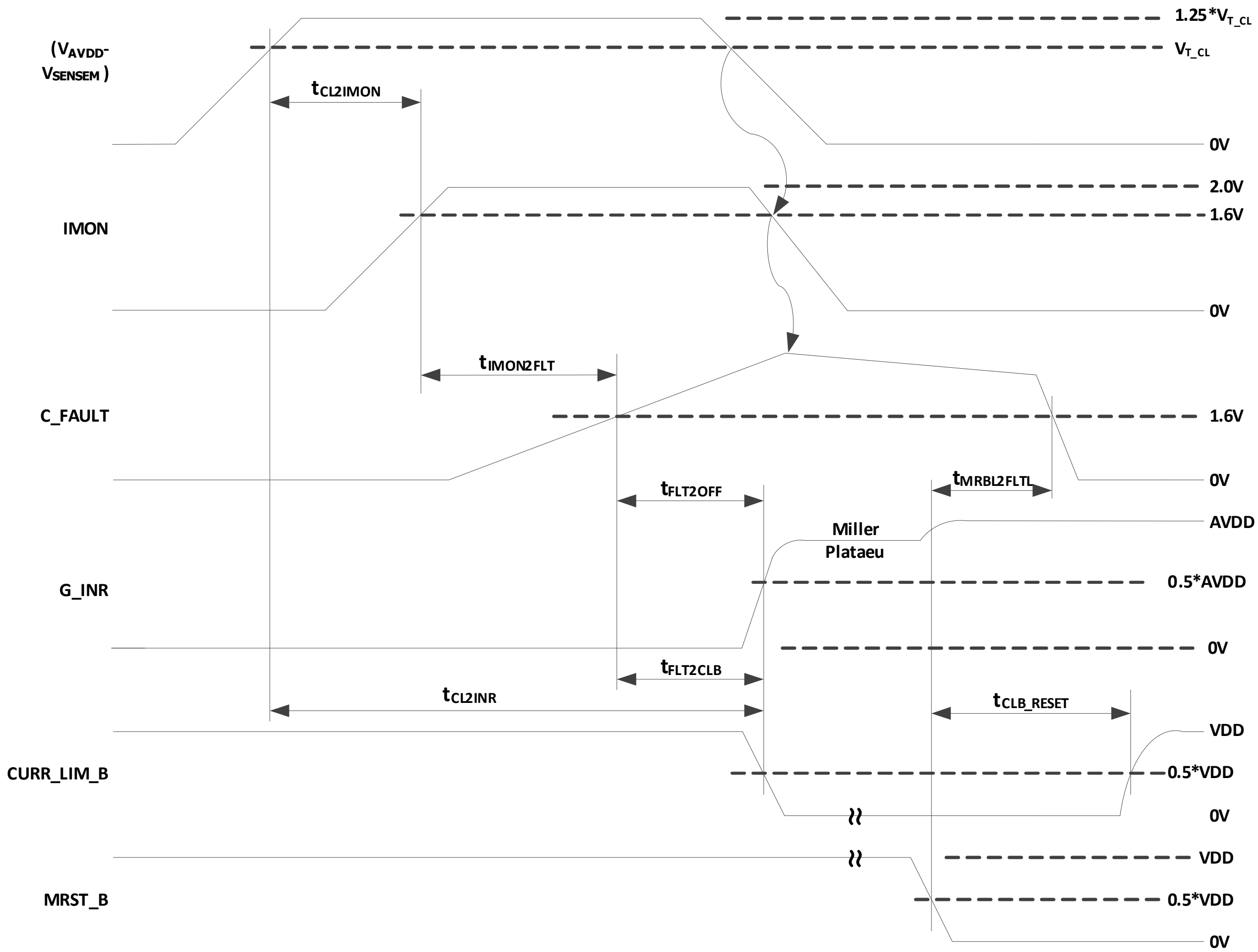


Figure 11-1. Current Limit Response Timing Diagram

Table 11-2: Reverse Current and short Circuit Break Timing

Unless otherwise noted, the following parameters are tested with AVDD = 4.5V & 5.5V and VDD = 3.0V & 3.6V

Symbol	Parameter	Conditions	Min	Max	Units
EN_B = LOW; EN_INR = EN_OR = HIGH; SLEEP_B = HIGH; PMB_EN = X;					
t_{BREAK_INR} (1)	INR FET Short Circuit Break Timing	(V_{AVDD}-V_{SENSEM}) transitions from 0mV to 1.25*V_{T_SC}		500	ns
t_{BREAK_OR} (1)	OR FET Reverse Current Break Timing	(V_{AVDD}-V_{VIN}) transitions from 0mV to 1.25*V_{T_RVRS}		500	ns
$t_{SC2CLBL}$	Short Circuit Detect to CURR_LIM_B LOW	(V_{AVDD}-V_{SENSEM}) transitions from 0mV to 1.25*V_{T_SC}		10	µs
$t_{RVRS2CLBL}$	Reverse Current Detect to CURR_LIM_B LOW	(V_{AVDD}-V_{VIN}) transitions from 0mV to 1.25*V_{T_RVRS}		10	µs
t_{CLB_RESET}	CURR_LIM_B Reset Delay	AVDD=4.5V; $R_{PULL-UP}$=1kΩ; C_{LOAD}=50pF		5	µs
$t_{RETRIGGER}$ (2)	Retrigger Delay	CURR_LIM_B ↑ to MRST_B ↑	0		ns

Notes:
1) Test performed without contribution of Miller Capacitance or Gate Charge on pin under test.
2) Provided as applications information only, neither guaranteed nor tested.

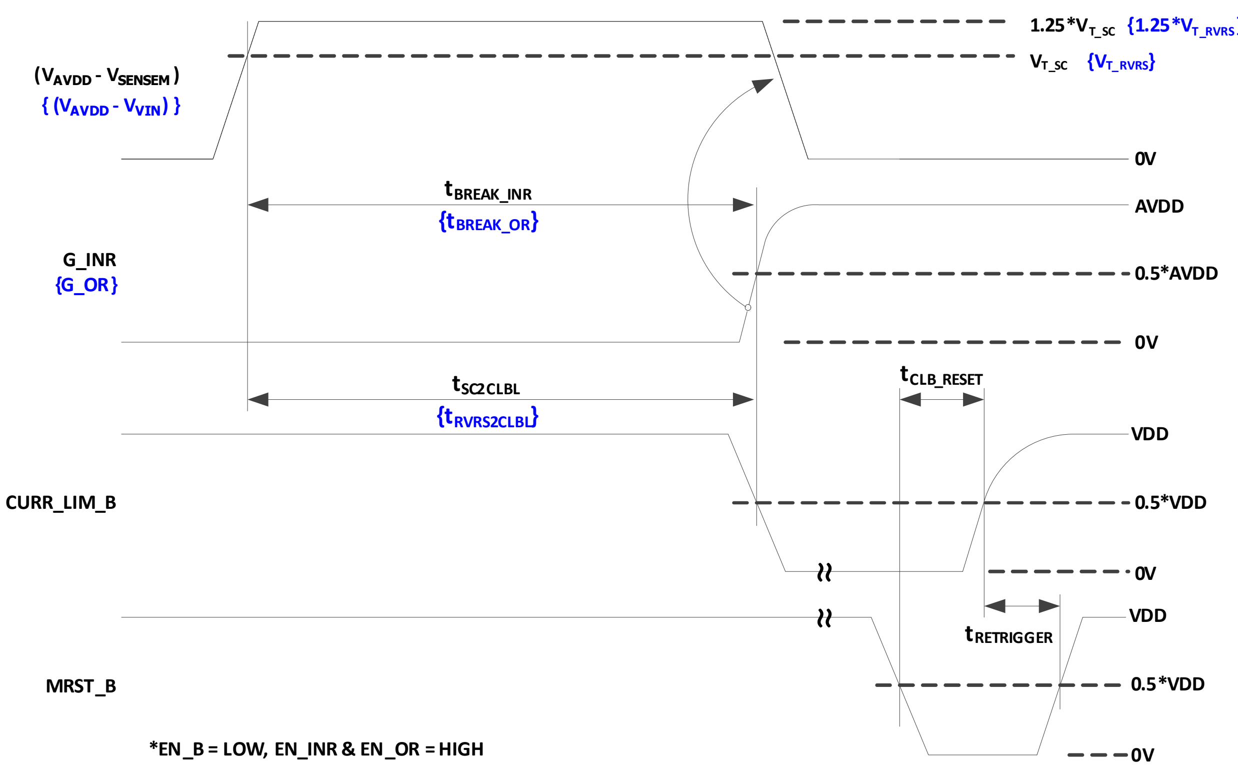


Figure 11-2. Reverse Current and Short Circuit Break Timing Diagram

Table 11-3: Voltage Fault and PGOOD Timing

Unless otherwise noted, the following parameters are tested with AVDD = 5.5V and VDD = 3.0V & 3.6V

Symbol	Parameter	Conditions	Min	Min	Units
MRST_B = SLEEP_B = HIGH; PMB_EN = EN_OR = X; EN_B = LOW; EN_INR = HIGH					
$t_{LOCKOUT}$ (1)	OVLO/UVLO Lockout ON Delay	OVLO ↑ or UVLO↓ to G_INR↑		40	µs
$t_{LOCK2PGL}$	OVLO/UVLO to PGOOD False Delay	OVLO ↑ or UVLO↓ to PGOOD↓		5	µs
$t_{LOCKOFF}$ (1)	OVLO/UVLO Lockout OFF Delay	OVLO↓ or UVLO↑ to G_INR↓		40	µs
t_{PGOOD1}	OVLO/UVLO to PGOOD True Delay	OVLO↓ or UVLO↑ to PGOOD↑		5	µs
$t_{FBL2PGL}$	FEEDBACK to PGOOD False Delay	FEEDBACK↓ to PGOOD↓		10	µs
t_{PGOOD2}	FEEDBACK to PGOOD True Delay	FEEDBACK↑ to PGOOD↑		10	µs

Note:
1) Test performed without contribution of Miller Capacitance or Gate Charge on pin under test.

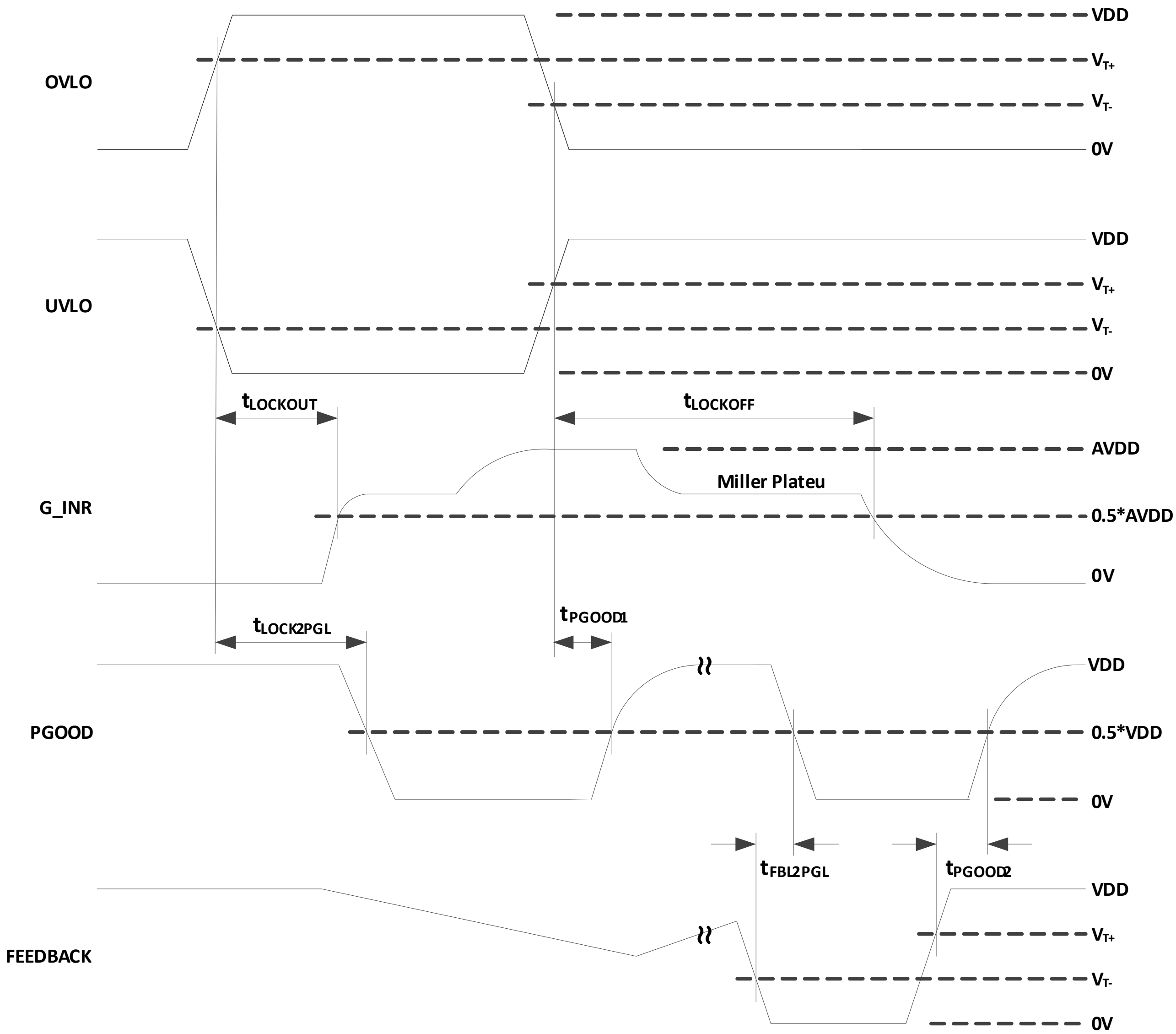


Figure 11-3. Voltage Fault and PGOOD Timing Diagram

Table 11-4:Commanded Enable and Disable Timing

Unless otherwise noted, the following parameters are tested with AVDD = 5.5V and VDD = 3.0V & 3.6V

Symbol	Parameter	Conditions	Min	Max	Units
MRST_B = SLEEP_B = HIGH; PMB_EN = X					
t_{DIS_INR} (1)	EN_INR False to G_INR Disabled	EN_B = LOW; EN_OR = X		40	μs
t_{EN_INR} (1)	EN_INR True to G_INR Enabled	EN_B = LOW; EN_OR = X		40	μs
t_{DIS_OR} (1)	EN_OR False to G_OR Disabled	EN_B = LOW; EN_INR = X		10	μs
t_{EN_OR} (1)	EN_OR True to G_OR Enabled	EN_B = LOW; EN_INR = X		10	μs
t_{DIS_ALL} (1)	EN_B False to G_INR & G_OR Disabled	EN_INR = HIGH; G_INR Rising		40	μs
		EN_OR = HIGH; G_OR Rising		10	μs
t_{EN_ALL} (1)	EN_B True to G_INR & G_OR Enabled	EN_INR = HIGH; G_INR Falling		40	μs
		EN_OR = HIGH; G_OR Falling		10	μs

Note:

1) Test performed without contribution of Miller Capacitance or Gate Charge on pin under test.

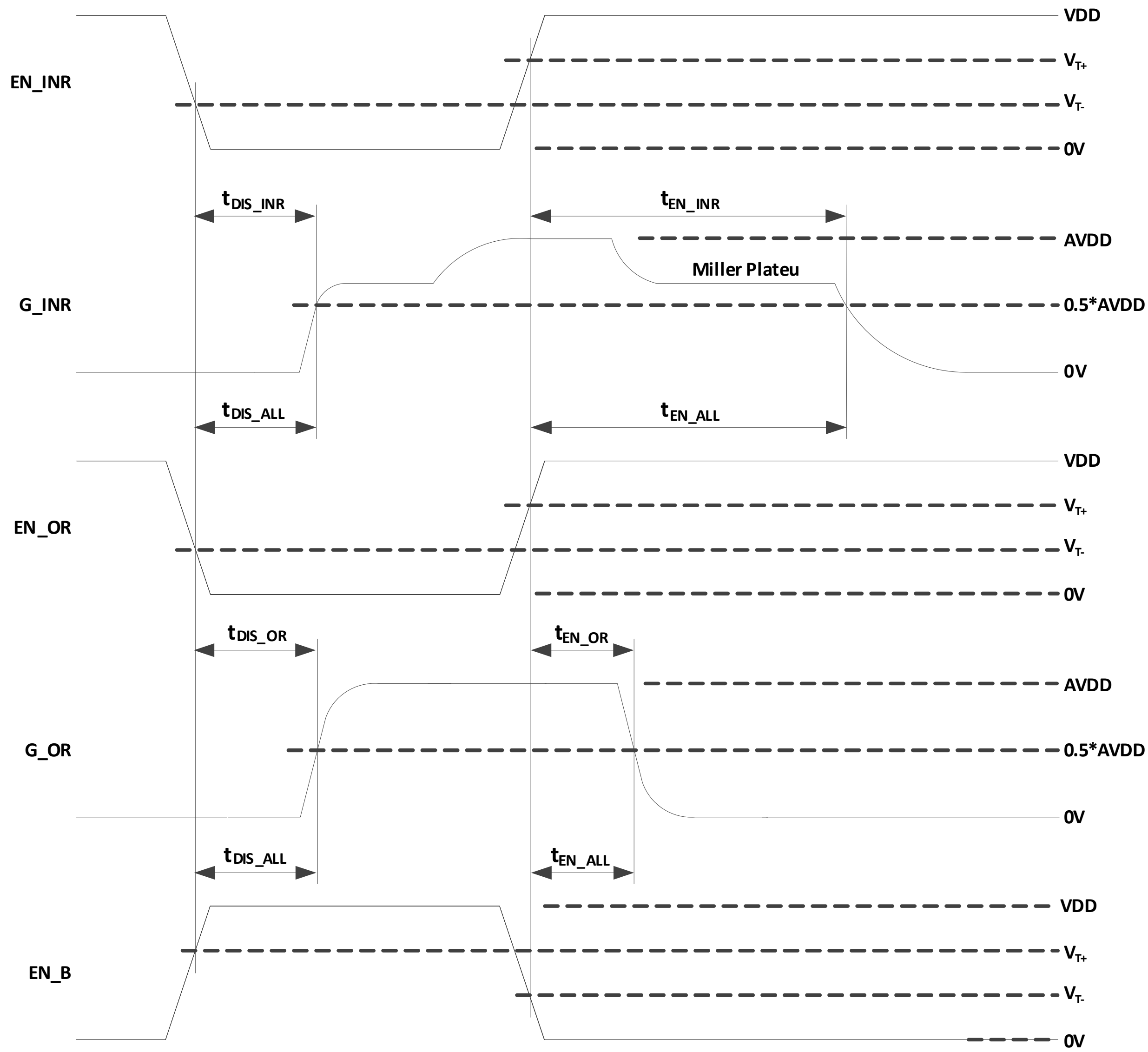


Figure 11-4. Commanded Enable and Disable Timing Diagram

Table 11-5: Power Up/Down and Reset Timings

Symbol	Parameter	Conditions	Min	Max	Units
In dual supply mode (INT_VDD_DIS = AVDD) AVDD ≥ (VDD – 0.5V) unless Power Switch ORing is implemented. In single supply mode (INT_VDD_DIS = DGND) VDD will track AVDD until it reaches its regulated voltage.					
$t_{MRST\_POR\_OFF}$ (1)	AVDD & VDD On to MRST_B False		50		µs
$t_{AVDDH2PGH}$ (2)	AVDD HIGH to PGOOD True			90	µs
$t_{VDDH2PGH}$ (2)	VDD HIGH to PGOOD True			90	µs
$t_{AVDDL2PGL}$ (2)	AVDD LOW to PGOOD False			90	µs
$t_{VDDL2PGL}$	VDD LOW to PGOOD False			90	µs

Notes:
1) Functionally tested only
2) Provided as applications information only, neither guaranteed nor tested.

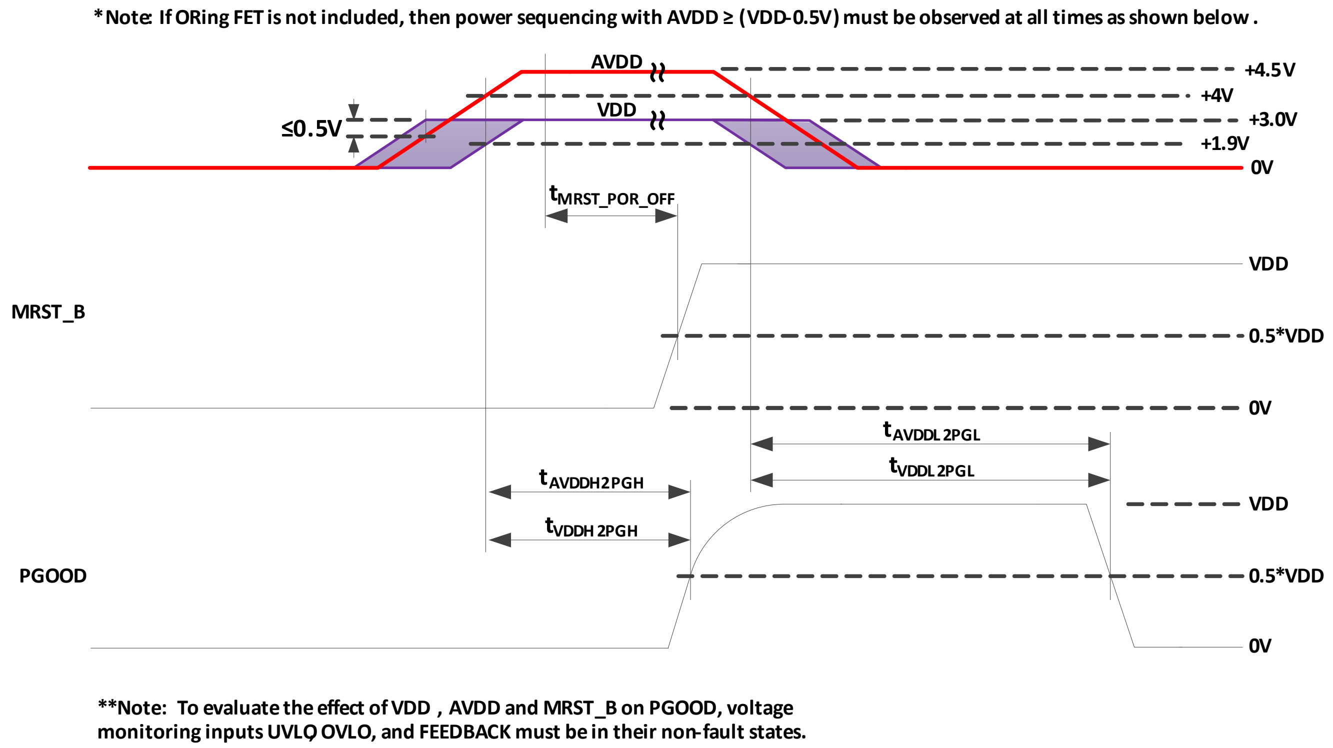


Figure 11-5. Power Up/Down and Reset Timing Diagram

Table 11-6: Master Reset Timing

Unless otherwise noted, the following parameters are tested with AVDD = 5.5V and VDD = 3.0V & 3.6V

Symbol	Parameter	Conditions	Min	Max	Units
EN_INR = EN_OR = SLEEP_B = UVLO = FEEDBACK = HIGH; EN_B = OVLO = LOW					
t_{MRSTB_LOW} (1)	MRST_B Pulse Width LOW		50		µs
t_{SETUP} (1)	Configuration Inputs SETUP time to MRST_B False	PMB_EN = HIGH	1		µs
t_{HOLD} (1)	Configuration Inputs HOLD time from MRST_B False	PMB_EN = HIGH	10		µs
$t_{MRSTBH2SMBRDY}$ (1)	MRST_B Deassertion to SMBus Ready for Communication	PMB_EN = HIGH		100	µs
$t_{MRSTBL2INR\_DIS}$ (2)	MRST_B True to G_INR Disabled	PMB_EN=LOW		500	ns
$t_{MRSTBH2INR\_EN}$ (2)	MRST_B False to G_INR Enabled	PMB_EN=LOW		40	µs
$t_{MRSTBL2OR\_DIS}$ (2)	MRST_B True to G_OR Disabled	PMB_EN=LOW		500	ns
$t_{MRSTBH2OR\_EN}$ (2)	MRST_B False to G_OR Enabled	PMB_EN=LOW		10	µs

Notes:
1) Functionally tested only.
2) Test performed without contribution of Miller Capacitance or Gate Charge on pin under test.

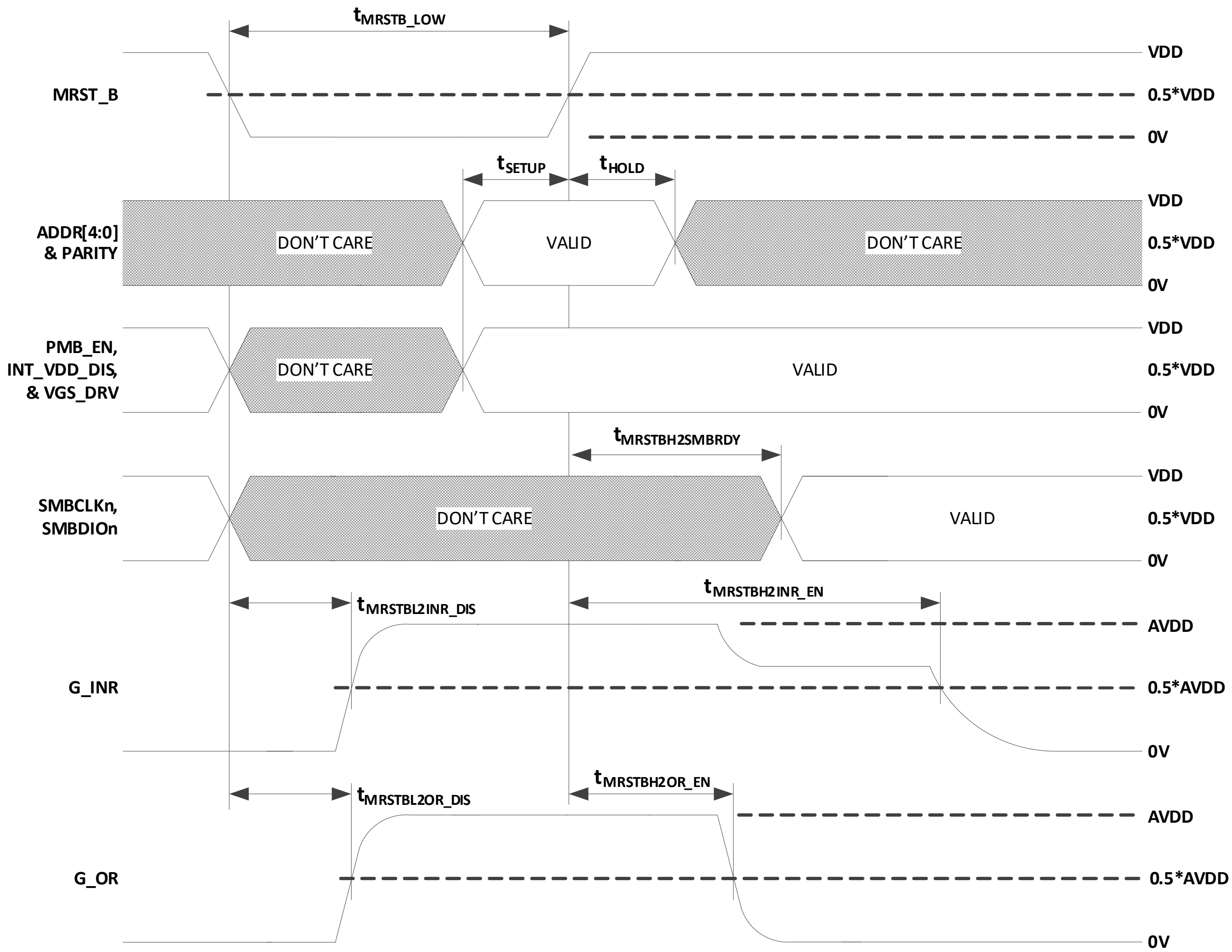


Figure 11-6. Master Reset Timing Diagram

Table 11-7: Sleep Timing

Unless otherwise noted, the following parameters are tested with AVDD = 5.5V and VDD = 3.0V & 3.6V

Symbol	Parameter	Conditions	Min	Max	Units
EN_INR = EN_OR = PMB_EN = MRST_B = UVLO = HIGH; EN_B = OVLO = FEEDBACK = LOW					
t_{SLEEP_ON} (1)	Time to Enter Sleep Mode			100	µs
t_{SLEEP_OFF} (1)	Time to Exit Sleep Mode			100	µs
$t_{SLPL2INR\_DIS}$ (2)	SLEEP_B True to G_INR Disabled			50	µs
$t_{SLPH2INR\_EN}$ (1)	SLEEP_B False to G_INR Enabled			70	µs
$t_{SLPL2OR\_DIS}$ (2)	SLEEP_B True to G_OR Disabled			50	µs
$t_{SLPH2OR\_EN}$ (1)	SLEEP_B False to G_OR Enabled			20	µs

Notes:

1) Provided as applications information only, neither guaranteed nor tested.
2) Test performed without contribution of Miller Capacitance or Gate Charge on pin under test.

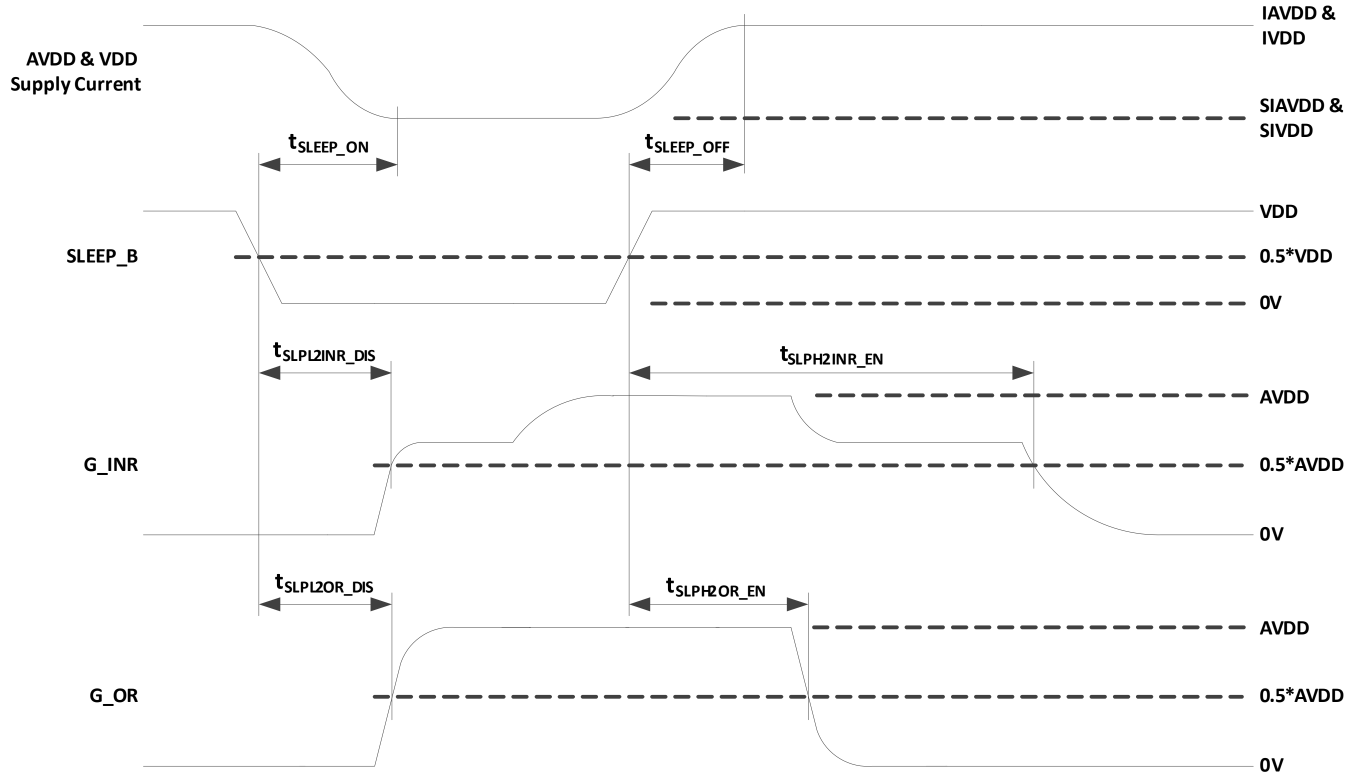


Figure 11-7. Sleep Timing Diagram

Table 11-8: Master Reset and Sleep Timing

Unless otherwise noted, the following parameters are tested with AVDD = 4.5V and VDD = 3.0V & 3.6V

Symbol	Parameter	Conditions	Min	Max	Units
MRST_B = SLEEP_B = HIGH; PMB_EN = HIGH;					
t_{H_START}	SMBCLK Hold Time After (REPEATED) Start Condition		0.6		µs
$t_{H\_DATA\_IN}$ (1)	SMBDIO Input Hold Time After SMBCLK		0		ns
$t_{S\_DATA\_IN}$ (1)	SMBDIO Input Setup Time Before SMBCLK		100		ns
t_{DATA_OUT} (2)	SMBDIO Output Data Valid After SMBCLK			0.6	µs
t_{S_START}	SMBCLK Setup Time Before REPEATED START Condition		0.6		µs
t_{S_STOP}	SMBCLK Setup Time Before STOP Condition		0.6		µs
t_{BUF}	Bus Free Time Between STOP and START Condition		1.3		µs
f_{SMB}	SMBus Operating Frequency			400	kHz
T_{SMB}	SMBCLK Period		2.5		µs
t_{SCL_LOW}	SMBCLK LOW Time		1.3		µs
t_{SCL_HIGH}	SMBCLK HIGH Time		0.6	50	µs
t_{FALL} (4)	SMBCLK/SMBDIO Fall Time			300	ns
t_{RISE} (4)	SMBCLK/SMBDIO Rise Time			300	ns
t_{NOISE_SPIKE} (3, 4)	Noise Spike Suppression Time			50	ns

Notes:

1) SMBDIO input setup and hold times must be assured at the corresponding pins of the UT05PFD103 in relation to the input threshold voltages V_{T+} (rising edge) and V_{T-} (falling edge).
2) SMBDIO out will be valid (above/below threshold voltage) at the corresponding UT05PFD103 pin the specified duration after SMBCLK is detected LOW. C_{LOAD} = 40pF.
3) Noise spikes up to the maximum Noise Spike Suppression time will be filtered by the UT05PFD103.
4) Provided as applications information only, neither guaranteed nor tested.

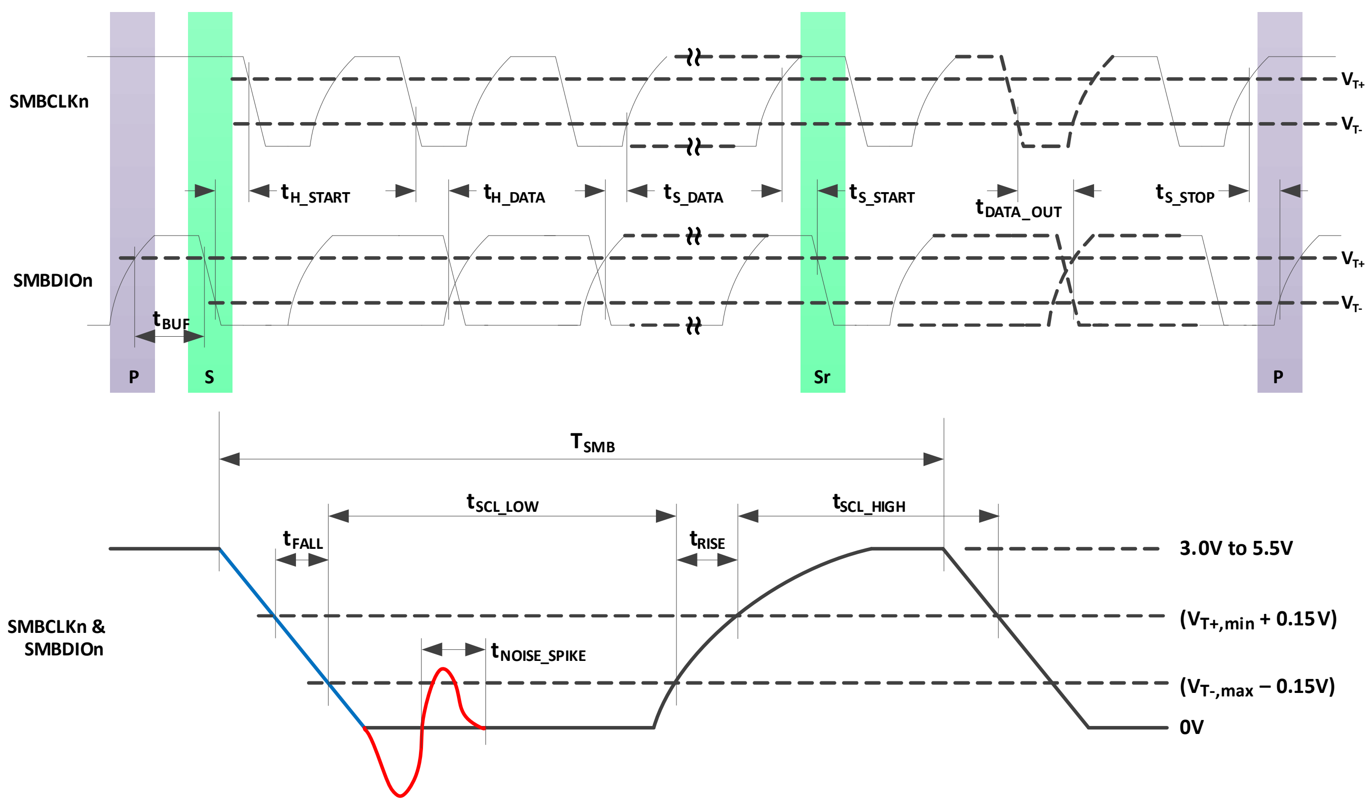


Figure 11-8. SMBus Timing Diagram

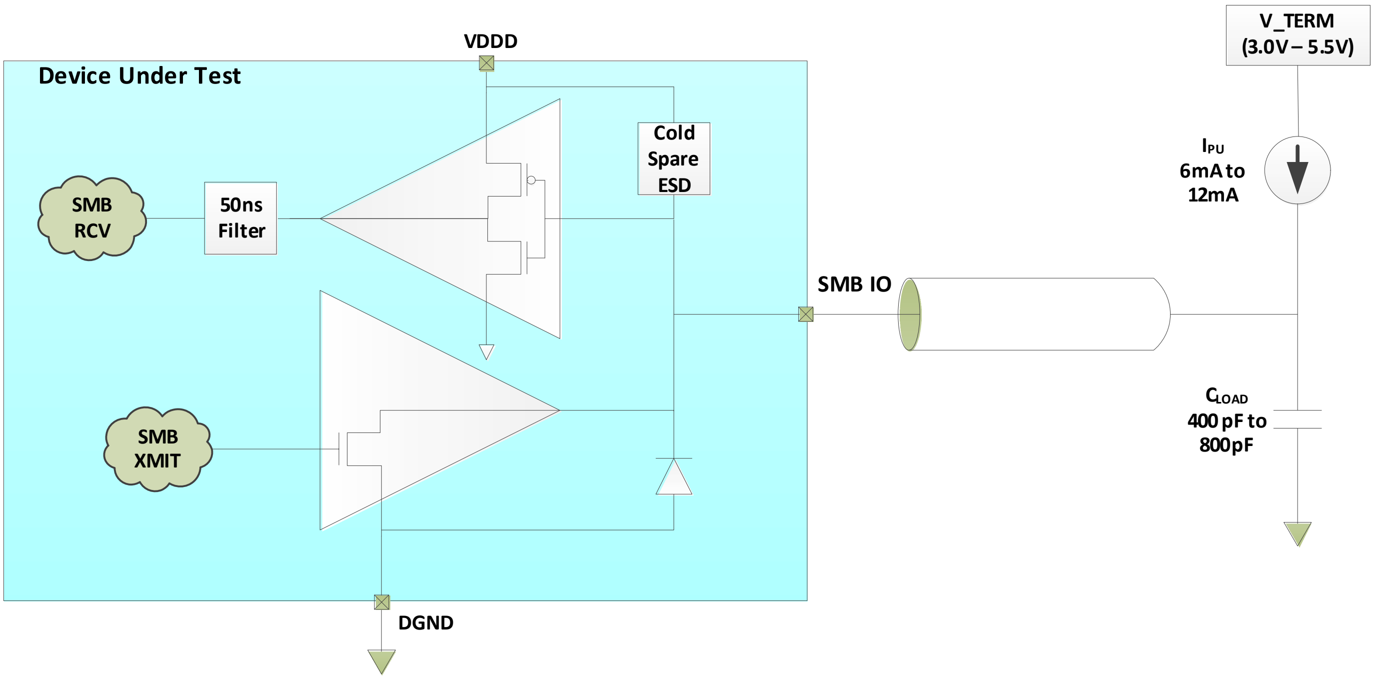
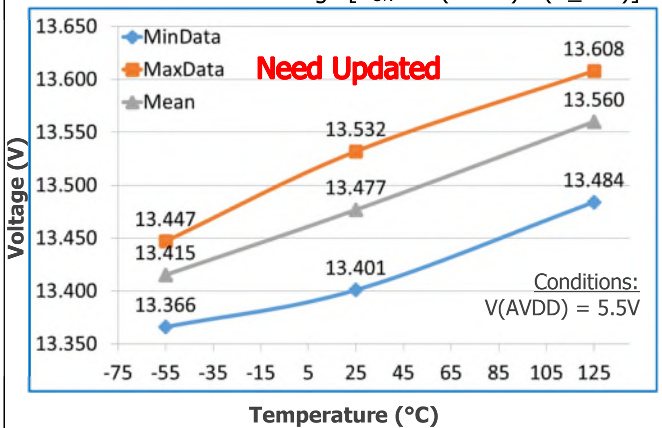


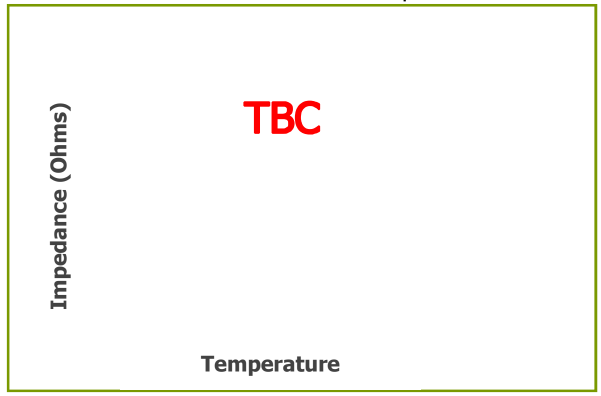
Figure 11-9. SMBus IO Test Load

12 Typical Performance Characteristics [1]

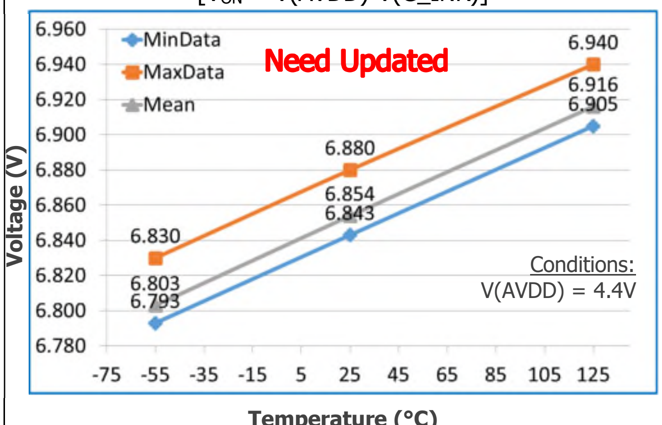
INR Gate Driver ON Voltage [V_{ON} = V(AVDD)-V(G_INR)]



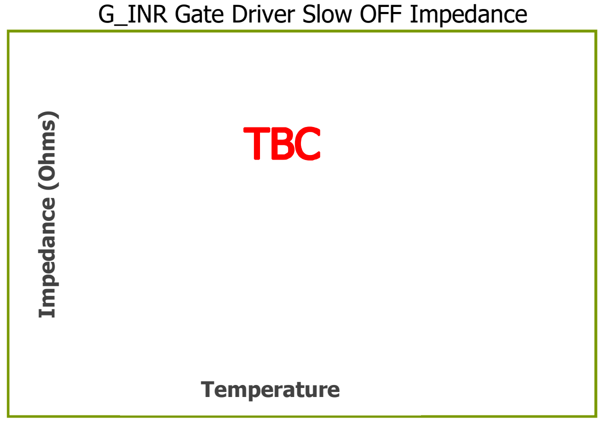
G_INR Gate Driver ON Impedance



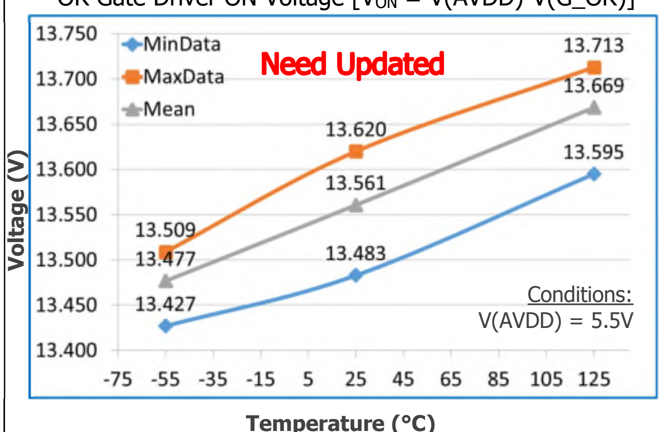
INR Gate Driver ON Voltage
[V_{ON} = V(AVDD)-V(G_INR)]



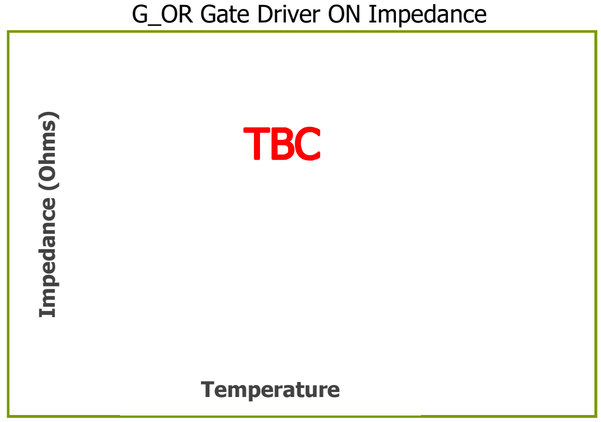
G_INR Gate Driver Slow OFF Impedance



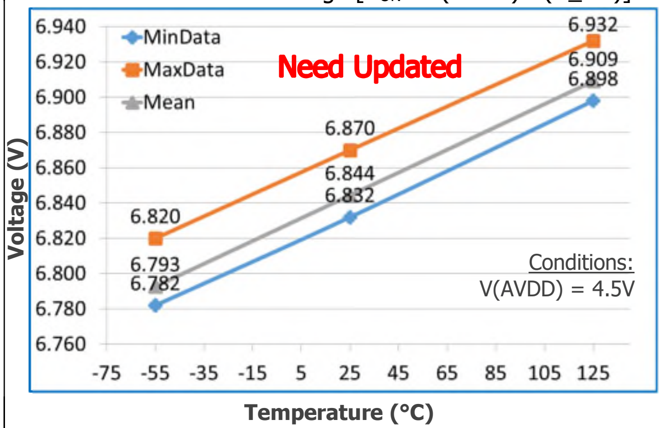
OR Gate Driver ON Voltage [V_{ON} = V(AVDD)-V(G_OR)]



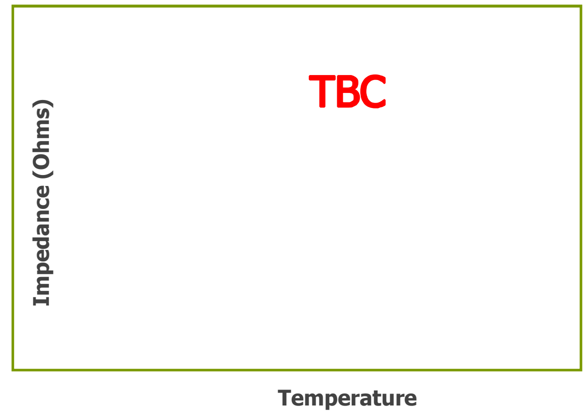
G_OR Gate Driver ON Impedance



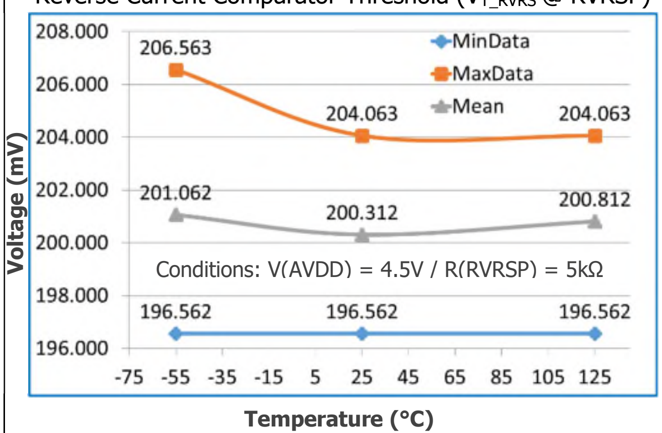
OR Gate Driver ON Voltage [V_{ON} =V(AVDD)-V(G_OR)]



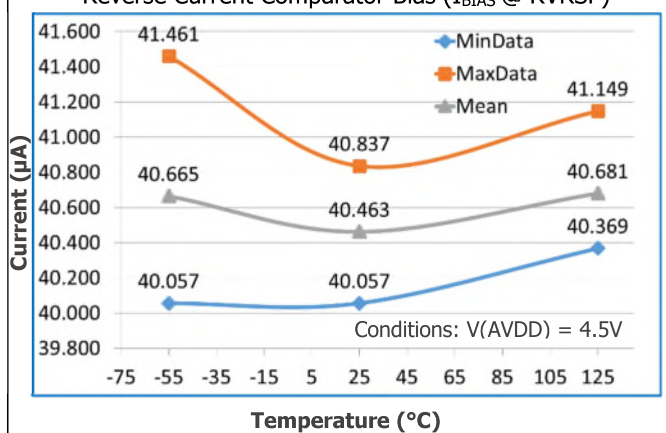
G_OR Gate Driver Slow OFF Impedance



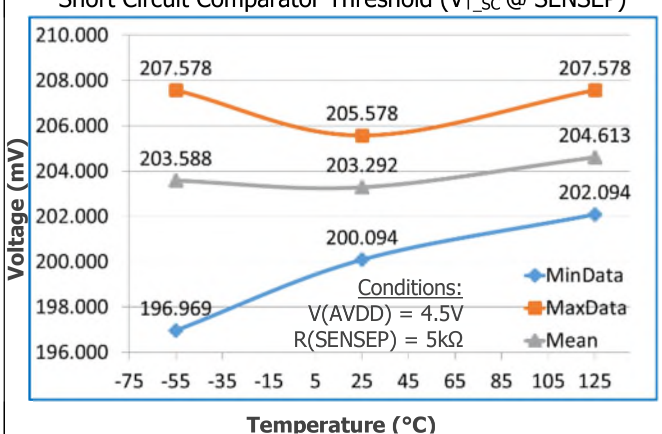
Reverse Current Comparator Threshold (V_{T_RVRS} @ RVRSP)



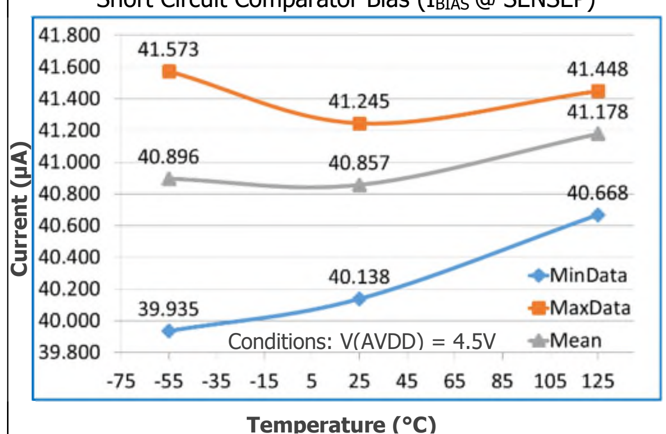
Reverse Current Comparator Bias (I_{BIAS} @ RVRSP)



Short Circuit Comparator Threshold (V_{T_SC} @ SENSEP)



Short Circuit Comparator Bias (I_{BIAS} @ SENSEP)



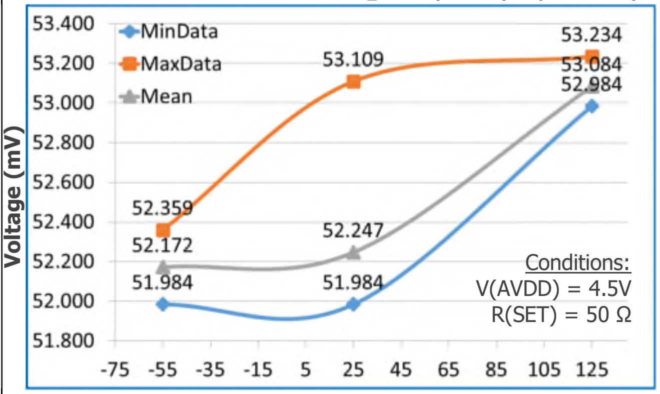
Current Sense Amplifier Gain Error

% (Measured IMON/1mA)

IMON @ V_{T_CL} = 25mV
IMON @ V_{T_CL} = 50mV
IMON @ V_{T_CL} = 50mV

Temperature

Overcurrent Limit Threshold [V_{T_CL} =V(AVDD)-V(SENSEM)]



Temperature (°C)

C_FAULT Charge Time (Δ 1V)

Time

ΔT @ Δ1V; C_FAULT = OPEN
ΔT @ Δ1V; C_FAULT = 10nF
ΔT @ Δ1V; C_FAULT = 100nF

Temperature

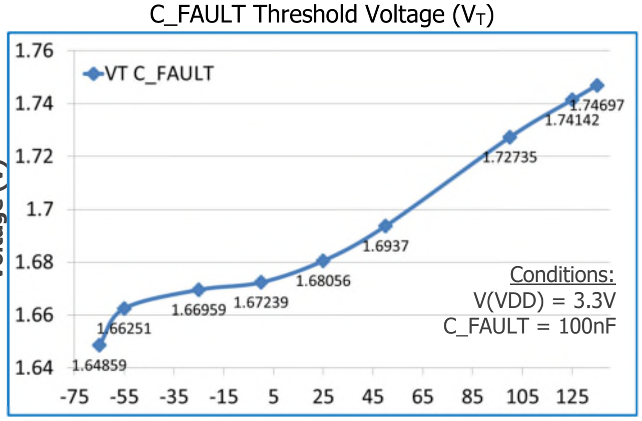
C_FAULT Discharge Time (Δ 1V)

Time

ΔT @ Δ1V; C_FAULT = OPEN
ΔT @ Δ1V; C_FAULT = 10nF
ΔT @ Δ1V; C_FAULT = 100nF

VDD

C_FAULT Threshold Voltage (V_T)



Temperature (°C)

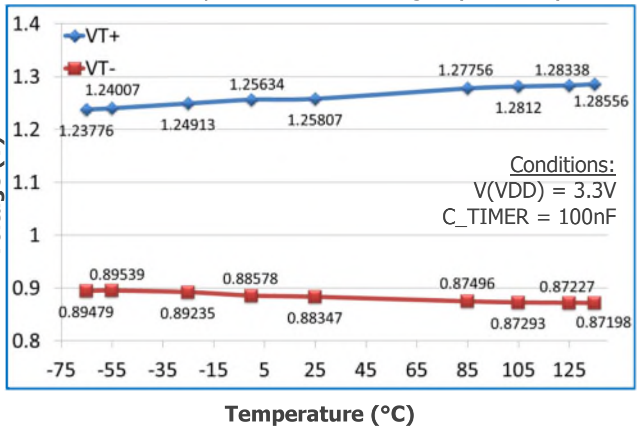
C_FAULT Charging Current

Current (uA)

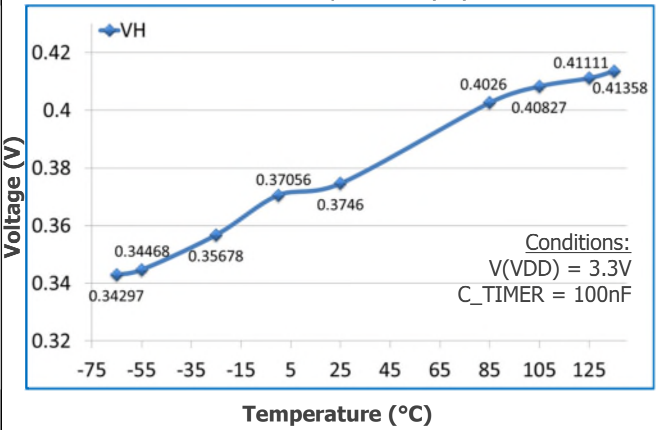
TBC

Temperature

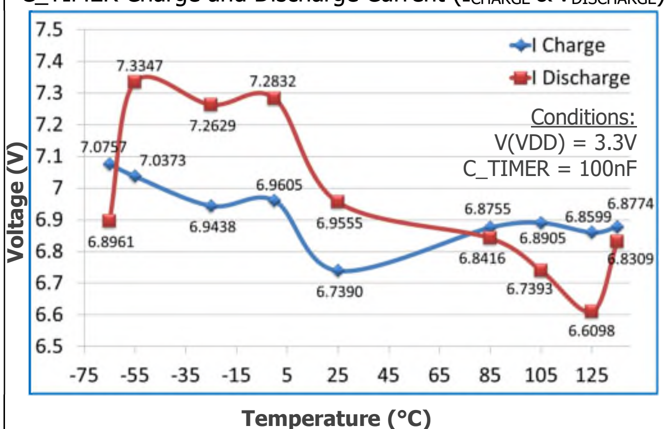
C_TIMER Input Threshold Voltages (V_{T+} & V_{T-})



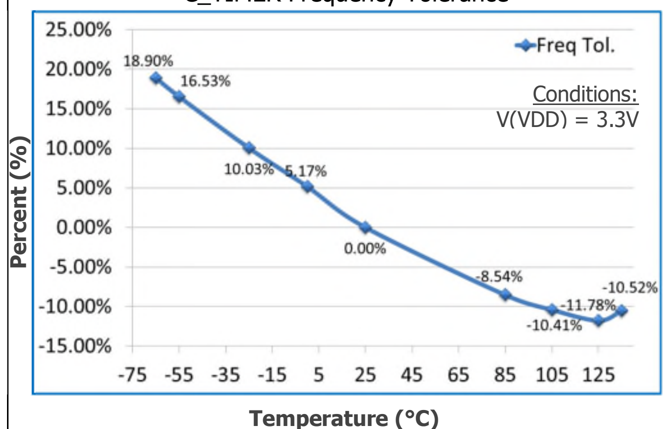
C_TIMER Hysteresis (V_H)



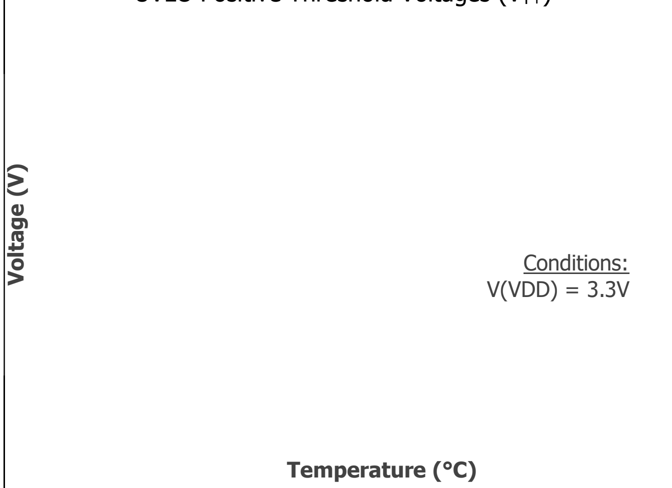
C_TIMER Charge and Discharge Current (I_{CHARGE} & $V_{DISCHARGE}$)



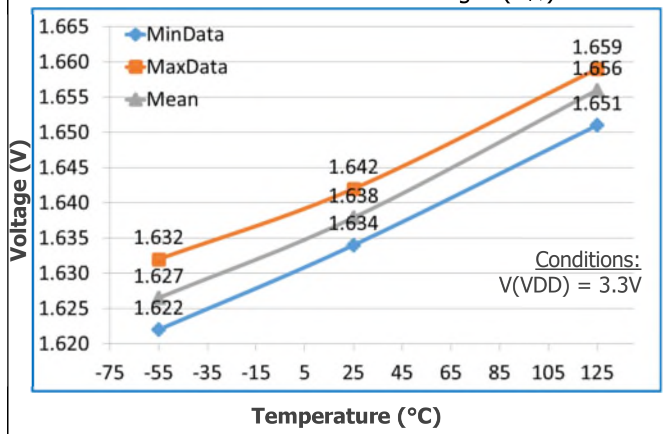
C_TIMER Frequency Tolerance



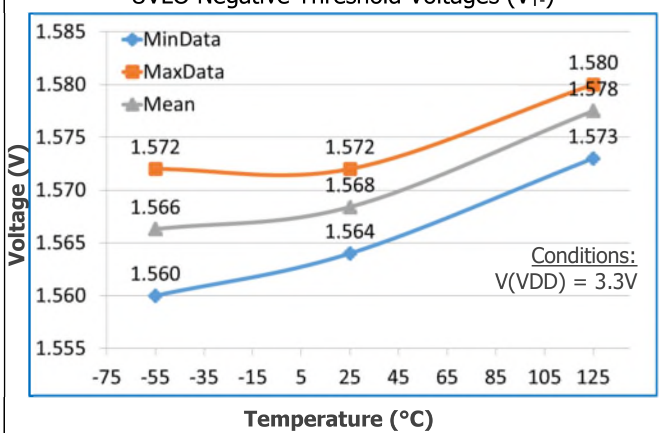
UVLO Positive Threshold Voltages (V_{T+})



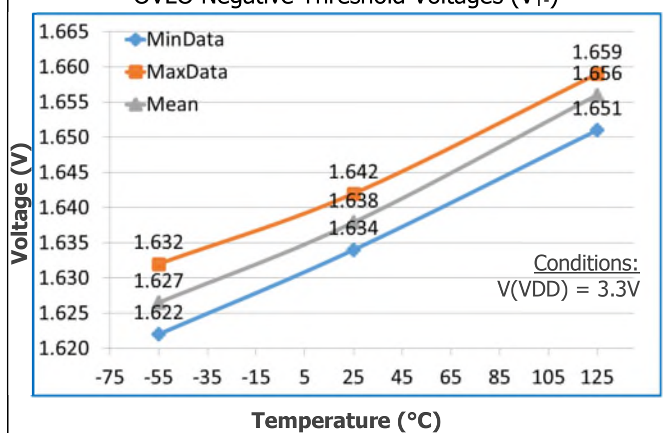
OVLO Positive Threshold Voltages (V_{T+})



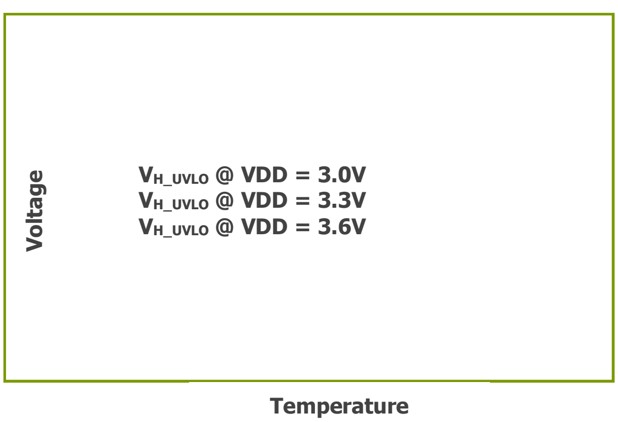
UVLO Negative Threshold Voltages (V_{T-})



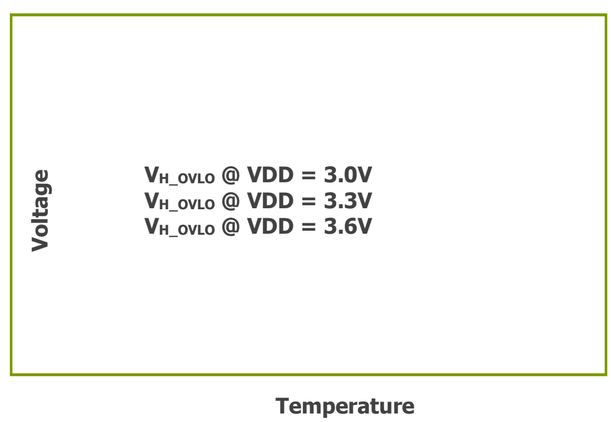
OVLO Negative Threshold Voltages (V_{T-})



UVLO Voltage Hysteresis



OVLO Voltage Hysteresis



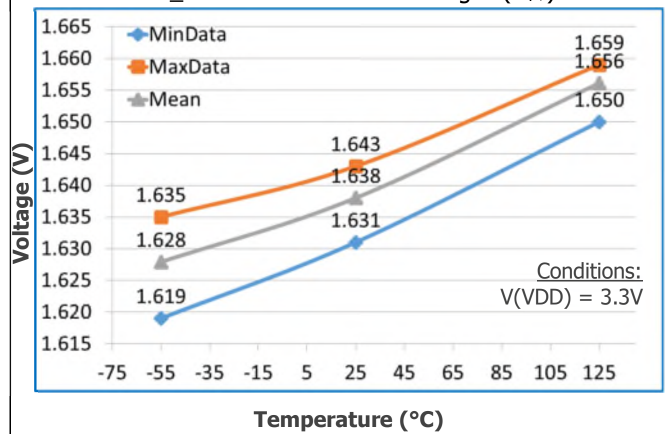
FEEDBACK Positive Threshold Voltages (V_{T+})

Voltage (V)

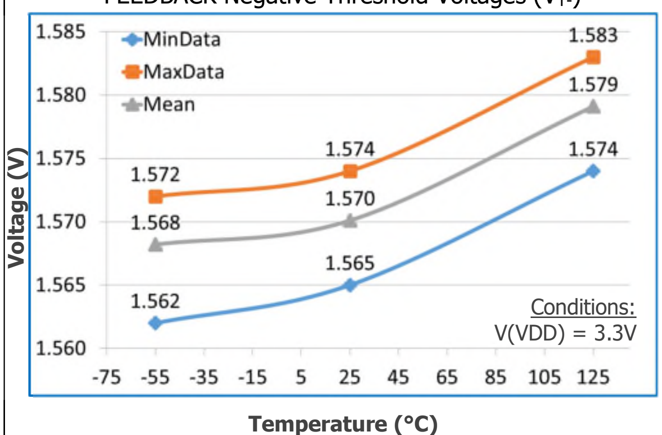
Conditions:
V(VDD) = 3.3V

Temperature (°C)

EN_B Positive Threshold Voltages (V_{T+})



FEEDBACK Negative Threshold Voltages (V_{T-})



EN_B Negative Threshold Voltages (V_{T-})

Voltage (V)

Conditions:
V(VDD) = 3.3V

Temperature (°C)

FEEDBACK Voltage Hysteresis

TBC

Voltage

$V_{H\_FEEDBACK}$ @ VDD = 3.0V
$V_{H\_FEEDBACK}$ @ VDD = 3.3V
$V_{H\_FEEDBACK}$ @ VDD = 3.6V

Temperature

EN_B Voltage Hysteresis

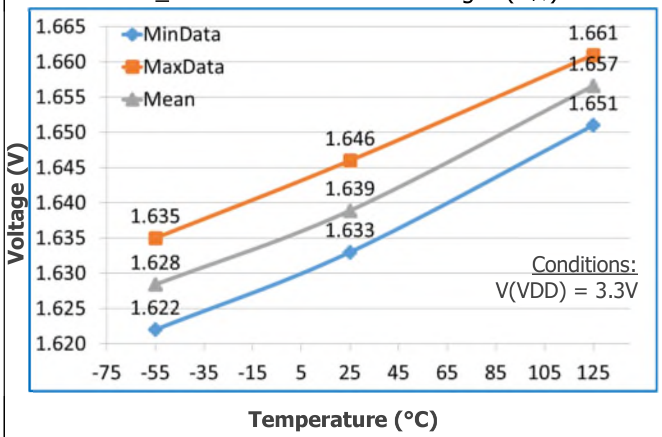
TBC

Voltage

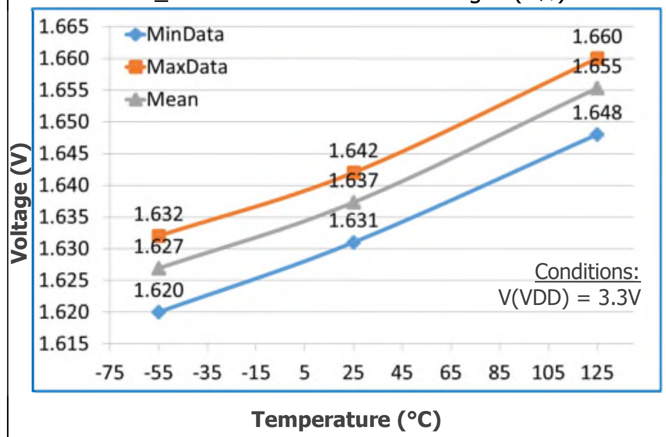
$V_{H\_EN\_B}$ @ VDD = 3.0V
$V_{H\_EN\_B}$ @ VDD = 3.3V
$V_{H\_EN\_B}$ @ VDD = 3.6V

Temperature

EN_OR Positive Threshold Voltages (V_{T+})



EN_INR Positive Threshold Voltages (V_{T+})



EN_OR Negative Threshold Voltages (V_{T-})

Voltage (V)

Conditions:
V(VDD) = 3.3V

Temperature (°C)

EN_INR Negative Threshold Voltages (V_{T-})

Voltage (V)

Conditions:
V(VDD) = 3.3V

Temperature (°C)

EN_OR Voltage Hysteresis

Voltage

$V_{H\_EN\_OR}$ @ VDD = 3.0V
$V_{H\_EN\_OR}$ @ VDD = 3.3V
$V_{H\_EN\_OR}$ @ VDD = 3.6V

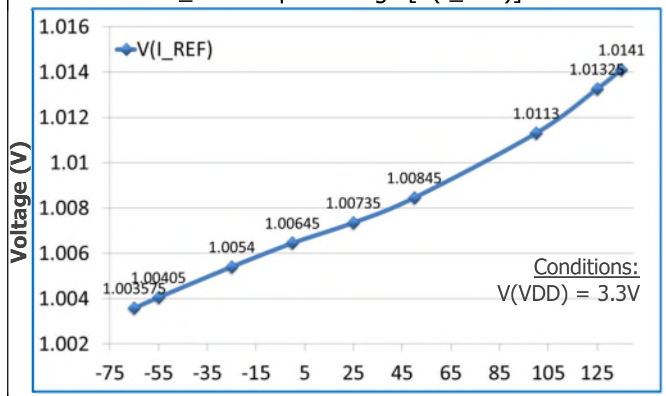
Temperature

EN_INR Voltage Hysteresis

Voltage

$V_{H\_EN\_INR}$ @ VDD = 3.0V
$V_{H\_EN\_INR}$ @ VDD = 3.3V
$V_{H\_EN\_INR}$ @ VDD = 3.6V

Temperature

IMON Input Voltage Threshold	I_REF Output Voltage [V(I_REF)]
TBC Voltage V_{IMON} @ VDD = 3.0V V_{IMON} @ VDD = 3.3V V_{IMON} @ VDD = 3.6V Temperature	 Temperature (°C)

VIN Pin Current to AGND

TBC

I_{VIN} @ V_{VIN} = 40V
I_{VIN} @ V_{VIN} = 20V
I_{VIN} @ V_{VIN} = 10V

Current

Temperature

VOUT Pin Current to AGND

TBC

I_{VOUT} @ V_{VOUT} = 40V
I_{VOUT} @ V_{VOUT} = 20V
I_{VOUT} @ V_{VOUT} = 10V

Current

Temperature

Active Single Supply Current

TBC

AI_{AVDD} @ AVDD = 8V
AI_{AVDD} @ AVDD = 28V
AI_{AVDD} @ AVDD = 36V

Current

Temperature

Active Dual Supply Current

TBC

AI_{AVDD} @ AVDD = 8V; VDD = 3.0V
AI_{VDD} @ AVDD = 8V; VDD = 3.0V
AI_{AVDD} @ AVDD = 28V; VDD = 3.3V
AI_{VDD} @ AVDD = 28V; VDD = 3.3V
AI_{AVDD} @ AVDD = 36V; VDD = 3.6V
AI_{VDD} @ AVDD = 36V; VDD = 3.6V

Current

Temperature

Sleep Single Supply Current

TBC

SI_{AVDD} @ AVDD = 8V
SI_{AVDD} @ AVDD = 28V
SI_{AVDD} @ AVDD = 36V

Current

Temperature

Sleep Dual Supply Current

TBC

SI_{AVDD} @ AVDD = 8V; VDD = 3.0V
SI_{VDD} @ AVDD = 8V; VDD = 3.0V
SI_{AVDD} @ AVDD = 28V; VDD = 3.3V
SI_{VDD} @ AVDD = 28V; VDD = 3.3V
SI_{AVDD} @ AVDD = 36V; VDD = 3.6V
SI_{VDD} @ AVDD = 36V; VDD = 3.6V

Current

Temperature

Regulated VDD from Single Supply

TBC

VDD @ AVDD = 8V
VDD @ AVDD = 28V
VDD @ AVDD = 36V

Voltage

Temperature

VIN Accuracy at ADC Output

TBC

$\%VIN_{ACCURACY}$ @ VDD = 3.3V; Temp = 25°C
$\%VIN_{ACCURACY}$ @ VDD = 3.6V; Temp = -55°C
$\%VIN_{ACCURACY}$ @ VDD = 3.0V; Temp = 125°C

%

VIN

VOUT Accuracy at ADC Output

TBC

$\%VOUT_{ACCURACY}$ @ VDD = 3.3V; Temp = 25°C
$\%VOUT_{ACCURACY}$ @ VDD = 3.6V; Temp = -55°C
$\%VOUT_{ACCURACY}$ @ VDD = 3.0V; Temp = 125°C

%

VOUT

IMON Accuracy at ADC Output for 25mV V_{T_CL}

TBC

$\%IMON_{ACCURACY}$ @ VDD = 3.3V; Temp = 25°C
$\%IMON_{ACCURACY}$ @ VDD = 3.6V; Temp = -55°C
$\%IMON_{ACCURACY}$ @ VDD = 3.0V; Temp = 125°C

%

IMON

IMON Accuracy at ADC Output for 50mV V_{T_CL}

TBC

$\%IMON_{ACCURACY}$ @ VDD = 3.3V; Temp = 25°C
$\%IMON_{ACCURACY}$ @ VDD = 3.6V; Temp = -55°C
$\%IMON_{ACCURACY}$ @ VDD = 3.0V; Temp = 125°C

Frequency

Temperature

IMON Accuracy at ADC Output for 100mV V_{T_CL}

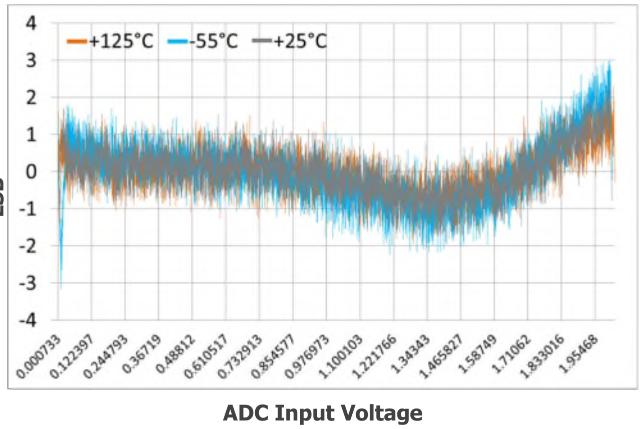
TBC

$\%IMON_{ACCURACY}$ @ VDD = 3.3V; Temp = 25°C
$\%IMON_{ACCURACY}$ @ VDD = 3.6V; Temp = -55°C
$\%IMON_{ACCURACY}$ @ VDD = 3.0V; Temp = 125°C

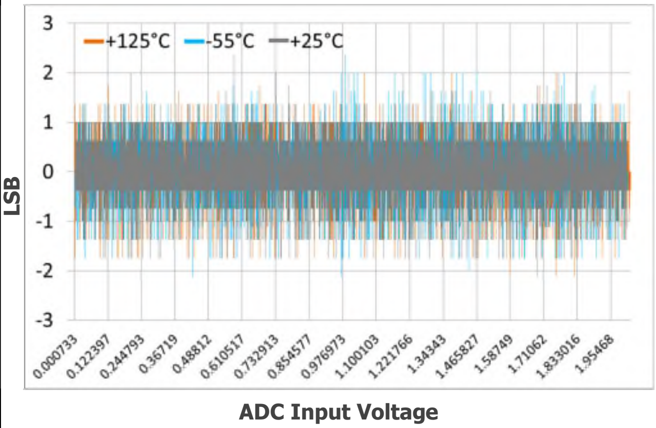
Voltage

Temperature

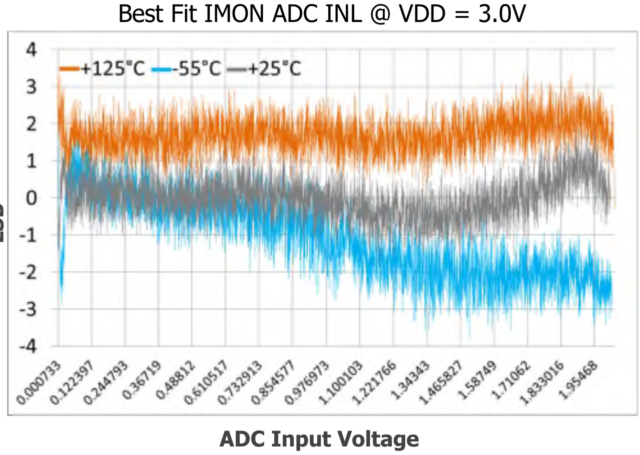
Best Fit IMON ADC INL @ VDD=3.3V



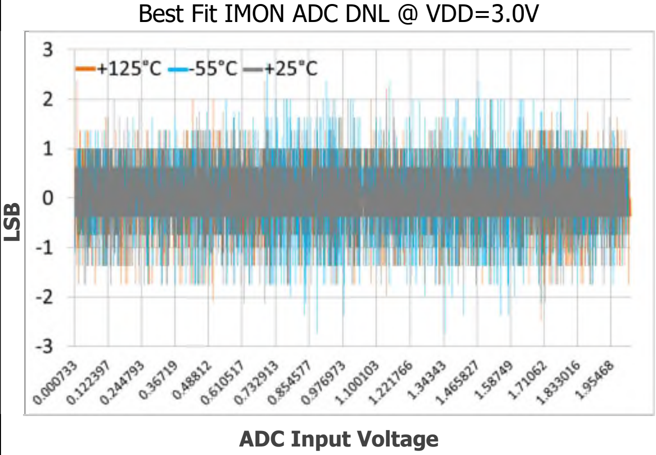
Best Fit IMON ADC DNL @ VDD=3.3V



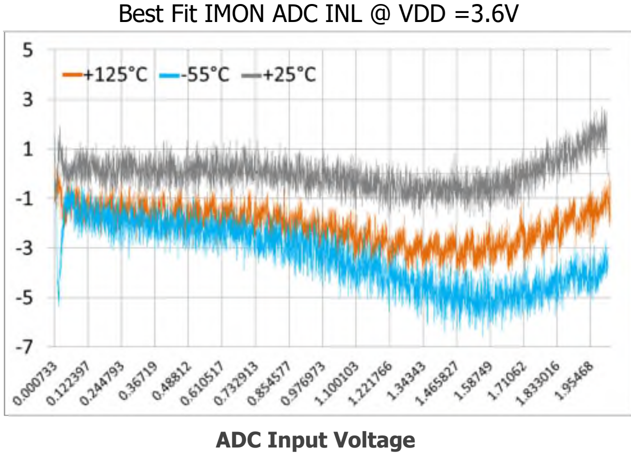
Best Fit IMON ADC INL @ VDD = 3.0V



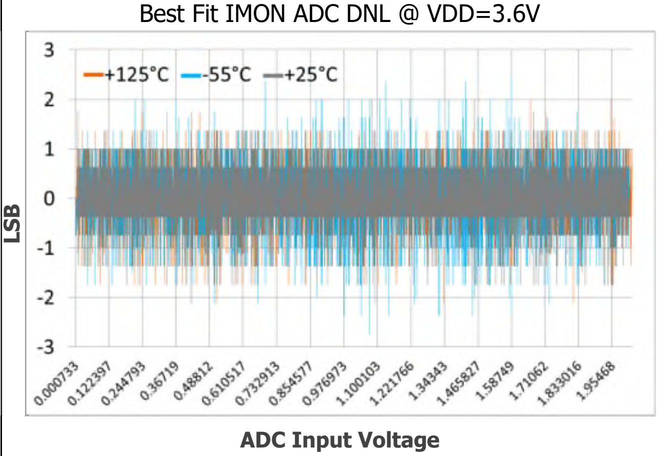
Best Fit IMON ADC DNL @ VDD=3.0V



Best Fit IMON ADC INL @ VDD =3.6V



Best Fit IMON ADC DNL @ VDD=3.6V



	ADC Differential Non-Linearity DNL @ VDD = 3.3V; Temp = 25°C LSB Voltage
	ADC Gain Error ERR_{GAIN} @ VDD = 3.0V ERR_{GAIN} @ VDD = 3.3V ERR_{GAIN} @ VDD = 3.6V LSB Temperature
	ADC Offset Error ERR_{OFFSET} @ VDD = 3.0V ERR_{OFFSET} @ VDD = 3.3V ERR_{OFFSET} @ VDD = 3.6V LSB Temperature

13 Detailed Functional Description

The following sections detail the UT05PFD103 features and operational behavior in detail.

13.1 PMBus™ / SMBus Functional Description

Power Management Bus (PMBus™) is a powerful communication protocol standard finding extensive use in commercial power system management applications. PMBus™ applies a protocol transport layer to configure, control, and gather data & telemetry from targeted power system component via an SMBus network layer. The SMBus network layer of the protocol stack performs packetization and handles bus commands delivered over an I²C link and physical layer.

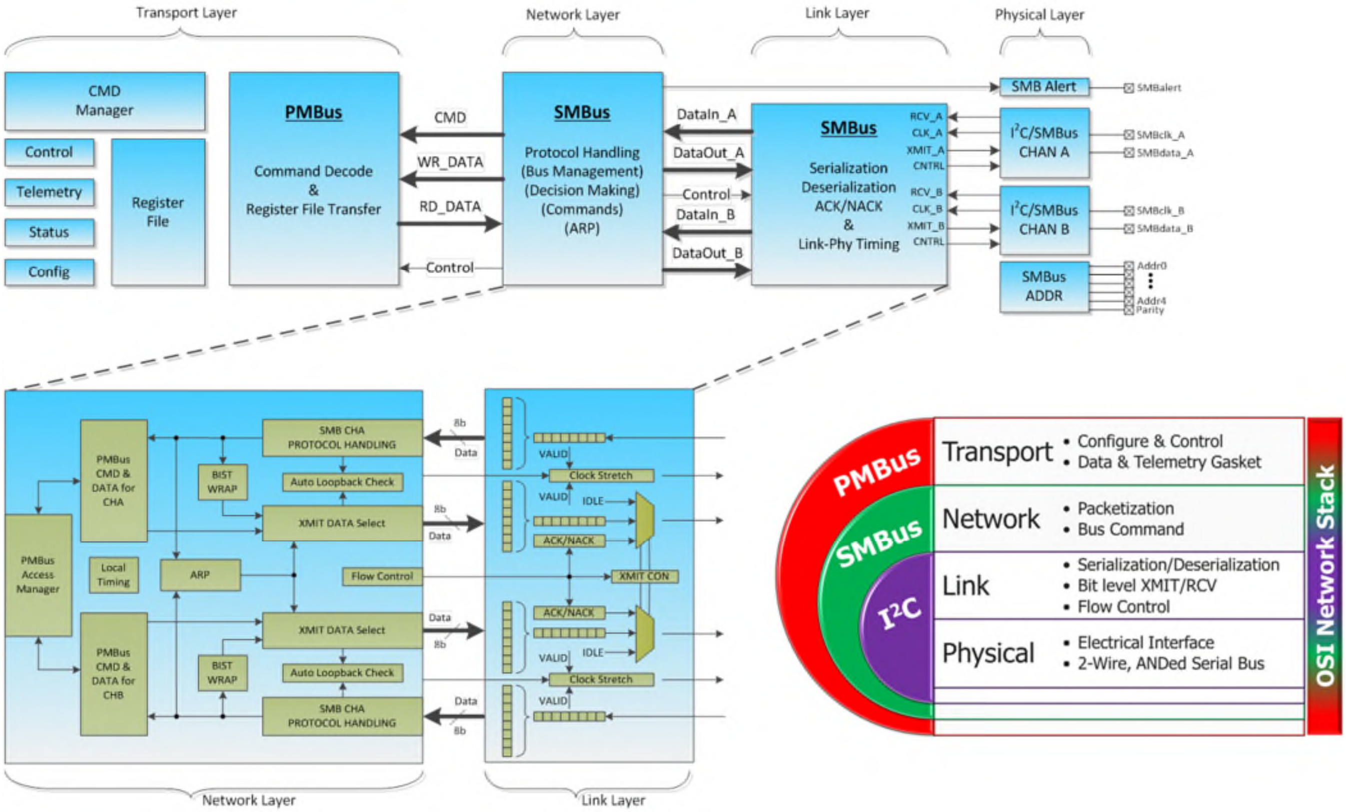


Figure 13-1. SPSC PMBus™ / SMBus Block Diagram

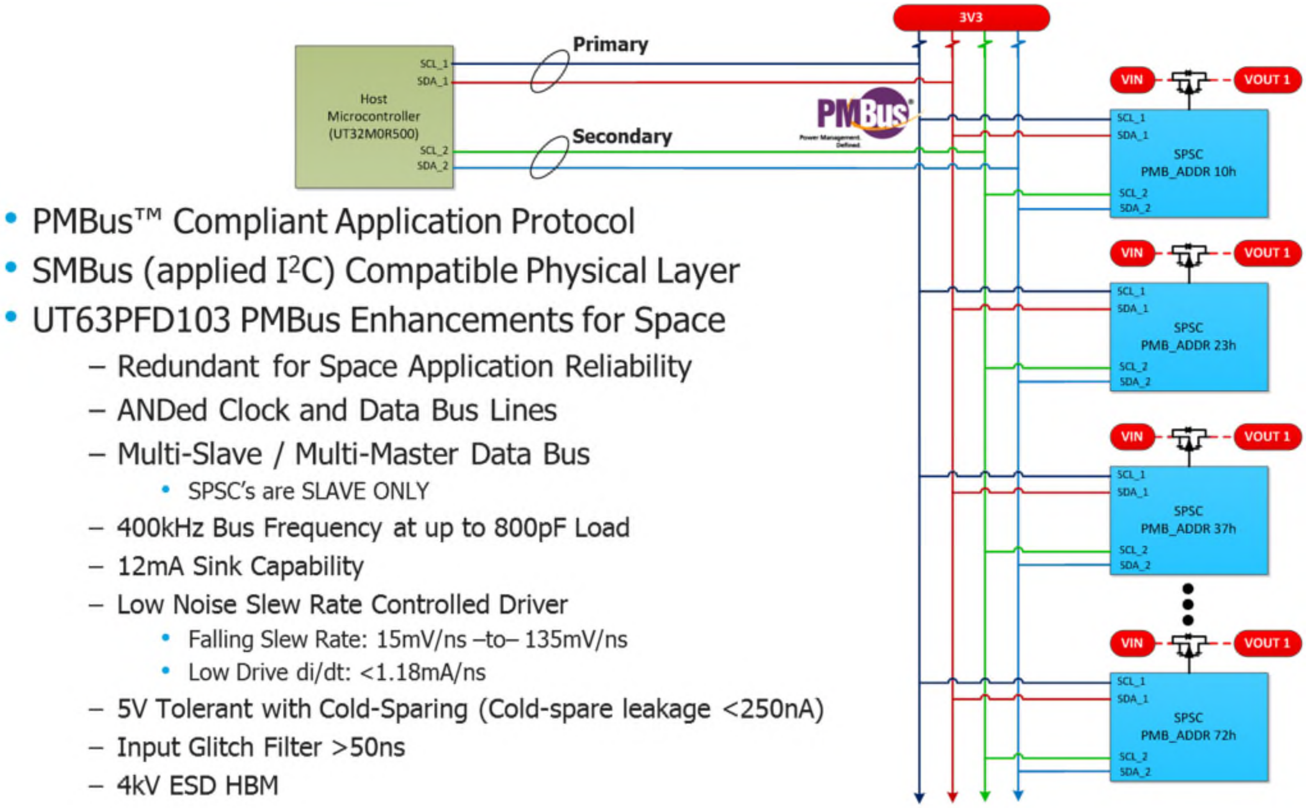


Figure 13-2. PMBus™ / SMBus System At a Glance

The I^{2}C link level protocol is a very simple 2-wire, AND'ed protocol which starts with an ADDRESS and DATA Direction byte followed by a packet of data being READ or WRITTEN. The following figures present typical I^{2}C communication. The SPSC supports 100 kbps Standard Mode (SM) and 400 kbps Fast-Mode (FM) I^{2}C data rates.

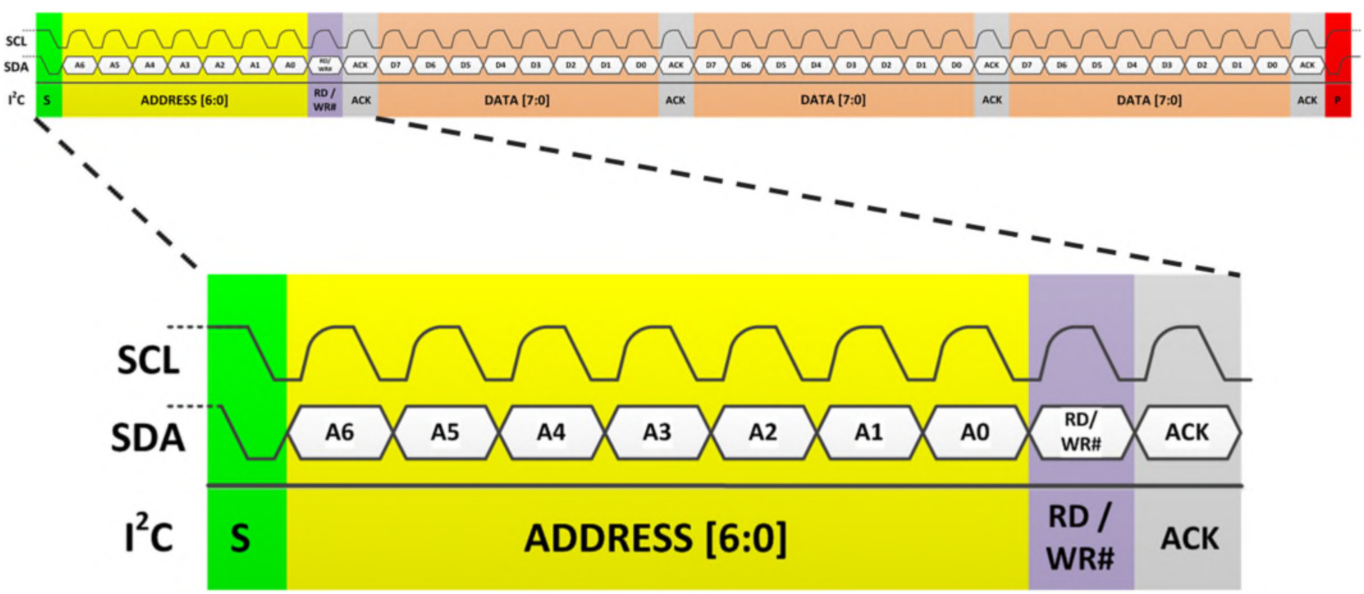


Figure 13-3. I^{2}C Address Byte Formatting

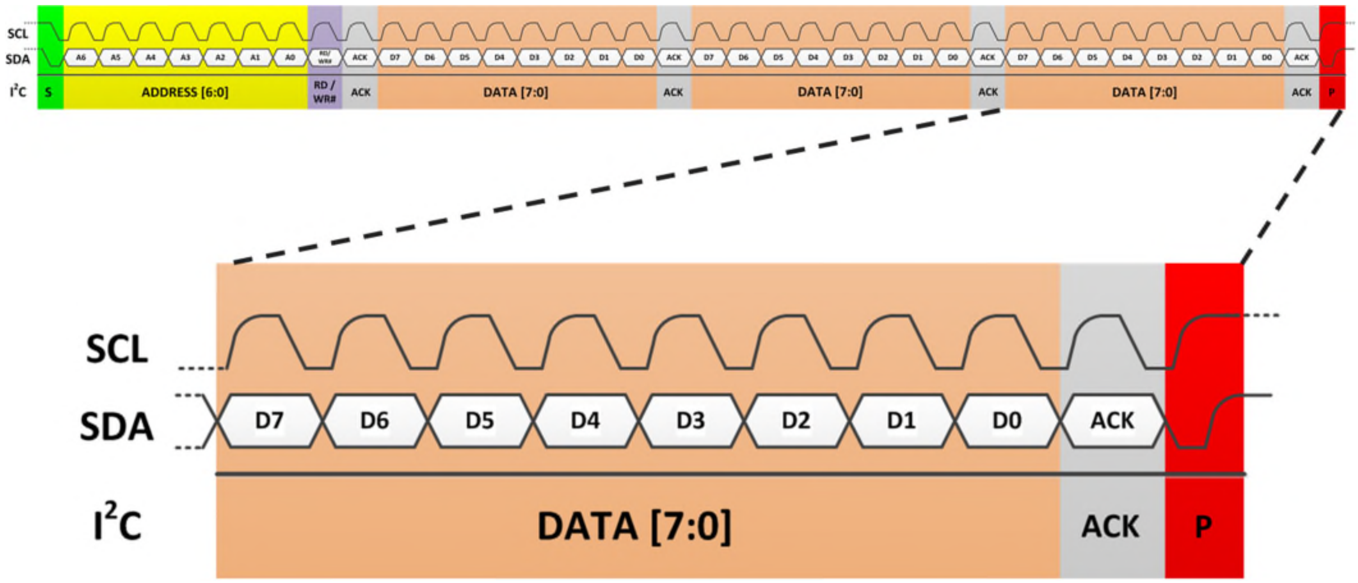


Figure 13-4. I^{2}C Data Byte Formatting

The SMBus protocol can be thought as "Applied I^{2}C". The following figure summarizes the SMBus application of the I^{2}C protocol for the purpose of facilitating PMBus™ interactions with the SPSC. For the purpose of fault tolerance, the SPSC supports a redundant pair of SMBus ports, each of which can coherently interact with the PMBus layer.

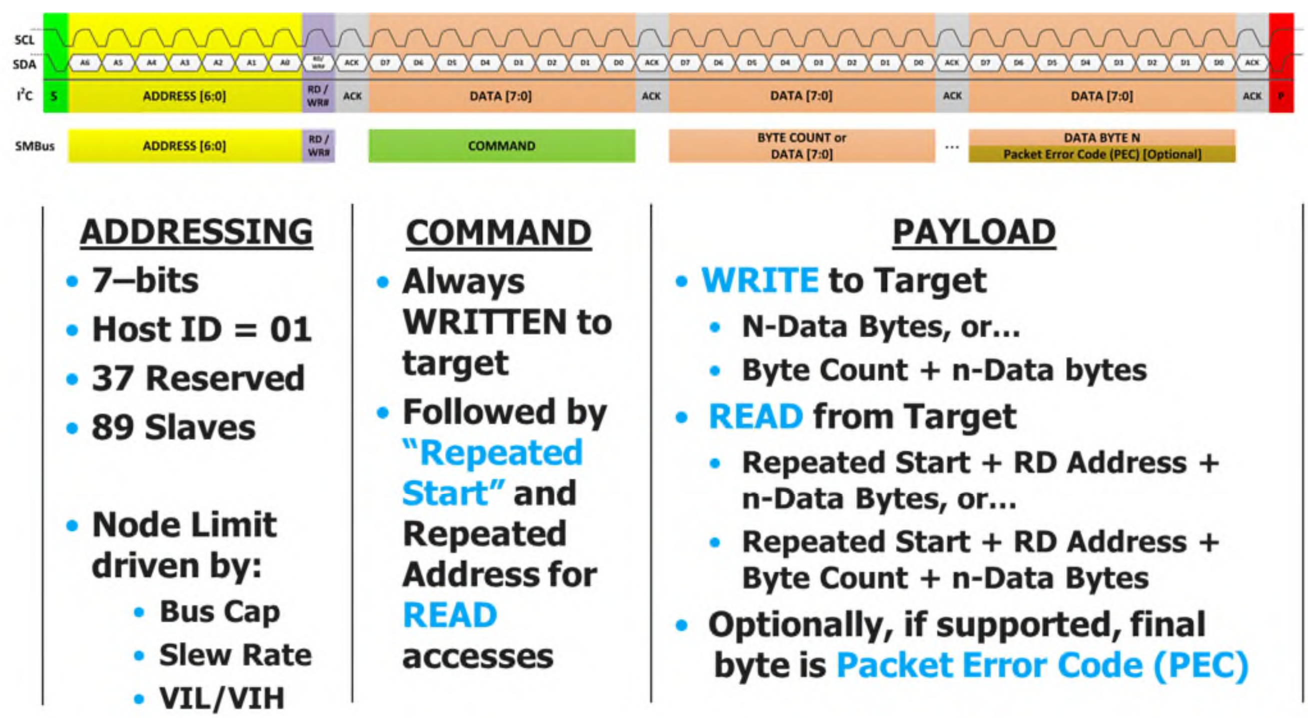
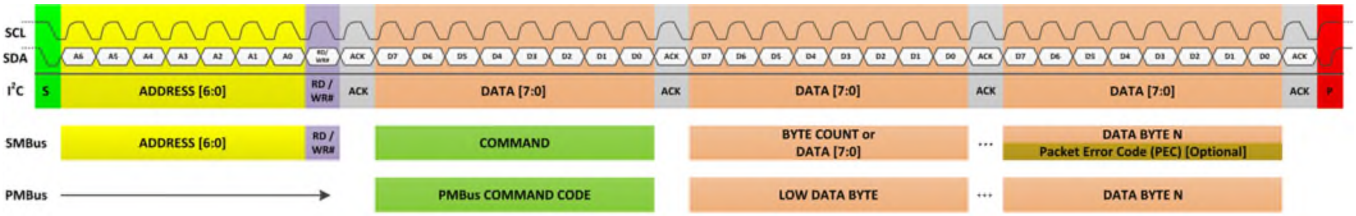


Figure 13-5. SMBus Network Layer Protocol Formatting Summary

Finally, the PMBus™ Transport layer of the network stack manages the actual register manipulations within the SPSC for the purpose of configuring, controlling, and gathering data & telemetry from the SPSC. The SPSC supports 11 PMBus™ commands.



PMBus COMMAND and DATA Examples

Command Code	Command Name	Write Size	Read Size	PMBus Spec. Reference
01h	OPERATION	Write Byte	Read Byte	12.1
03h	CLEAR_FAULTS	N/A	N/A	15.1
19h	CAPABILITY	N/A	Read Byte	11.12
47h	IOUT_OC_FAULT_RESPONSE	Write Byte	Read Byte	15.9
7Ah	STATUS_VOUT	Write Byte	Read Byte	17.3
7Bh	STATUS_IOUT	Write Byte	Read Byte	17.4
7Ch	STATUS_INPUT	Write Byte	Read Byte	17.5
88h	READ_VIN	N/A	Read Word	18.1
8Bh	READ_VOUT	N/A	Read Word	18.4
8Ch	READ_IOUT	N/A	Read Word	18.5
D0h	GATE_OFF_DELAY	Write Byte	Read Byte	N/A
D1h	GATE_ON_DELAY	Write Byte	Read Byte	N/A

Figure 13-6. PMBus Protocol Formatting and Supported Commands

13.1.1 PMBus™ Command Definitions

Command: 01h OPERATION (BYTE READ and WRITE)

Description: The OPERATION command sets top level configuration bits for the SPSC and STARTS and STOPS ORFET and HSFET operation.

Bit	Function
7	•ON/OFF# - Ignored if PMB_EN pin is low WRITE: 0 = FET Gates OFF 1 = FET Gates ON, if all other operating conditions are valid READ: Reflects ON/OFF# state of HSFET Only
6	•Enable Selected Fault Controls 0 = Act on all valid fault conditions 1 = Act on faults set by selected fault enabling
5:4	•Reserved
3:2	•Enable Selected Fault Responses 00, 01, 10 = Act on all valid faults 11 = Do not act on OV or UV faults •Note: Current faults are ALWAYS acted upon
1	•SMBAlert Enable: 0 = Disabled 1 = Enabled
0	•Pulse Enable: 0 = Pulse mode disabled, normal operation enabled 1 = Pulse mode enabled, INR_G timed pulsing ON/OFF

Command: 03h CLEAR_FAULTS (WRITE-only / No Data Included)

- The CLEAR_FAULTS command is a WRITE-ONLY command with NO DATA included.

- The CLEAR_FAULTS command is used to clear any fault bits that have been set.
- This command clears all bits in all status registers simultaneously.
- At the same time, the device negates (clears, releases) its SMBALERT# signal output if the device is asserting the SMBALERT# signal.
- The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart.
  - Units that have shut down for a fault condition are restarted by usual means.
  - If the fault is still present when the bit is cleared, the fault bit immediately sets again and the host is notified by the usual means.

Command: 19h CAPABILITY (BYTE READ)

7	6	5	4	3	2	1	0

Description: The CAPABILITY command allows the system host to determine key capabilities of SPSC PMBus/SMBus functionality

- Bits 1:0 — •Reserved:
  00 = Always read as 00
- Bit 2 — •AVSBus Support:
  0 = AVSBus Not Supported
- Bit 3 — •Numeric Format
  0 = Numeric Format is DIRECT
- Bit 4 — •SMBALERT#
  1 = The device does have a SMBALERT# pin and does support the SMBus Alert Response protocol.
- Bits 6:5 — •Maximum Bus Speed
  01 = Maximum supported bus speed is 400kHz
- Bit 7 — •Packet Error Checking
  1 = Packet Error Checking is supported

Command: 47h IOUT_OC_FAULT_RESPONSE (BYTE READ and WRITE)

7	6	5	4	3	2	1	0

Description: This command configures the SPSC response in the event of an OC fault.

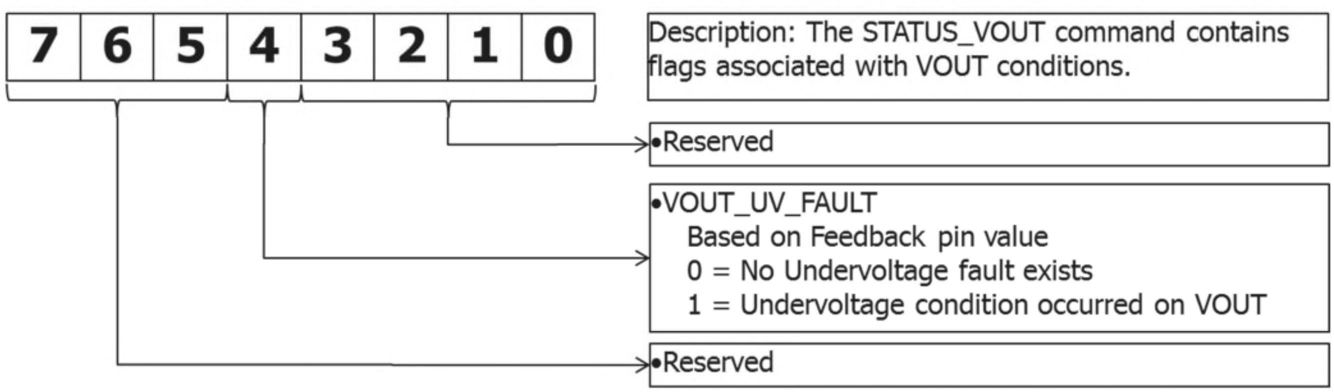
- Bits 2:0 — •Retry Delay Time
  The time unit is set by C_TIMER
  000b-111b = 1-8 time units delay before retry
- Bits 5:3 — •Retry (Retrigger Mode) Count
  000 = No retries shall be attempted (Latch Mode)
  001-110 = Retry 1 to 6 times
  111 = Continue to retry indefinitely
- Bits 7:6 — •SPSC Overcurrent Response
  These bits are permanently set to 11b.
  11 = Informs device to respond to OC faults in accordance with settings in bits 5:0
  • Note: Retries are NOT used if a Short Circuit or Reverse Current fault occurs. In such a case, the host must restart operation by asserting bit 7 of the OPERATION register.

Table 13-1. Actual Retry Delay Values

Command 47H Retry_Delay Time Value	+ Delay Offset	= Actual Cool-off Period (# of CLK_ADJ Periods)
0 (000b)	+2.5 to +3.5	2.5 to 3.5
1 (001b)	+1.5 to +2.5	2.5 to 3.5
2 (010b)	+0.5 to +1.5	2.5 to 3.5
3 (011b)	+0.5 to +1.5	3.5 to 4.5
4 (100b)	+0.5 to +1.5	4.5 to 5.5
5 (101b)	+0.5 to +1.5	5.5 to 6.5
6 (110b)	+0.5 to +1.5	6.5 to 7.5
7 (111b)	+0.5 to +1.5	7.5 to 8.5

**Note that the typical delay offset of "0.5 to 1.5" is due to the sampling of the current fault latch on the next falling edge of the user's adjustable clock period (C_TIMER), following the 2-period sampling the SPSC's internal 1.5Mhz clock. The 1.5Mhz sampling is required to synchronize the current fault latch before turning off the G_INR FET driver.

Command: 7Ah   STATUS_VOUT   (BYTE READ and WRITE)



Notes:

- VOUT_UV_FAULT is ONLY set when the FEEDBACK input transitions from HIGH-to-LOW
- If no preceding fault exists at the time VOUT_UV_FAULT sets, then it will be the source of the SMBAlert# assertion

Command: 7Bh STATUS_IOUT (BYTE READ and WRITE)

7	6	5	4	3	2	1	0

Description: The STATUS_IOUT command contains flags associated with IOUT conditions

- Bits 2:0 — Reserved
- Bit 3 — IOUT_SC_FAULT (i.e. High-Current Fault)
  - 0 = No fault is detected
  - 1 = Short/high-current fault has occurred
- Bit 4 — IOUT_UC_FAULT (i.e. Reverse Current Fault)
  - 0 = No fault is detected
  - 1 = Undercurrent fault has occurred
- Bits 6:5 — Reserved
- Bit 7 — IOUT_OC_FAULT
  - 0 = No fault is detected
  - 1 = Overcurrent fault timeout occurred on IOUT

Command: 7Ch STATUS_INPUT (BYTE READ and WRITE)

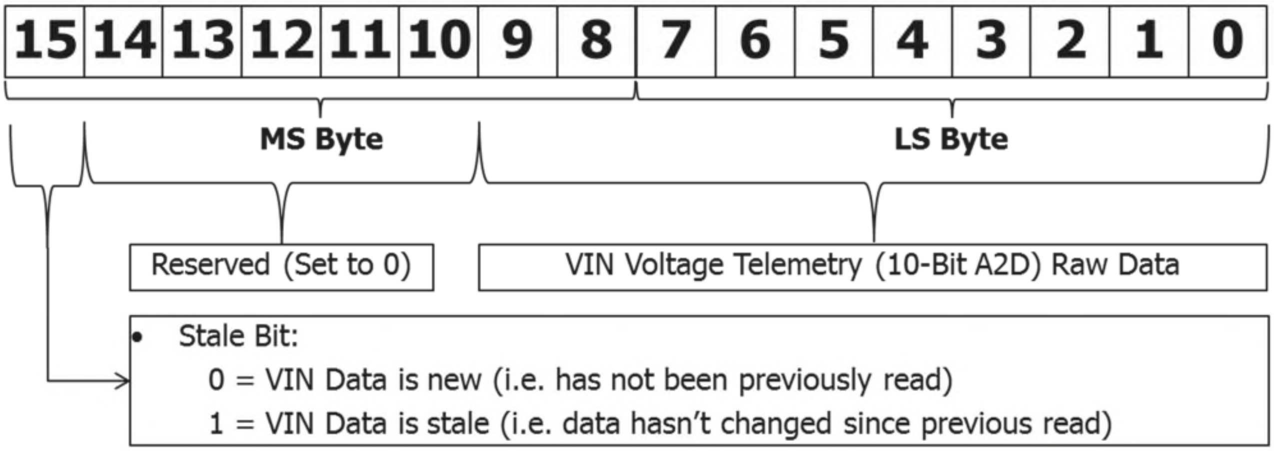
7	6	5	4	3	2	1	0

Description: The STATUS_INPUT command contains flags associated with VIN conditions

- Bits 2:0 — Reserved
- Bit 3 — INSUFFICIENT_DEV_POWER
  - 0 = No fault is detected
  - 1 = Power domain within device is out of spec low
- Bit 4 — VIN_UV_FAULT
  - 0 = No fault is detected
  - 1 = UVLO pin is low (Undervoltage)
- Bits 6:5 — Reserved
- Bit 7 — VIN_OV_FAULT
  - 0 = No fault is detected
  - 1 = OVLO pin is high (Overvoltage)

Command: 88h READ_VIN (WORD READ-only)

Description: The READ_VIN command provides a two-byte (word) data value representing the converted output of the 10-bit A2D. Data is in the PMBus DIRECT data format.



$$X(V) = \frac{39.065mV}{bit} * READ\_VIN_{10}$$

Example:

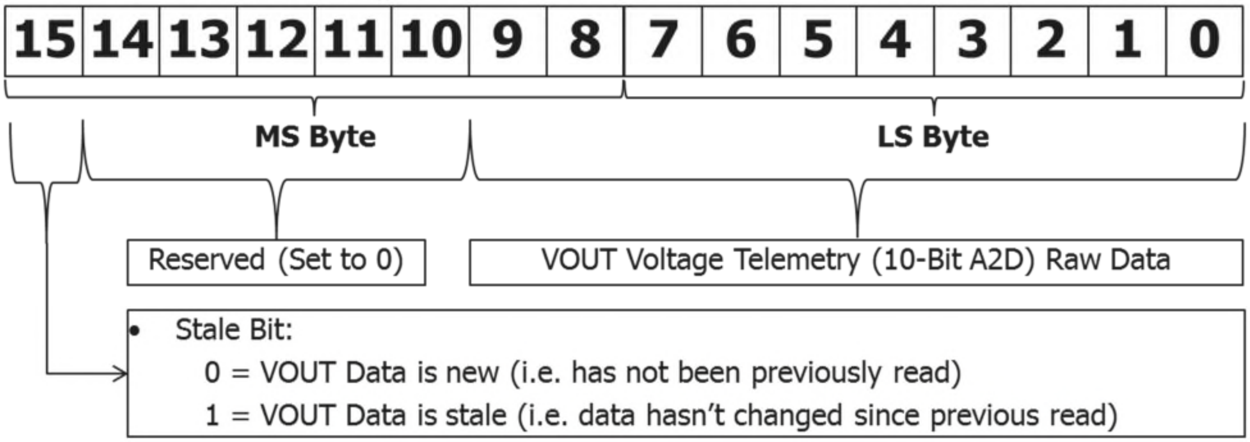
READ_VIN = 03FFh (1023_{10}) then:

$$X_{VIN} = .039065 * 1023 = 39.9635V$$

**Note: The data structure shown above is after constructing the 16-bit word received over the SMBus "READ WORD" protocol were data comes over the bus as LOW byte bits 7..0 followed by HIGH byte bits 15..8.

Command: 8Bh READ_VOUT (WORD READ-only)

Description: The READ_VOUT command provides a two-byte (word) data value representing the converted output of the 10-bit A2D. Data is in the PMBus DIRECT data format.



$$X(V) = \frac{39.065mV}{bit} * READ\_VOUT_{10}$$

Example:

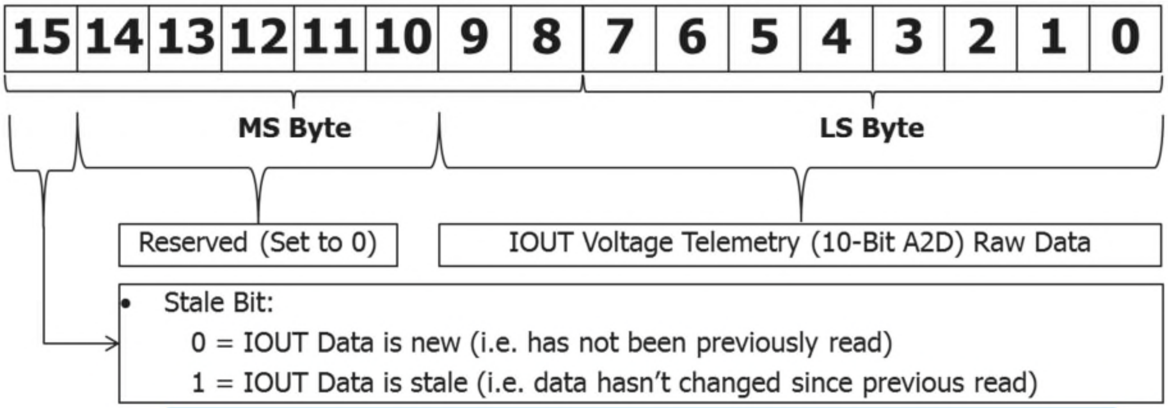
READ_VOUT = 02ADh (685_{10}) then:

$$X_{VOUT} = .039065 * 685 = 26.7595V$$

**Note: The data structure shown above is after constructing the 16-bit word received over the SMBus "READ WORD" protocol were data comes over the bus as LOW byte bits 7..0 followed by HIGH byte bits 15..8.

Command: 8Ch READ_IOUT (WORD READ-only)

Description: The READ_IOUT command provides a two-byte (word) data value representing the converted output of the 10-bit A2D. Data is in the PMBus DIRECT data format.



$$X(A) = \frac{R_{SET}}{R_{SENSE}} * \frac{ADC_{FS}}{R_{IMON}} * \frac{1}{1024} * READ\_IOUT_{10}$$

Example: $R_{SET} = 25\Omega; R_{SENSE} = 10m\Omega; R_{IMON} = 1.6k\Omega; ADC_{FS} = 2V;$
READ_IOUT = 0309h (777_{10}) then:

$$X_{IOUT} = \frac{25}{0.01} * \frac{2}{1600} * \frac{1}{1024} * 777 = 2.3712A$$

**Note: The data structure shown above is after constructing the 16-bit word received over the SMBus "READ WORD" protocol were data comes over the bus as LOW byte bits 7..0 followed by HIGH byte bits 15..8.

Command: D0h GATE_OFF_DELAY (BYTE READ and WRITE)

7	6	5	4	3	2	1	0

Description: The GATE_OFF_DELAY command sets the duration that the G_INR (Inrush FET Gate) is held in the "OFF" state.

- This command is only applicable when the PULSE_EN bit is set in the OPERATION register (OPERATION.0)

Bits 7:0:

- GATE_OFF_DELAY Time Counter
  The time unit is set by C_TIMER
  00h = 1 Time Unit
  •••
  FFh = 256 Time Units

Command: D1h GATE_ON_DELAY (BYTE READ and WRITE)

7	6	5	4	3	2	1	0

Description: The GATE_ON_DELAY command sets the duration that the G_INR (Inrush FET Gate) is held in the "ON" state.

- This command is only applicable when the PULSE_EN bit is set in the OPERATION register (OPERATION.0)

Bits 7:0:

- GATE_ON_DELAY Time Counter
  The time unit is set by C_TIMER
  00h = 1 Time Unit
  •••
  FFh = 256 Time Units

General Call Address: 00h / Command: 06h SOFT_RESET (WRITE-only)

Description: Address 00h is the General Call Address (GCA) which behaves as a "Broadcast" address to all slave devices that support the GCA. For the GCA, the SPSC supports only the SOFT_RESET command 06h.

Behavior:

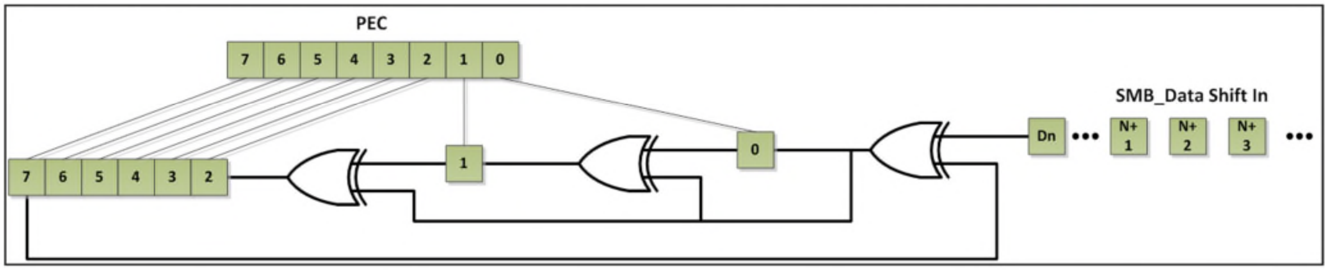
- Upon receipt of the GCA with WRITE bit, the SPSC provides and ACK and observes the COMMAND byte. If the COMMAND byte is anything other than 06h, the SPSC will NACK the message and return to wait for a new START bit.
- If the COMMAND byte is 06H, the SPSC will ACK the COMMAND byte and observe for a STOP bit or a valid PEC byte to follow.
- After receipt of the STOP bit or valid PEC with STOP bit, the SPSC will execute the SOFT_RESET.
- SOFT_RESET results in the following SPSC actions:
  - All resettable flops in the SPSC digital macro are reset

SMBus Packet Error Code (PEC)

- The UT36PFD103 Supports PEC verification on WRITE commands and PEC generation on READ commands
- SMBus PEC uses a CRC-8-CCITT algorithm
  - https://en.wikipedia.org/wiki/Cyclic_redundancy_check

$$C(x) = x^8 + x^2 + x + 1$$

- Logically, the CRC-8 Algorithm can be implemented according to the following circuit diagram with the initialization value of 00H:



- A simple C based algorithm using a CRC8 lookup table is located here:
  - https://www.3dbrew.org/wiki/CRC-8-CCITT

13.1.2 SMBus Ternary Addressing with Parity

Using 5 ternary address pins plus a binary parity pin, the SPSC supports addressing for every possible SMBus slave address. Unlike binary pins, ternary pins support three states: LOW, MID, HIGH. The choice of ternary IO was used to provide full 7-bit SMBus addressing with fewer pins. The SPSC supports PMBus™ plug & play through its implementation of the SMBus Address Resolution Protocol (ARP). If the SMBus address and parity are invalid or duplicate, the power SMBus host is responsible for ARP'ing to determine which valid terminals are connected to the bus and assign new addresses to terminals that have an invalid or duplicate address set by the switch bank. The SPSC only reads the state of its ADDR[4:0] and Parity inputs while in reset. The following table provides the ternary to decimal decoding of the address pins and associated odd parity. ODD parity is calculated against the binary equivalent of the decimal value for the device address.

Table 13-2. SMBus Address and Parity Decoding

Decimal Value	Ternary Pins (MSA:LSA)	Parity Switch		Decimal Value	Ternary Pins (MSA:LSA)	Parity Switch
16	LLMHM	LOGIC 0		70	LHMHM	LOGIC 0
17	LLMHH	LOGIC 1		71	LHMHH	LOGIC 1
18	LLHLL	LOGIC 1		76	LHHMM	LOGIC 0
19	LLHLM	LOGIC 0		77	LHHMH	LOGIC 1
20	LLHLH	LOGIC 1		78	LHHHL	LOGIC 1
21	LLHML	LOGIC 0		79	LHHHM	LOGIC 0
22	LLHMM	LOGIC 0		8 0	LHHHH	LOGIC 1
23	LLHMH	LOGIC 1		81	HLLLL	LOGIC 0
24	LLHHL	LOGIC 1		82	HLLLM	LOGIC 0
25	LLHHM	LOGIC 0		83	HLLLH	LOGIC 1
26	LLHHH	LOGIC 0		84	HLLML	LOGIC 0
27	LMLLL	LOGIC 1		85	HLLMM	LOGIC 1
28	LMLLM	LOGIC 0		86	HLLMH	LOGIC 1
29	LMLLH	LOGIC 1		87	HLLHL	LOGIC 0
30	LMLML	LOGIC 1		88	HLLHM	LOGIC 0
31	LMLMM	LOGIC 0		89	HLLHH	LOGIC 1
32	LMLMH	LOGIC 0		90	HLMLL	LOGIC 1
33	LMLHL	LOGIC 1		91	HLMLM	LOGIC 0
34	LMLHM	LOGIC 1		92	HLMLH	LOGIC 1
35	LMLHH	LOGIC 0		93	HLMML	LOGIC 0
36	LMMLL	LOGIC 1		94	HLMMM	LOGIC 0
37	LMMLM	LOGIC 0		95	HLMMH	LOGIC 1
38	LMMLH	LOGIC 0		96	HLMHL	LOGIC 1
39	LMMML	LOGIC 1		98	HLMHH	LOGIC 0
41	LMMMH	LOGIC 0		99	HLHLL	LOGIC 1
42	LMMHL	LOGIC 0		100	HLHLM	LOGIC 0
43	LMMHM	LOGIC 1		101	HLHLH	LOGIC 1
46	LMHLM	LOGIC 1		102	HLHML	LOGIC 1
47	LMHLH	LOGIC 0		103	HLHMM	LOGIC 0
48	LMHML	LOGIC 1		104	HLHMH	LOGIC 0
49	LMHMM	LOGIC 0		105	HLHHL	LOGIC 1
50	LMHMH	LOGIC 0		106	HLHHM	LOGIC 1
51	LMHHL	LOGIC 1		107	HLHHH	LOGIC 0
52	LMHHM	LOGIC 0		108	HMLLL	LOGIC 1
53	LMHHH	LOGIC 1		109	HMLLM	LOGIC 0
54	LHLLL	LOGIC 1		110	HMLLH	LOGIC 0
56	LHLLH	LOGIC 0		111	HMLML	LOGIC 1
57	LHLML	LOGIC 1		112	HMLMM	LOGIC 0
58	LHLMM	LOGIC 1		113	HMLMH	LOGIC 1
59	LHLMH	LOGIC 0		114	HMLHL	LOGIC 1
60	LHLHL	LOGIC 1		115	HMLHM	LOGIC 0
61	LHLHM	LOGIC 0		116	HMLHH	LOGIC 1
62	LHLHH	LOGIC 0		117	HMMLL	LOGIC 0
63	LHMLL	LOGIC 1		118	HMMLM	LOGIC 0
69	LHMHL	LOGIC 0		119	HMMLH	LOGIC 1

14 Application Configurations

Figure 14-1 presents the essential configuration of the SPSC proving Load-Switch control with inrush current limiting and eFuse protection for current and voltage faults. In this application scenario a single discrete command is provided by power system manager to enable/disable device operation. Two digital flags are also provided to the system manager to indicate when a current limit fault has occurred and when the monitored power rails are all good.

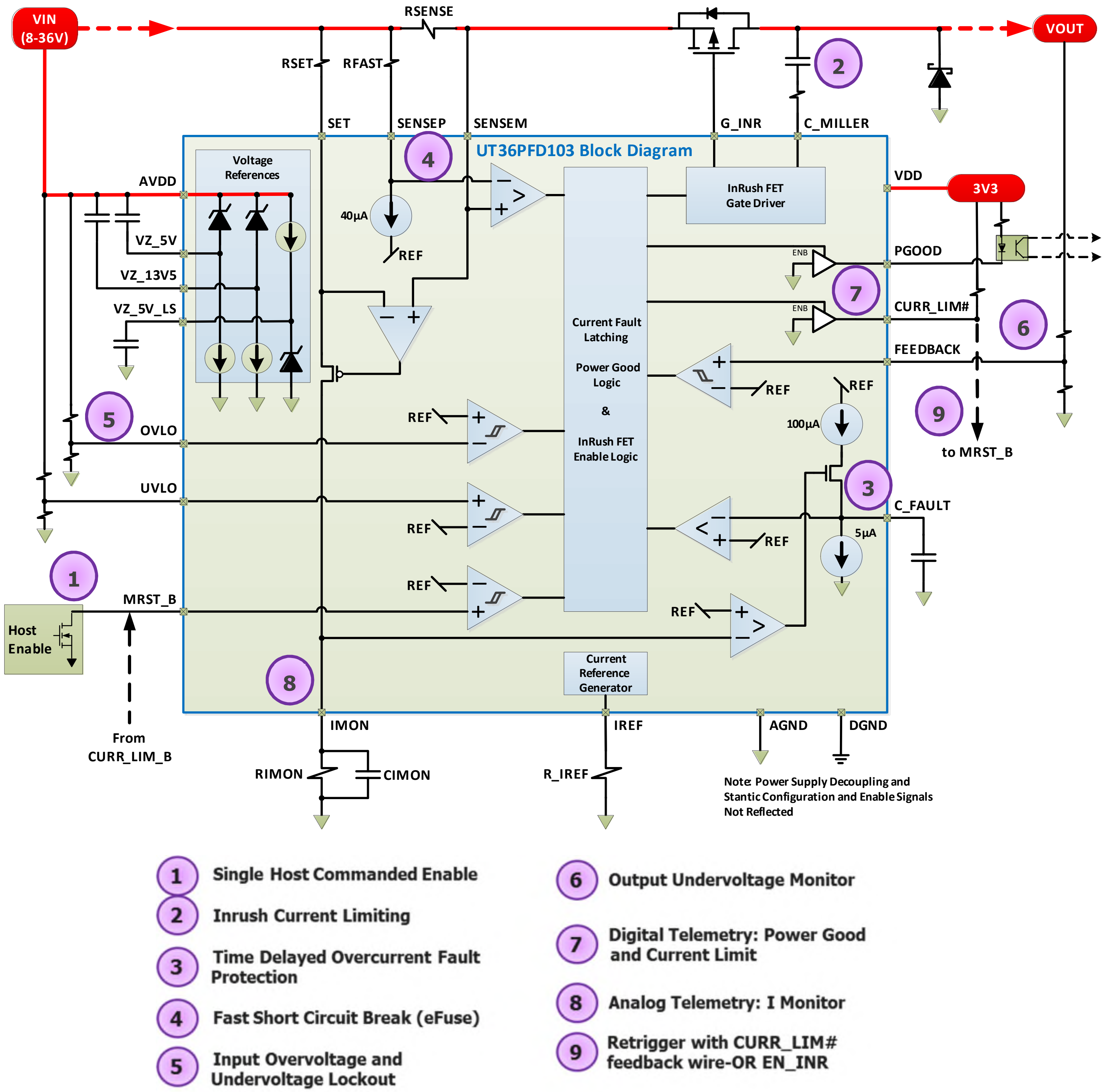


Figure 14-1. Essential Hot Swap Controller Configuration with eFuse Fault Protection

UT05PFD103

Although power system manager command and control of the SPSC is not depicted, Figure 14-2 demonstrates the efficient routing of essential analog and switch control signals when providing inrush current limited, hot swap control with eFuse protection and an added ORing FET acting as an Ideal Diode. For this application, the EN_B, EN_INR and EN_OR pins could be strapped to automatically enable power switching control or alternatively they could be driven by the power system manager.

If digitized telemetry and more detailed status information is required, employ PMBus functionality by interfacing system manager containing an I2C serial port to the SPSC SMBus port. The available digitized telemetry includes 10-bit, single ended representation of the IMON pin, and a scaled representation of the voltage on VIN and VOUT.

To disable the PMBus feature on the SPSC, simply ground the PMB_EN input. All other PMBus related signals may be left floating.

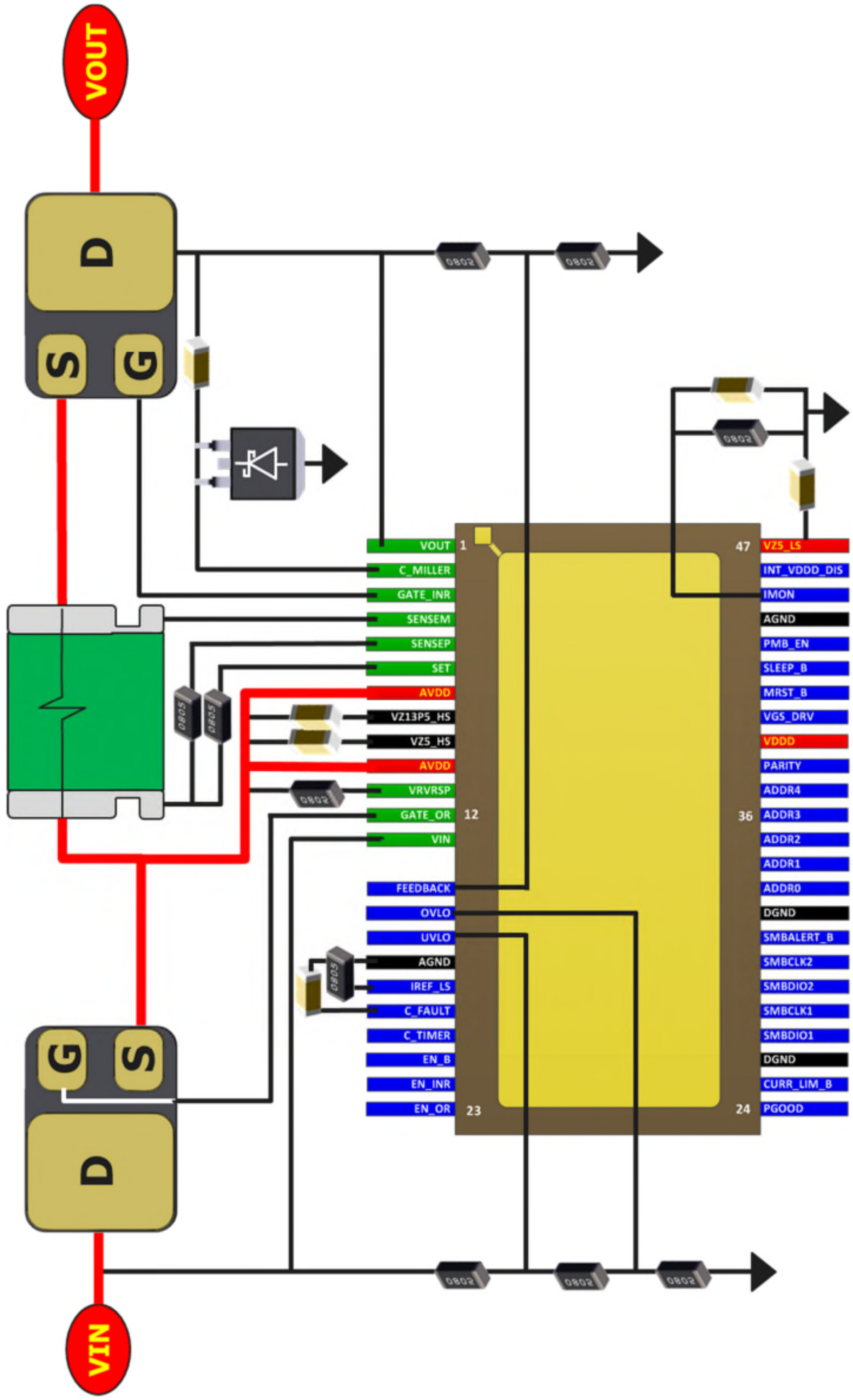


Figure 14-2. Essential SPSC Load-Switch control with eFuse protection and Ideal Diode

15 Packaging Drawings

(Package Mass = 2.3gm)

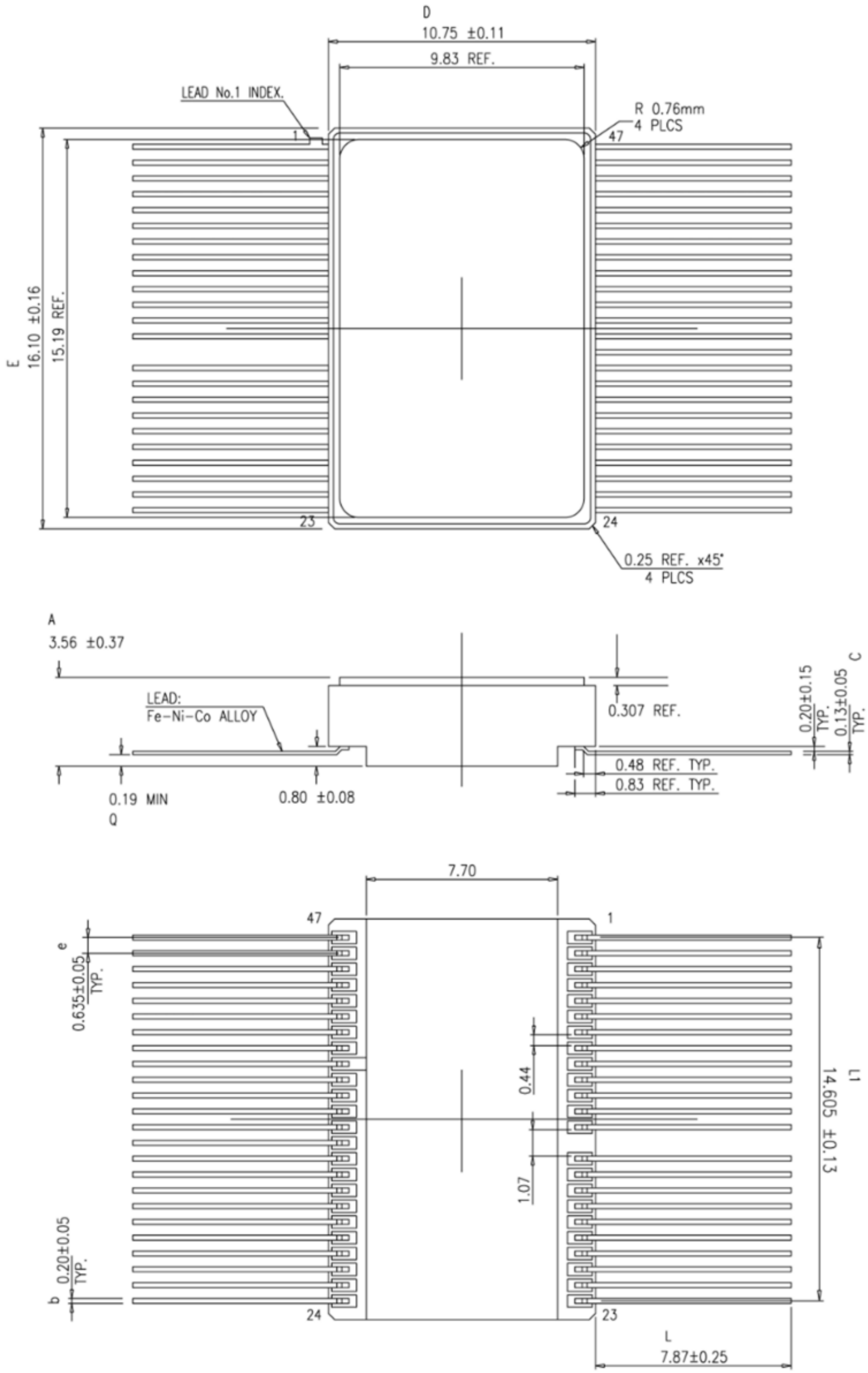


Figure 15-1: 47-Lead Flatpack Outline Drawing

16 Ordering information

16.1 CAES Part Number

Generic Datasheet Part Numbering

UTxxxxx * * * *

Lead Finish: (Notes: 1, 2)
(blank) = Leave this field blank if ordering bare die
(A) = Hot Solder Dipped or Tinned
(C) = Gold
(X) = Factory Option (Gold, Solder, or Tinned)

Screening Level: (Notes: 3, 4, 5)
(blank) = Leave this field blank if ordering bare die
(P) = Prototype Flow (Temperature Range: 25°C only)
(C) = HiRel Flow (Temperature Range: -55°C to +125°C)
(L) = Constellation Flow (Contact Factory for Availability)

Case Outline:
(DIE) = Bare die (Contact Factory for Availability)
(X) = 47-Ceramic Flat Package

Radiation Designator: (Note 5)
(-) = No RHA Assurance
(R) = 100k rad(Si) – (effective dose rate 1 rad(Si)/sec) – Constellation Only
(F) = 300k rad(Si) – (effective dose rate 1 rad(Si)/sec) – Constellation Only

Device Type:
(05PFD103) = 5V Smart Power Switch Controller

NOTES:
1. Lead finish (A, C, or X) must be specified.
2. If and "X" is specified when ordering, then the part marking will match the lead finish applied to the device shipped
3. Prototype Flow per CAES Manufacturing Flows Document. Lead finish is Factory Option "X" - only. Radiation is neither tested nor guaranteed.
4. HiRel Flow per CAES Manufacturing Flows Document.
5. Constellation Flow per CAES Manufacturing Flows Document. Radiation TID tolerance may (or may not) be ordered.

16.2 SMD Part Number

5962 * ***** ** * * *

Lead Finish: (Notes: 1, 2)
(A) = Hot Solder Dipped or Tinned (for packaged device)
(C) = Gold
(X) = Factory Option (Gold, Solder, or Tinned)
(A) = Die detail reference

Case Outline:
(X) = 47-Lead Ceramic Flat Package
(9) = Bare Die (Contact factory for availability)

QML/JAN Class:
(Q) = Class Q
(V) = Class V

Device Type:
(01)

SMD Project Number:
(20215) = 5V Smart Power Switch Controller

Radiation Hardness Assurance:
(R) = 100 krad(Si) – (effective dose rate 1 rad(Si)/sec)
(F) = 300 krad(Si) – (effective dose rate 1 rad(Si)/sec)

Federal Stock Class Designator

NOTES:

1. Lead finish must be specified. If "X" is specified when ordering, the factory will determine lead finish. Part marking will reflect the lead finish applied to the device shipped.
2. If ordering bare die, the lead finish refers to the associated die detail drawing in the SMD. The sequence follows the English alphabet, beginning with "A".

17 Revision History

Date	Version	Editor	Datasheet Level	Change Description
1/30/2020	1.0	TLM	Advanced	Initial Customer Release
2/26/2020	1.1	TLM	Advanced	Corrected package pinout changing pin 40 from VDD to DGND. DC Electrical Tables 10-X updated to more accurately address test conditions, adjust target limits as appropriate, removed non-essential parameters and updated parameter notes to better reflect those that shall not be expected to receive full measurement level testing during production. Timing Characteristics Tables 11-X updated to more accurately reflect test conditions, remove non-essential or non-applicable parameters and updated notes to better reflect those that shall not be expected to receive full measurement level testing during production. Timing parameters associated with the FET Gate Driver outputs (G_OR and G_INR) will not include the contribution of MILLER CAPACITANCE or GATE-CHARGE during production testing. As such their transitional threshold for timing purposes will be to the 50% switching point. Timing diagrams have been updated to reflect this change, even when the show Miller Plateaus, which are provided for application visualization only.
4/30/2021	1.2	TLM	Advanced	Converted document to new CAES template. Added package mass. Clarified PMB_EN pin description. Expanded section 6.1 to provide more accurate VOUT slew rate calculations. Corrected/clarified conditions in Table 10-1. Corrected limits and added 2 new parameters in Table 10-5. Corrected and added previously undefined limits in Table 10-6. Corrected limit in Table 11-6. Added clarifying wording regarding SMBus address parity in section 13.1.2 and corrected SMBus address MSA:LSA ordering Table 13-2. Updated part ordering descriptions.
8/12/2021	1.3	TLM	Advanced	Added SpaceVPX/SpaceUM VS3 switching in application section of first page. Removed Cold-Sparing as an I/O feature throughout document. Added strong recommendation for series resistor with CMILLER pin for current protection during fast eFuse events in section 6.1. Added Single Event Burnout as parameter in Table 8-1 and updated notes. Added note to Table 9-1 Recommended Operating Conditions to indicate 5.5V continuous operation is after derating from the technology capability. Corrected/updated limits in Tables 10-2 and 10-4. Corrected conditions, limits, and added note to several parameters in Table 11-7. Added clarifying note to PMBus commands 88h, 8Bh, and 8Ch described in section 13.1.1
April 2022	2.0	TLM	Final	Updated many parameter limits in Tables 10-x and 11-x based on full device characterization.

UT05PFD103

Datasheet Definitions

	Definition
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet ***is subject to change***. Specifications can be ***TBD*** and the part package and pinout are ***not final***.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in Production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

ECCN Classification 9A515.e.1

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