DATASHEET

REV G: 02/18/21

SCD3370

ACT-D16M96S High Speed 16 x 96 Megabit 3.3V Synchronous DRAM Multichip Module

ACT-D16M96S

FEATURES

- ❑ Six (6) low power 4M x 16 x 4 banks Synchronous Dynamic Random Access Memory chips in one MCM.
- ❑ Configured as "2" independent 4M x 48 x 4 banks.
- ❑ High-Speed, low-noise, low-voltage TTL (LVTTL) interface.
- ❑ 3.3V Power supply (±5% tolerance).
- ❑ Separate logic and output driver power pins.
- ❑ Up to 50MHz data rates.
- ❑ Internal pipelined operation; column address can be changed every clock cycle.
- ❑ Programmable burst lengths: 1, 2, 4, 8, or full page.
- ❑ Auto precharge, includes concurrent auto precharge, and auto refresh modes.
- ❑ Self refresh mode.
- ❑ 64ms, 8,192-cycle refresh.
- ❑ CAS latency (CL) programmable to 2 cycles from column address entry.
- ❑ Cycle-by-Cycle DQ-bus write mask capability with upper and lower byte control.
- ❑ Chip select and clock enable for enhanced-system interfacing.
- ❑ Designed for commercial, industrial, and aerospace applications.
- ❑ MIL-PRF-38534 compliant devices available.
- ❑ CAES is a Class H & K MIL-PRF-38534 manufacturer.
- ❑ 200-Lead, hermetic, CQFP, cavity-up package.

INTRODUCTION

The ACT-D16M96S device is a high-speed synchronous dynamic random access memory (SDRAM) organized as 2 independent 4M x 48 x 4 banks. All inputs and outputs of the ACT-D16M96S are compatible with the LVTTL interface. All inputs and outputs are synchronized with the CLK input to simplify system design and enhance use with high-speed microprocessors and caches.

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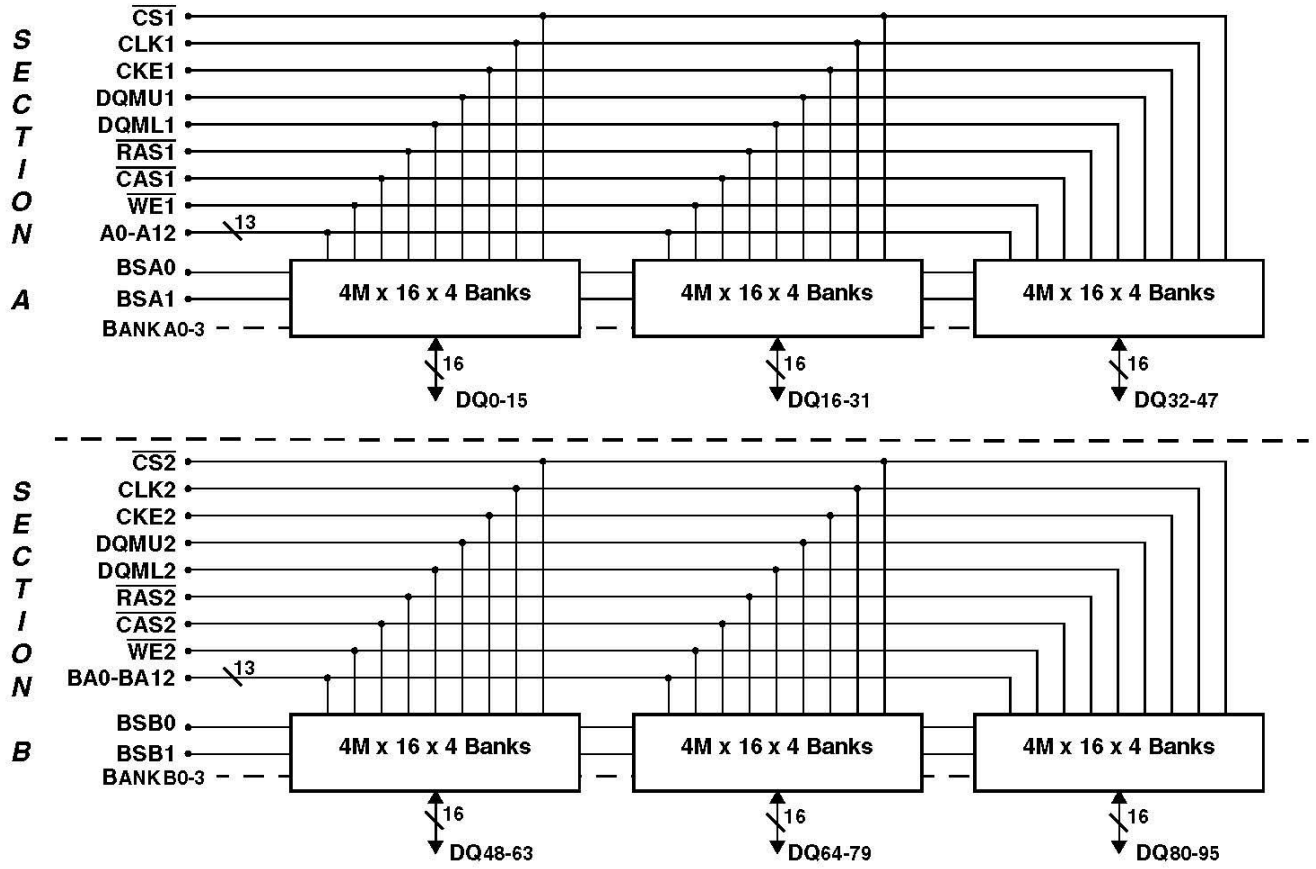
DETAILED BLOCK DIAGRAM



ACT-D16M96S

FUNCTIONAL DESCRIPTION

There are six (6) 256Mb SDRAMs (4 Meg x 16 x 4 banks) chips that operate at 3.3V and include a synchronous interface (all signals registered on the positive edge of the clock signal, CLK). Each of the 67,108,864-bit banks is organized as 8,192 rows by 512 columns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BSA0, BSA1, BSB0, BSB1 select the bank, A0-A12; BA0-BA12 select the row).The address bits (x16: A0-8; BA0-BA8) registered coincident with READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

For additional Detail Information regarding the operation of the individual chip (MT48LC16M16A2 – 4 meg x 16 x 4 banks) see Micron 524,288-WORD BY 16-BIT BY 4- BANK SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY Data sheet Revision M dated1/09 or contact the CAES Sales Department.

ABSOLUTE MAXIMUM RATINGS[1]

Table 1: Absolute Maximum Ratings

SYMBOL	RATING	RANGE	UNITS
V_{CC}	Supply Voltage	-0.5 to 4.6	V
V_{CCQ}	Supply Voltage range for output drivers	-0.5 to 4.6	V
V_{RANGE}	Voltage range on any pin with respect to V_{ss}	-0.5 to 4.6	V
T_{BIAS}	Junction Temperature under Bias [2]	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
PW	Power Distribution	4.2	W

NOTES:
1. Stresses above those listed under "Absolute Maximums Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Tested with Case set to specified temperature. The temperature rise of ΘJC is negligible due to the low duty cycle during testing.

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RECOMMENDED OPERATING CONDITIONS

Table 2: Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage	3.15	3.3	3.45	V
V_{CCQ}	Supply Voltage range for output drivers	3.15	3.3	3.45	V
V_{SS}	Supply Voltage	-	0	-	V
V_{SSQ}	Supply Voltage range for output drivers	-	0	-	V
V_{IH}	Input High Voltage	2	-	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage [1]	-0.3	-	0.8	V
T_C	Operating Temperature (Junction) [2]	-55	-	+107	°C

NOTES:
1. VIL Minimum = 1.5 Vac (Pulsewidth ≤ 5ns)
2. Tested with Case set to specified temperature. The temperature rise of 0jc is negligible due to the low duty cycle during testing and it is recommended that the maximum junction temperature should be kept less than +110°C.

THERMAL IMPEDANCE

Table 3: Thermal Impedance

PARAMETER	Θ_{JC}	UNITS
Junction to Case	1.53	°C/W

NOTE: Model based on Micron die database Y16Y and die size – 5,250.010µm x 8,879.002µm (206.693 mil x 349.567 mil) using CAES ceramic co-fired package 25G5060 Rev B.

DC CHARACTERISTICS

Table 4: DC Characteristics
(V_{CC} = 3.3V ±0.15; T_J = -55°C to +107°C, See Notes 1 & 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output Low Voltage	V_{OL}	I_{OL} = 2mA	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -2mA	2.4	-	V
Input current (Leakage)	I_I	0V ≤ V_I ≤ V_{CC} + 0.3V, All other pins = 0V to V_{CC}	-10	+10	µA
Output current (Leakage)	I_O	0V ≤ V_O ≤ V_{CC} + 0.3V, Output disabled	-10	+10	µA
Precharge standby current in non-power-down mode	I_{CC2N}	CKE ≥ V_{IH} MIN, tck = 20ns (See Note 2)	-	180	mA
	I_{CC2NS}	CKE ≥ V_{IH} MIN, CLK < V_{IL} MAX, tck = ∞, (See Note 3)	-	120	mA

NOTES:
1. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.
2. Control, DQ, and address inputs change state only once every 40ns.
3. Control, DQ, and address inputs do not change (stable).
4. All ICC parameters measured with VCC, not VCCQ.
5. Tested with Case set to specified temperature. The temperature rise of ΘJC is negligible due to the low duty cycle during testing.

CAPACITANCE*

Table 5: Capacitance
(f = 1MHz, Tc = 25°C

SYMBOL	PARAMETER	MIN	MAX	UNITS
Ci(S)	Input Capacitance, CLK Input	-	50	pF
Ci(AC)	Input Capacitance, Address and Control Inputs: A0-A11, CS, DQMx, RAS, CAS, WE	-	40	pF
Ci(E)	Input Capacitance, CKE Input	-	50	pF
C_O	Output Capacitance	-	20	pF

* - Parameters Guaranteed but not tested.

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AC TIMING*

** Table 6: AC Timing * & **
(VCC = 3.3V ± 0.15V, TJ = -55°C to 107°C, See Note 4)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Cycle time, CLK	tCK2	CAS latency = 2	20	-	ns
Pulse duration, CLK high	tCH	-	5	-	ns
Pulse duration, CLK low	tCL	-	5	-	ns
Access time, CLK high to data out (See Note 1)	tAC2	CAS latency = 2	-	13	ns
Hold time, CLK high to data out	tOH	-	1	-	ns
Setup time, address input	tIS[addr]	-	3	-	ns
Setup time, banksel input	tIS[banksel]	-	3	-	ns
Setup time, data input	tIS[data]	-	2.5	-	ns
Setup time, control input	tIS[cntrl]	-	2.5	-	ns
Hold time, address, control, and data input	tIH	-	2.5	-	ns
Delay time, ACTV command to DEAC or DCAB command	tRAS	-	72	100000	ns
Delay time, ACTV or REFR to ACTV, MRS or REFR command	tRC	-	100	-	ns
Delay time, ACTV command to READ, READ-P, WRT, or WRT-P command (See Note 2)	tRCD	2 * 12.5ns Cycles	25	-	ns
Delay time, DEAC or DCAB command to ACTV, MRS or REFR command	tRP	2 * 12.5ns Cycles	25	-	ns
Delay time, ACTV command in one bank to ACTV command in the other bank	tRRD	-	18	-	ns
Delay time, MRS command to ACTV, MRS or REFR command	tRSA	-	30	-	ns
Final data out of READ-P operation to ACTV, MRS or REFR command	tAPR	-	tRP-(CL-1)*tCK (See Note 3)	-	ns
Final data in of WRT-P operation to ACTV, MRS or REFR command	tAPW	-	60	-	ns
Delay time, final data in of WRT operation to DEAC or DCAB command	tWR	Ck = 12.5ns	1ck+7ns	-	ns
Refresh interval	tREF	-	-	50	ms
Delay time, CS low or high to input enabled or inhibited	nCDD	-	0	0	Cycle
Delay time, CKE high or low to CLK enabled or disabled	nCLE	-	1	1	Cycle
Delay time, final data in of WRT operation to READ, READ-P, WRT, or WRT-P	nCWL	-	1	-	Cycle
Delay time, ENBL or MASK command to enabled or masked data in	nDID	-	0	0	Cycle
Delay time, ENBL or MASK command to enabled or masked data out	nDOD	-	2	2	Cycle
Delay time, DEAC or DCAB, command to DQ in high-impedance state	nHZP2	CAS latency = 2	-	2	Cycle
Delay time, WRT command to first data in	nWCD	-	0	0	Cycle
Delay time, STOP command to READ or WRT command	nBSD	-	-	2	Cycle

* - See Figure 2 – LVTTL Load Circuit for load circuits.
** - All references are made to the rising transition of CLK, unless otherwise noted.
NOTES:

1. tAC is referenced from the rising transition of CLK that is previous to the data-out cycle. For example, the first data out tAC is referenced from the rising transition of CLK within the following cycle: CAS latency minus one cycle after the READ command. An access time is measured at output reference level 1.5 V.
2. For read or write operations with automatic deactivate, tRCD must be set to satisfy minimum tRAS.
3. CL = CAS Latency
4. Tested with Case set to specified temperature. The temperature rise of ΘJC is negligible due to the low duty cycle during testing.

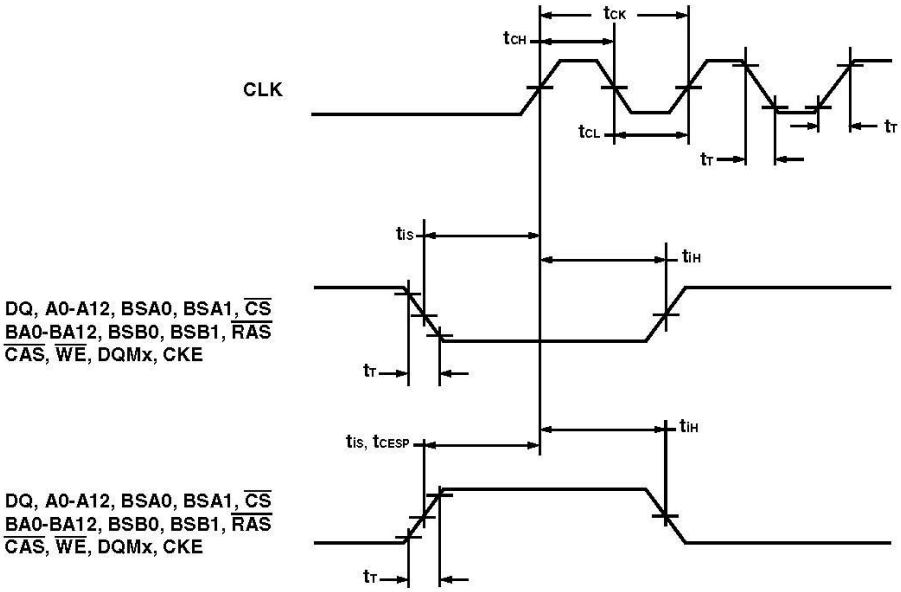

Figure 2: Input Attribute Parameters

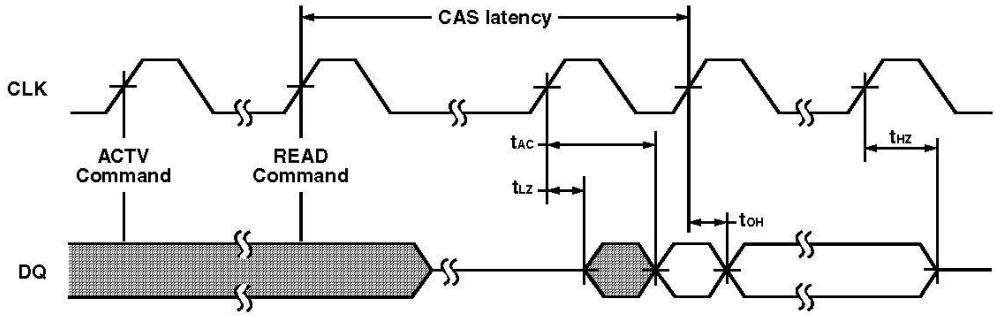

Figure 3: Output Parameters

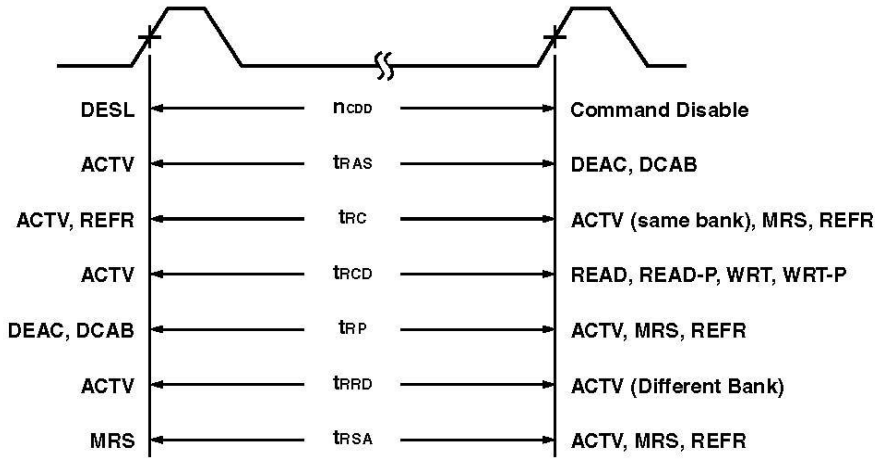

Figure 4: Command-to-Command Parameters

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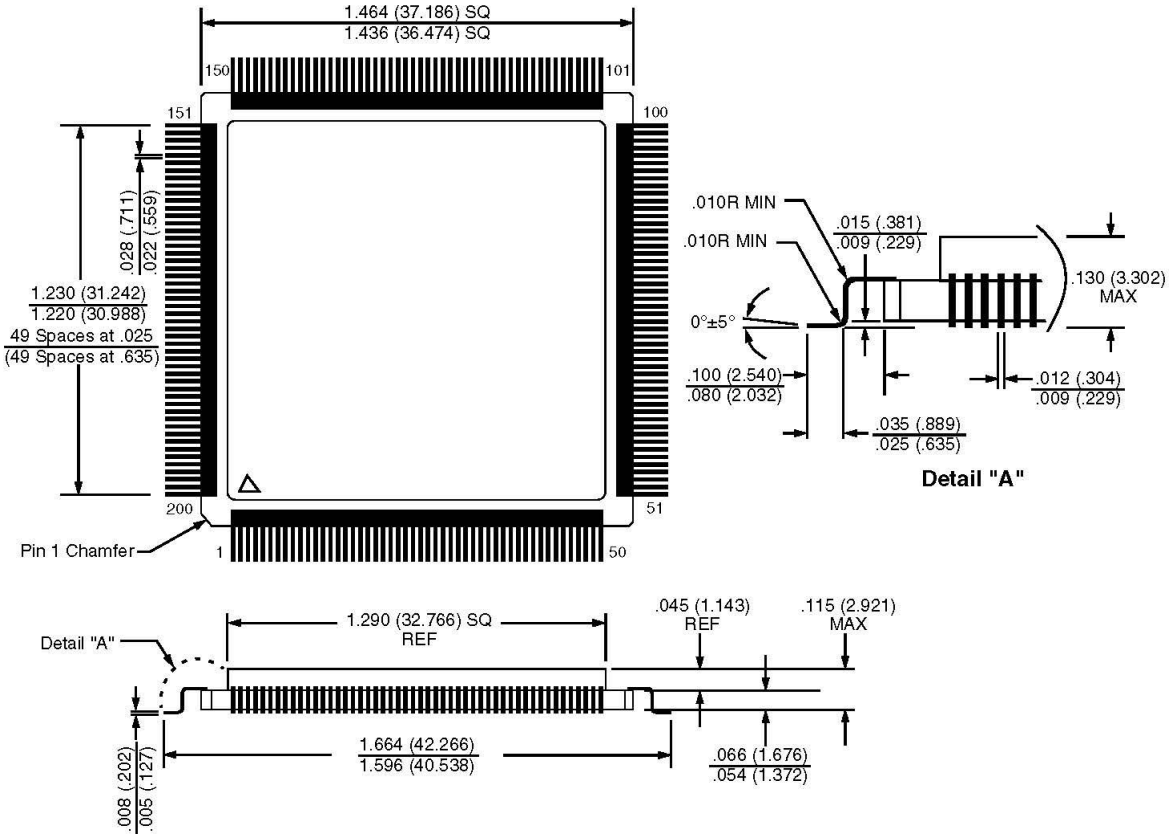
PACKAGE INFORMATION – "F20" – CQFP 200 LEADS



NOTE: 1. All Dimensions in inches (Millimeters) MAX/MIN or Typical where noted.

Table 7: Pin Nomenclature

A0-A12 BA0-BA12	Address Inputs A0-A12, BA0-BA12 Row Addresses A0-A8, BA0-BA8 Column Addresses A10, BA10 Automatic-Precharge Select
BSA0, BSB0 BSA1, BSB1	Bank Select
CAS1, CAS2	Column-Address Strobe
CKE1, CKE2	Clock Enable
CLK1, CLK2	System Clock
CS1, CS2	Chip Select
DQ0-DQ95	SDRAM Data Input/Output
DQML1, 2 DQMU1, 2	Data/Input Mask Enables
RAS1, RAS2	Row-Address Strobe
VCC	Power Supply
VCCQ	Power Supply for Output Drivers
VSS	Ground

VSSQ	Ground for Output Drivers
WE1, WE2	Write Enable

ACT-D16M96S CQFP PINOUTS – "F20"

Table 8: ACT-D16M96S CQFP PINOUTS – "F20"

PIN #	FUNCTION	PIN#	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION
1	DQ2	41	DQ91	81	DQ67	121	VSSQ	161	DQ30
2	DQ3	42	BA11	82	DQ66	122	BA1	162	VSSQ
3	VSSQ	43	DQ92	83	VSS	123	BA2	163	DQ29
4	DQ4	44	DQ93	84	DQ65	124	VCCQ	164	DQ28
5	DQ5	45	VCCQ	85	DQ64	125	BA3	165	VCC
6	VCCQ	46	DQ94	86	VCC	126	A4	166	DQ27
7	DQ6	47	DQ95	87	DQ63	127	VCCQ	167	DQ26
8	DQ7	48	VSSQ	88	DQ62	128	A5	168	VSS
9	A11	49	DQ87	89	VSSQ	129	A6	169	DQ25
10	DQML1	50	DQ86	90	DQ61	130	VSSQ	170	DQ24
11	WE1	51	DQ85	91	DQ60	131	A7	171	VSSQ
12	VSSQ	52	DQ84	92	VSSQ	132	A8	172	CLK1
13	CAS1	53	VSSQ	93	DQ59	133	VSS	173	CKE1
14	RAS1	54	DQ83	94	DQ58	134	A9	174	VCCQ
15	VCC	55	DQ82	95	VCCQ	135	DQMU1	175	DQ23
16	CS1	56	VCCQ	96	DQ57	136	VCC	176	DQ22
17	BSA0	57	DQ81	97	DQ56	137	DQ40	177	VCCQ
18	VSS	58	DQ80	98	VSSQ	138	DQ41	178	DQ21
19	A10	59	BSA1	99	DQ48	139	VSSQ	179	DQ20
20	A0	60	DQ79	100	DQ49	140	DQ42	180	VSSQ
21	VSSQ	61	DQ78	101	DQ50	141	DQ43	181	DQ19
22	A1	62	VSSQ	102	DQ51	142	BA12	182	DQ18
23	A2	63	DQ77	103	VSSQ	143	DQ44	183	VSS
24	VCCQ	64	DQ76	104	DQ52	144	DQ45	184	DQ17
25	A3	65	VCC	105	DQ53	145	VCCQ	185	DQ16
26	BA4	66	DQ75	106	VCCQ	146	DQ46	186	VCC
27	VCCQ	67	DQ74	107	DQ54	147	DQ47	187	DQ15
28	BA5	68	VSS	108	DQ55	148	VSSQ	188	DQ14
29	BA6	69	DQ73	109	VSSQ	149	DQ39	189	VSSQ
30	VSSQ	70	DQ72	110	DQML2	150	DQ38	190	DQ13
31	BA7	71	VSSQ	111	WE2	151	DQ37	191	DQ12
32	BA8	72	CLK2	112	VSSQ	152	DQ36	192	BSB1
33	VSS	73	CKE2	113	CAS2	153	VSSQ	193	DQ11
34	BA9	74	VCCQ	114	RAS2	154	DQ35	194	DQ10
35	DQMU2	75	DQ71	115	VCC	155	DQ34	195	VCCQ
36	VCC	76	DQ70	116	CS2	156	VCCQ	196	DQ9
37	DQ88	77	VCCQ	117	BSB0	157	DQ33	197	DQ8
38	DQ89	78	DQ69	118	VSS	158	DQ32	198	VSSQ
39	VSSQ	79	DQ68	119	BA10	159	A12	199	DQ0
40	DQ90	80	VSSQ	120	BA0	160	DQ31	200	DQ1

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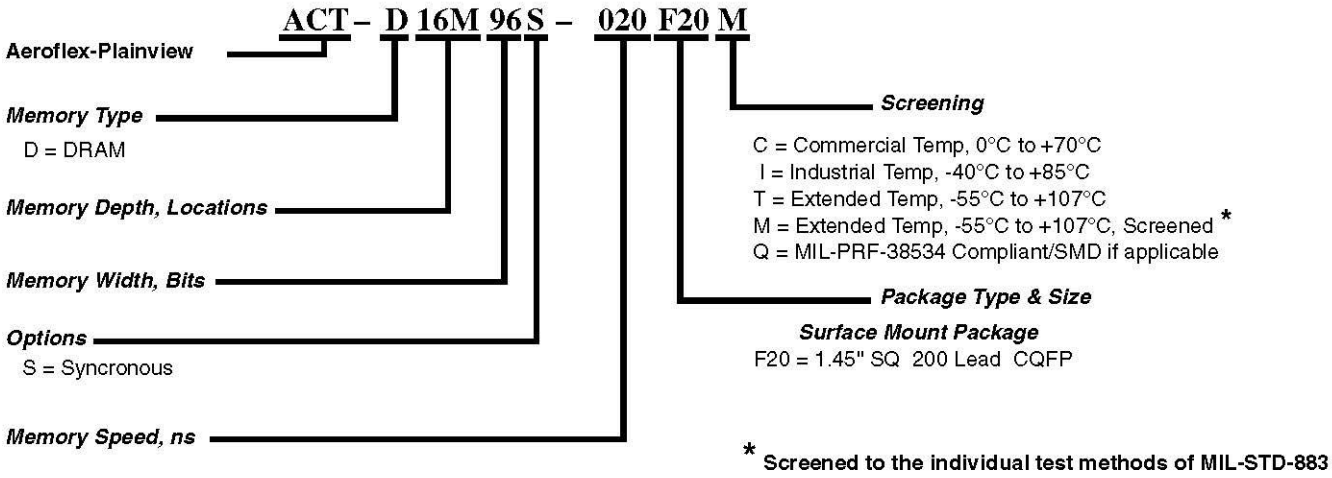
ORDERING INFORMATION

PART NUMBER	SCREENING	SPEED	PACKAGE
ACT-D16M96S-020F20C	Commercial Temperature	20 ns	200 Lead CQFP
ACT-D16M96S-020F20T	Extended Temperature	20 ns	200 Lead CQFP
ACT-D16M96S-020F20M	Extended Temperature Screening	20 ns	200 Lead CQFP

PART NUMBER BREAKDOWN



* Screened to the individual test methods of MIL-STD-883

REVISION HISTORY

Date	Rev. #	Change Description	Initials
09/17/2018	F	REVISED PER ECN 7965-60	CL
02/18/2021	G	REVISED PER ECN 23515	CL

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Datasheet Definitions

	DEFINITION
Advanced Datasheet	Product In Development
Preliminary Datasheet	Shipping Prototype
Datasheet	Shipping QML & Reduced Hi - Rel