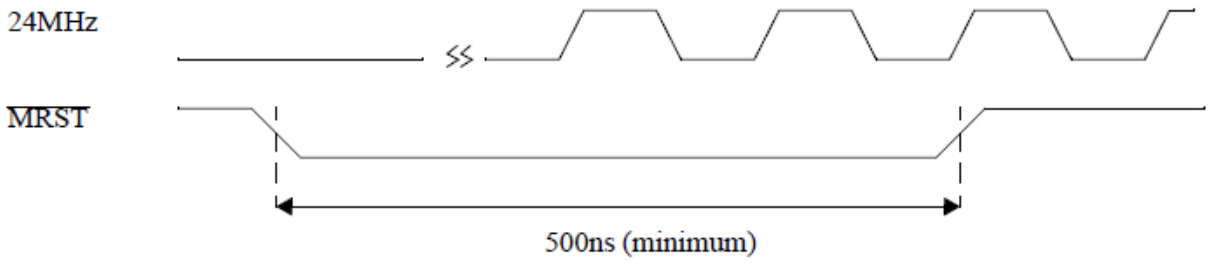
UT69151 SµMMIT Family (All Revisions): Reset

To properly prepare the SµMMIT family (i.e., SµMMIT, SµMMITLX/DX, or SµMMIT XT) of devices for operation, assert both master reset (*MRST*) and the JTAG reset *(TRST*) before attempting device initialization. If not properly reset, the SµMMIT family of devices can enter an undefined state and not meet the Date Sheet specifications and required MIL-STD-1553 functionality.

Master Reset:

Hold input *MRST* to a logic zero voltage level for at least 500ns while applying a minimum of two 24MHz clocks to input *24MHz*. After two 24MHz clock periods and 500ns have passed, input *MRST* can transition back to a logic one voltage level.



JTAG Reset:

Hold input *TRST* to a logical zero voltage level for at least 500ns while applying a minimum of two 24MHz clocks to input *24MHz*. For system simplicity, tie *TRST* to *MRST*. For systems not using the JTAG port, tie JTAG input *TRST* to a logic zero voltage level.

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