APPLICATION NOTE

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Utilizing the UT54ACS164245S as Cold-Sparing Buffer

Abstract

UTMC has developed the UT54ACS164245S 16-bit Multipurpose Transceiver to be used as a cold-sparing buffer in applications where redundant subsystems are to remain in a high impedance power-off state. This allows a redundant subsystem to be connected to the host system while being electrically isolated from the functioning host system.

Introduction

Redundancy of mission critical subsystems is a common practice used to ensure reliable operation of a spacecraft or satellite. The inputs and outputs of the UT54ACS164245S, while no power is being supplied to the device, can be tied to an active bus while remaining in a high impedance state. With V_{DD} equal to zero volts, the UT54ACS164245S outputs and inputs present a minimum impedance of 1MΩ making it ideal for cold-sparing applications. Further, the architecture of the UT54ACS164245S provides two separate 8-bit ports with their own control signals and signal lines. Operation can be as two independent 8-bit buffers or by tying the control signal lines together as a single 16-bit buffer. The device is also designed with the capability of translating voltage levels between the system and cold-spared subsystem.

The first section of this application note describes the device and its pin functionality followed by an example of using the device to cold-spare a redundant subsystem. The example describes an application where an array of memory devices, such as a solid state recorder, is configured as a redundant powered-down subsystem utilizing UT54ACS164245S cold-sparing transceivers.

Device Architecture

Figure 1 provides a closer look at the signal lines, power pins, and control signals for UT54ACS164245S operation. The signal ports are four 8-bit ports. Since the device operates bi-directionally, Ports 1 & 2 are described as having both "A" and "B" sides as well. Note V_{DD1} and V_{DD2} are internally connected to supply power to "B" and "A" ports

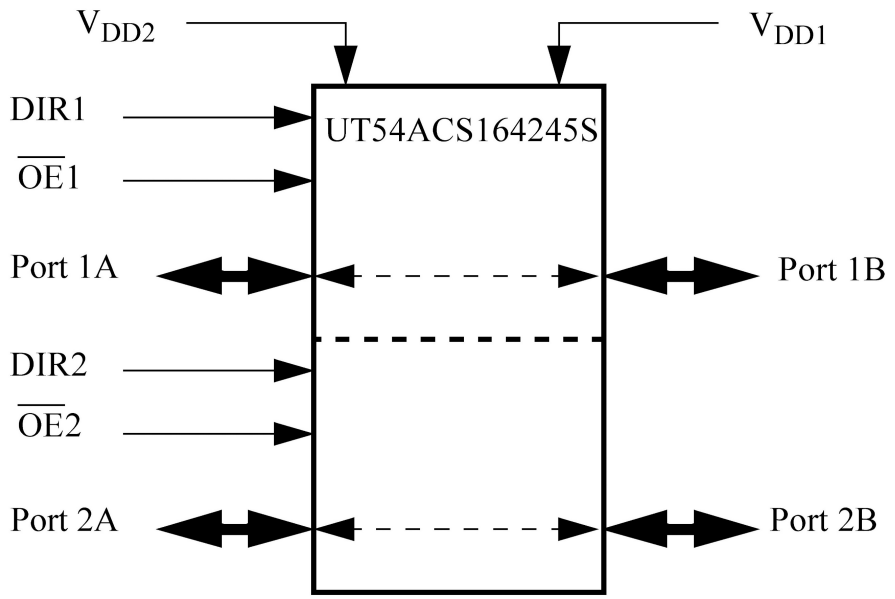

Figure 1. Architectural Block Diagram of the UT54ACS164245S 16-bit (8-bit) Buffer(s)

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of the device, respectively. Although appearing contrary to conceptual logic, this convention has been established by several manufacturers of similar commercial parts. Suffice it to say that if the UT54ACS164245S is used to cold-spare a redundant subsystem where one system is at 3.3 Volts and the other at 5 Volts, then side "A" of the device must interface the 3.3 Volt system. Alternative supply voltage operations will be visited later in this application note.

Directional buffering and device enabling are controlled by the control signals aptly labeled DIRx and $\overline{OE}$x. Output Enable controls, $\overline{OE}$1 and $\overline{OE}$2, are active low signals that cause the UT54ACS164245S to buffer data from one side of the device to the other. When the $\overline{OE}$x signals are 'high" or when the device ports have zero volts on their supply inputs, the device inputs/outputs remain in a high impedance state. This designed behavior is fundamental to the cold-spare functionality provided by the UT54ACS164245S. Direction signals, DIR1 and DIR2, control the flow of "A" data to bus "B" or "B" data to bus "A". Referencing the UT54ACS164245S Data Sheet shows the actual pin numbers for ports 1 and 2 and their connectivity between sides "A" and "B" of the device. Table 1 summarizes the device function effected by the direction and enable signals.

Table 1: Control Signal Function Table

Enable $\overline{OE}$x	Direction DIRx	Operation
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	High Impedance Isolation

When using the UT54ACS164245S to cold-spare a subsystem of a different voltage level than the host system, the designer must maintain the required constraint that $V_{DD1} \geq V_{DD2}$. As mentioned above, with one side of the UT54ACS164245S buffer device interfacing a 5-Volt system and the other connected to a 3.3-Volt system, the "A" ports of the part must interface the 3.3-Volt system. Where the host and subsystem are the same voltage supply level there is no constraint as to which interfaces to the "A" or "B" ports.

Cold-Spared Memory Array

A scenario where the UT54ACS164245S is used to cold-spare a redundant memory card, or solid-state recorder, is treated in this example. For sake of fully utilizing the UT54ACS164245S cold-spare buffer it will be useful to describe a rather full featured memory subsystem. The memory card will contain an arbitrary number of SRAM devices, say 40 Mbits worth of 512K x 8 SRAMs. This requires an array of 10 memory components. Encoding, to enable the particular memories, can be done by a programmable part also resident on the cold-spared, redundant sub-system. Further, let all the components on this subsystem, memories and programmable logic, requires 5-Volt power.

From the above description of the redundant memory sub-system, it is possible to make an assessment of the signals interfacing the cold-spared sub-system to the functioning host system. Considering the 8-bit data bus width of the memory components, the interface will include 8 data lines buffered by the UT54ACS164245S. In addition to the data lines, the address space of the cold-spared system is 5 Megabytes requiring a minimum of 23 address signals to select each byte of the memory array. A usual 512K memory device uses 19 address lines. In the case of this particular example the host system will supply at least 4 more address signals to the cold-spared memory subsystem. The read and write control signals must also be added to this list of cold-spared and electrically isolated signals. The total

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number of signal lines to be isolated from the memory subsystem through UT54ACS164245S devices is 33. This can be accomplished by using three UT54ACS164245S parts.

Of the three UT54ACS164245S devices only the device used to cold-spare the data signals must have directional control. The remaining signals will always be uni-directional from the host system to the memory and programmable logic device on the cold-spared memory card. Additionally, the incoming read or write control line can be used to provide proper direction control for the UT54ACS164245S cold-spared data signals. Assuming that the "A" side of the UT54ACS164245S is chosen to interface with the host system, the direction control of the cold-sparing buffer coincides with the logic of the host read signal, assuming active-low read and write signals. Figure 2 provides a block diagram of the memory card or subsystem. For clarity, the chip select signals from the programmable device and the 19 address connections to each SRAM are left out.

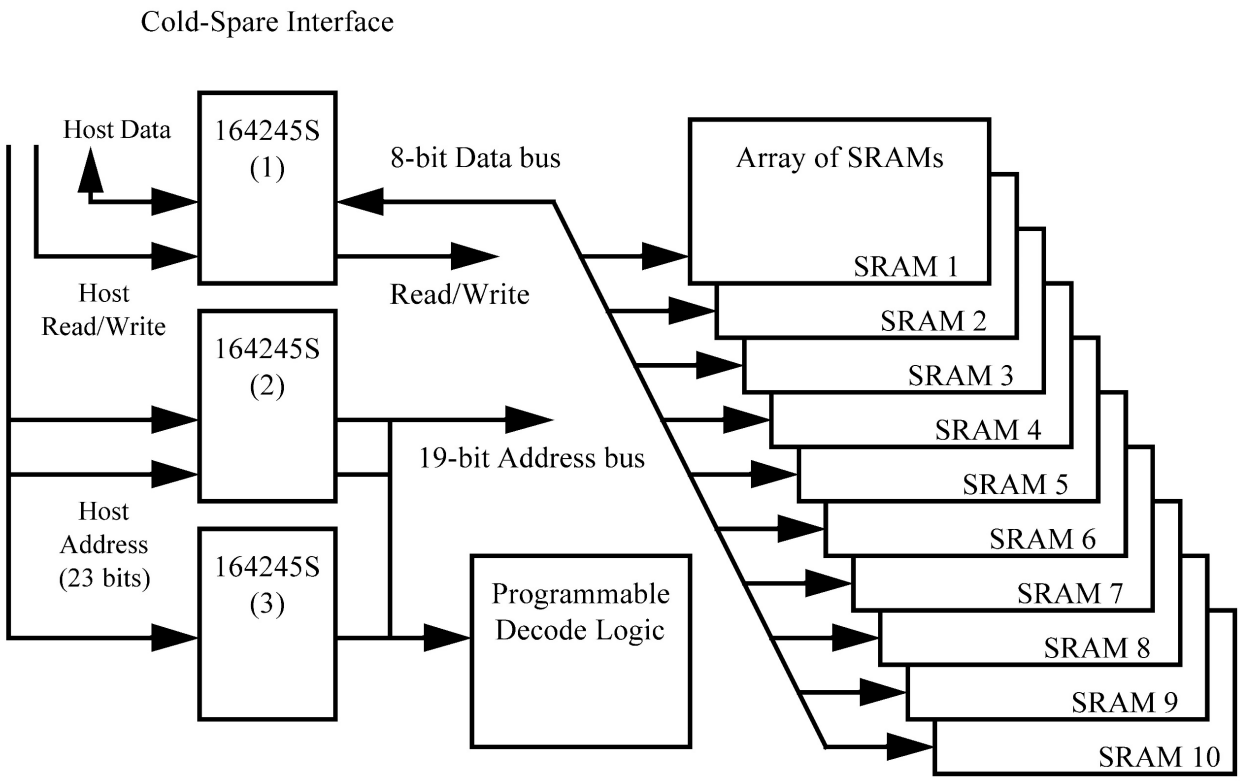

Figure 2. Block Diagram of Cold-Spared Memory Card (Subsystem)

While Figure 2 provides an overview of the cold-spared memory card, Figure 3 illustrates more detail concerning the three UT54ACS164245S devices used in this subsystem. The UT54ACS164245S labeled "1" provides cold sparing to the 8-bit data bus as well as the read and write control lines. The remaining two cold-spare buffers provides isolation to the 23 address lines. Since the address lines and control signals are uni-directional, the direction pins for their respective ports can be tied to the power supply. When the parts are powered up the signals will be buffered from the "A" ports (host bus) to the "B" ports (subsystem). As noted above, the data lines are bidirectional and the signal direction can be controlled by the active low read signal from the host system. In summary, all direction pins of each

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UT54ACS164245S need to be tied high, while the DIR pin of the data signal port will be controlled by the host read signal. All output enable pins will be tied to the ground plane of the subsystem and enables the cold-sparing devices upon subsystem power-up. In this particular design it might be worth noting that the lower order bits of the address signals are cold-spared by the UT54ACS164245S device labeled "2". A better idea would be to pair the least significant byte of the address bus with the most significant seven bits of the address bus to minimize switching interference on the memory subsystem.

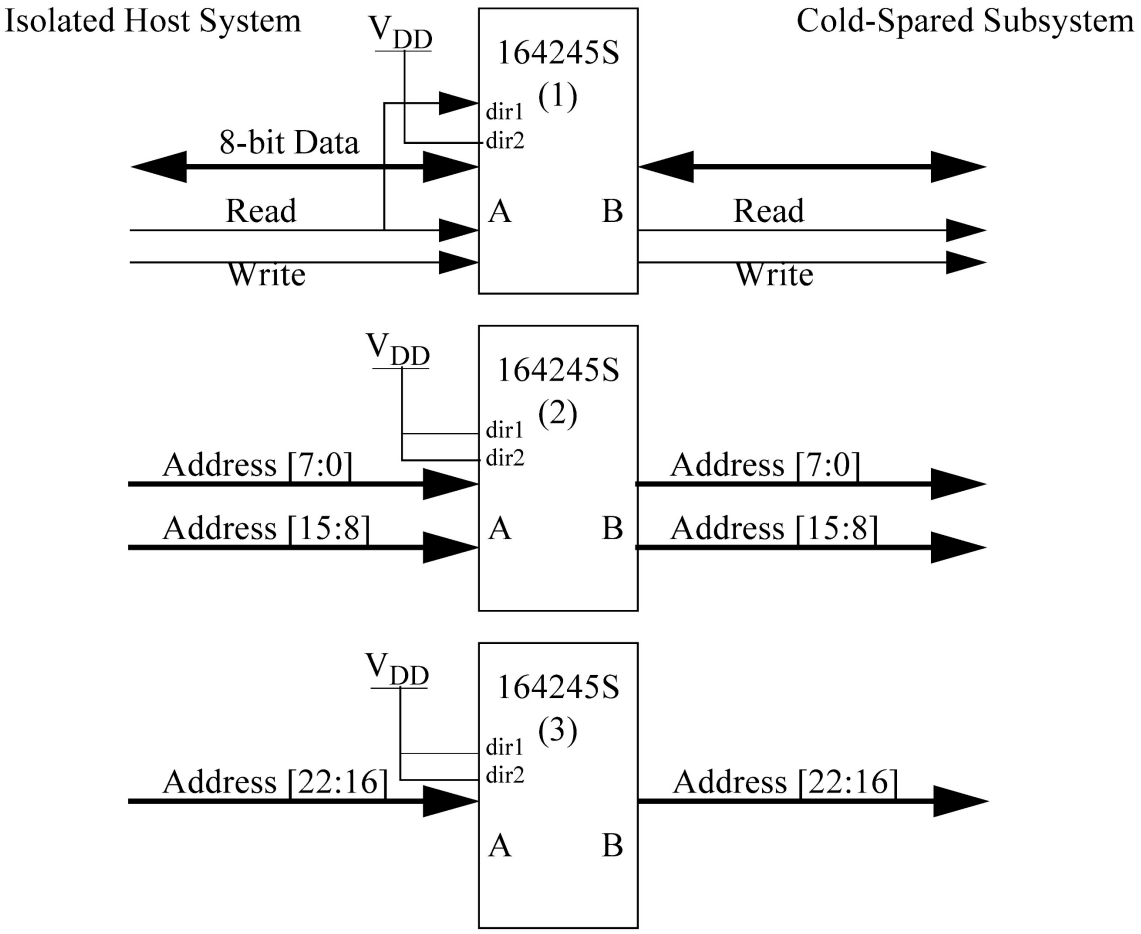

Figure 3. UT54ACS16425S Cold-Sparing Control

Summary

The UT54ACS164245S Cold-Sparing Transceiver was shown to be useful in providing electrical isolation to a redundant powered-down subsystem - a common practice to ensure space system reliability. The high speed, low power UT54ACS164245S transceiver is designed to perform multiple functions including: asynchronous two-way communication, signal buffering, voltage translation, and cold-sparing. With V_{DD} equal to zero volts, the UT54ACS164245S outputs and inputs present a minimum impedance of 1MΩ making it ideal for cold-sparing applications.

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