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8-Bit MSI & 16-Bit Logic Products with Unused or Floating Logic Inputs

Table 1: Cross Reference of Applicable Products, 8-bit MSI Logic

Logic Function Product Description	Manufacturer Part Number	SMD Number	Device Type
Logic quadruple 2-input NAND gates	UT54ACS00	5962-96512	01
	UT54ACS00E*	5962-96512	02, 03
	UT54ACTS00	5962-96513	01
	UT54ACTS00E*	5962-96513	02, 03
Logic quadruple 2-input NOR gates	UT54ACS02	5962-96514	01
	UT54ACS02E*	5962-96514	02, 03
	UT54ACTS02	5962-96515	01
	UT54ACTS02E*	5962-96515	02, 03
Hex inverters	UT54ACS04	5962-96516	01
	UT54ACS04E*	5962-96516	02, 03
	UT54ACTS04	5962-96517	01
	UT54ACTS04E*	5962-96517	02, 03
Logic quadruple 2-input AND gates	UT54ACS08	5962-96518	01
	UT54ACS08E*	5962-96518	02, 03
	UT54ACTS08	5962-96519	01
	UT54ACTS08E*	5962-96519	02, 03
Logic triple 3-input NAND gates	UT54ACS10	5962-96520	01
	UT54ACTS10	5962-96521	01
Logic triple 3-input AND gates	UT54ACS11	5962-96522	01
	UT54ACTS11	5962-96523	01
Hex inverting Schmitt trigger	UT54ACS14	5962-96524	01
	UT54ACS14E*	5962-96524	02, 03
	UT54ACTS14	5962-96525	01
	UT54ACTS14E*	5962-96525	02, 03
Logic dual 4-input NAND gates	UT54ACS20	5962-96526	01
	UT54ACTS20	5962-96527	01
	UT54ACTS20E*	5962-96527	02, 03

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Logic Function Product Description	Manufacturer Part Number	SMD Number	Device Type
Logic triple 3-input NOR gates	UT54ACS27	5962-96528	01
	UT54ACTS27	5962-96529	01
Hex non-inverting buffers	UT54ACS34	5962-96530	01
	UT54ACTS34	5962-96531	01
Logic 4-wide AND-OR-INVERT gates	UT54ACS54	5962-96532	01
	UT54ACTS54	5962-96533	01
FLIP-FLOPs dual D with clear and preset	UT54ACS74	5962-96534	01
	UT54ACS74E*	5962-96534	02, 03
	UT54ACTS74	5962-96535	01
	UT54ACTS74E*	5962-96535	02, 03
Comparators 4-bit	UT54ACS85	5962-96536	01
	UT54ACTS85	5962-96537	01
Logic Quadruple 2-input XOR gates	UT54ACS86	5962-96538	01
	UT54ACS86E*	5962-96538	02, 03
	UT54ACTS86	5962-96539	01
FLIP-FLOPSs dual J-K	UT54ACS109	5962-96540	01
	UT54ACS109E*	5962-96540	02, 03
	UT54ACTS109	5962-96541	01
Logic quadruple 2-Input NAND with Schmitt triggers	UT54ACS132	5962-96542	01
	UT54ACS132E*	5962-96542	02, 03
	UT54ACTS132	5962-96543	01
Decoders/demultiplexers 3-line to 8-line	UT54ACS138	5962-96544	01
	UT54ACS138E*	5962-96544	02, 03
	UT54ACTS138	5962-96545	01
Decoders/demultiplexers dual 2-line to 4-line	UT54ACS139	5962-96546	01
	UT54ACTS139	5962-96547	01
Data selectors/multiplexers 1 to 8	UT54ACS151	5962-96548	01
	UT54ACTS151	5962-96549	01

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Logic Function Product Description	Manufacturer Part Number	SMD Number	Device Type
Multiplexers 4-input dual	UT54ACS153	5962-96550	01
	UT54ACTS153	5962-96551	01
	UT54ACTS153E*	5962-96551	02, 03
Multiplexers quadruple 2 to 1	UT54ACS157	5962-96552	01
	UT54ACTS157	5962-96553	01
	UT54ACTS157E*	5962-96553	02, 03
Counters 4-bit synchronous	UT54ACS163	5962-96554	01
	UT54ACTS163	5962-96555	01
Registers 8-bit shift	UT54ACS164	5962-96556	01
	UT54ACS164E*	5962-96556	02, 03
	UT54ACTS164	5962-96557	01
	UT54ACTS164E*	5962-96557	02, 03
Registers 8-bit shift parallel	UT54ACS165	5962-96558	01
	UT54ACS165E*	5962-96558	02, 03
	UT54ACTS165	5962-96559	01
Counters 4-bit binary up-down	UT54ACS169	5962-96560	01
	UT54ACTS169	5962-96561	01
Counters up-down BCD synchronous 4-bit	UT54ACS190	5962-96562	01
	UT54ACTS190	5962-96563	01
Counters up-down binary synchronous 4-bit	UT54ACS191	5962-96564	01
	UT54ACS191E*	5962-96564	02, 03
	UT54ACTS191	5962-96565	01
Clocks up-down synchronous 4-bit	UT54ACS193	5962-96566	01
	UT54ACS193E*	5962-96566	02, 03
	UT54ACTS193	5962-96567	01
Clock and wait-state generation circuit	UT54ACTS220	5962-96753	01
Buffers octal with inverted 3-state outputs	UT54ACS240	5962-96568	01
	UT54ACTS240	5962-96569	01

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8-Bit MSI & 16-Bit Logic Products with Unused or Floating Logic Inputs

Logic Function Product Description	Manufacturer Part Number	SMD Number	Device Type
Buffers/line drivers octal with 3-state outputs	UT54ACS244	5962-96570	01
	UT54ACS244E*	5962-96570	02, 03
	UT54ACTS244	5962-96571	01
Transceivers octal bus with 3-state outputs	UT54ACS245	5962-96572	01
	UT54ACTS245	5962-96573	01
	UT54ACTS245E*	5962-96573	02, 03
Transceivers octal bus Schmitt trigger with 3-state outputs	UT54ACS245S	5962-96572	02
Multiplexers 4-input dual with 3-state outputs	UT54ACS253	5962-96574	01
	UT54ACTS253	5962-96575	01
Look-ahead carry generator for counters	UT54ACS264	5962-96576	01
	UT54ACTS264	5962-96577	01
FLIP-FLOPs octal D with clear	UT54ACS273	5962-96578	01
	UT54ACS273E*	5962-96578	02, 03
	UT54ACTS273	5962-96579	01
Latches quadruple S-R	UT54ACS279	5962-96580	01
	UT54ACTS279	5962-96581	01
9-bit parity generators/checkers	UT54ACS280	5962-96582	01
	UT54ACTS280	5962-96583	01
Adders 4-bit parity binary full	UT54ACS283	5962-96584	01
	UT54ACS283E*	5962-96584	02, 03
	UT54ACTS283	5962-96585	01
Registers universal shift/storage	UT54ACS299E*	5962-06238	02, 03
Buffers/line drivers hex with 3-state outputs	UT54ACS365	5962-96586	01
	UT54ACTS365	5962-96587	01
Latches octal transparent with 3-state outputs	UT54ACS373	5962-96588	01
	UT54ACTS373	5962-96589	01
FLIP-FLOPS octal D with 3-state outputs	UT54ACS374	5962-96590	01
	UT54ACTS374	5962-96591	01

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8-Bit MSI & 16-Bit Logic Products with Unused or Floating Logic Inputs

Logic Function Product Description	Manufacturer Part Number	SMD Number	Device Type
Octal Buffers and Line Drivers with inverted 3-state outputs	UT54ACS540	5962-96592	01
	UT54ACTS540	5962-96593	01
Octal Buffers and Line Drivers with 3-state outputs	UT54ACS541	5962-96594	01
	UT54ACTS541	5962-96595	01
	UT54ACTS541E*	5962-96595	02, 03
EDACs	UT54ACS630	5962-06239	01
Transceivers latchable with >parity generator/checker	UT54ACS899	5962-06240	01
Logic dual 4-input NOR gates	UT54ACS4002	5962-96596	01
	UT54ACTS4002	5962-96597	01

*3.0V to 5.0V Supply Range

Table 2: Cross Reference of Applicable Products, 16-bit Logic

Logic Function Product Description	Manufacturer Part Number	SMD Number	Device Type
16-bit Buffer/Line Driver, TTL Inputs and Three-State Quiet Outputs	UT54ACTQ16244	5962-06243	01
16-bit Bidirectional Transceiver, TTL Inputs, and Three-State Quiet Outputs	UT54ACTQ16245	5962-06244	01
16-bit D Flip-Flop TTL Inputs, and Three-State Quiet Outputs	UT54ACTQ16374	5962-06245	01
Schmitt CMOS 16-bit Bidirectional MultiPurpose Registered Transceiver, with cold/warm spare	UT54ACS164646S	5962-06234	01
Schmitt CMOS 16-bit Bidirectional MultiPurpose Low Voltage Transceiver, with cold/warm spare	UT54ACS162245SLV	5962-02543	01
16-bit Bidirectional MultiPurpose Transceiver with cold spare	UT54ACS164245S/SE	5962-98580	01, 02, 03, 04, 05
16-bit Bidirectional MultiPurpose Transceiver with cold/warm spare	UT54ACS164245SEI	5962-98580	06, 07

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8-Bit MSI & 16-Bit Logic Products with Unused or Floating Logic Inputs

1.0 Overview

To avoid system-level problems in designs that use 8-b and 16-b logic devices, it is important that unused or floating CMOS, or TTL inputs and bi-directional signals are properly managed. Since CMOS inputs are inherently high impedance (high-Z), when inputs are left unconnected, or otherwise not properly driven, the voltage potential at the input can float to most any value between V_{SS} and V_{DD}. This is because the floating input is effectively an isolated capacitor with one terminal unconnected, and so it can easily pick up noise or stray charges. See Figure 1. Ensuring that unused inputs and bi-directional signals are properly managed will reduce the chances of current and future system malfunction or failure.

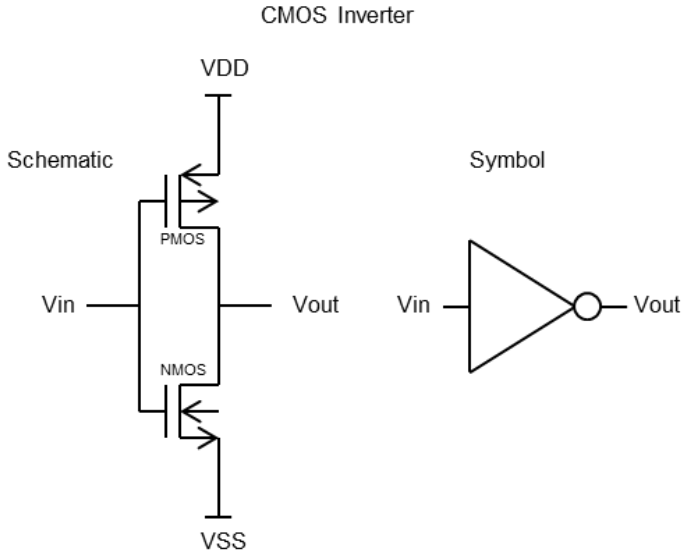

Figure 1: CMOS Inverter: Schematic and Symbol

There are two common conditions that occur in practice and that can lead to floating inputs for Cobham 16-b or 8-b MSI CMOS Logic products. The first case can arise when some logic inputs are not needed, or unused during logic design. The second results from a high impedance (High-Z) logic state of the driving circuit or bus connected to the 16-b or 8-b MSI CMOS logic input. A Tri-State output driver or data bus connection to the input is an example of this condition.

Since CMOS inputs are High-Z, any condition where the logic input is not driven to either a logic HI or logic LO state can result in indeterminate logic levels. The results of this condition are: 1) Undesired or anomalous output behavior, such as unknown logic state, or oscillation and 2) High current consumption can result if the input logic level is at or near the mid-point of the input voltage range, or between LO and HI logic levels. This is the region of maximum switching current (IDDQ) for CMOS logic circuits. The Vout vs. Vin and IDDQ vs. Vin transfer curves for a CMOS inverter are shown in Figure 2.

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8-Bit MSI & 16-Bit Logic Products with Unused or Floating Logic Inputs

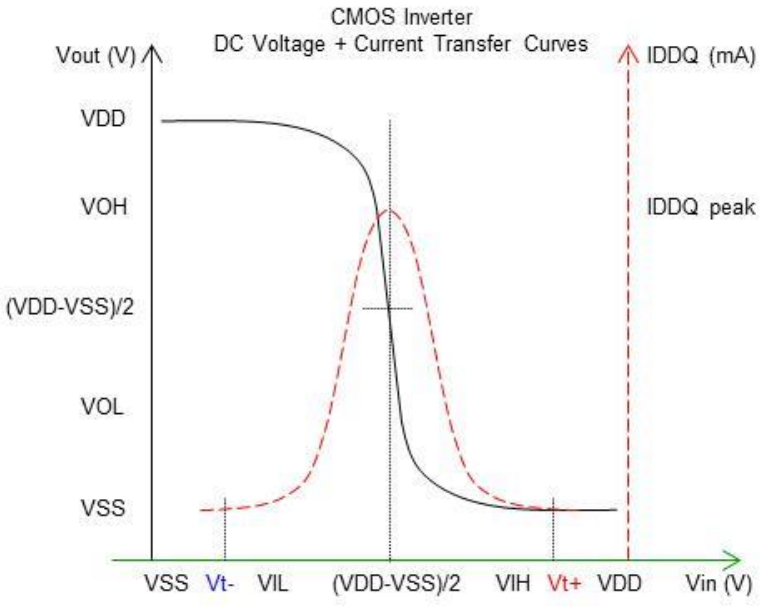

Figure 2: CMOS Inverter: DC Voltage + Current Transfer Curves

The question then arises as to what to do with these unused, High-Z, or otherwise floating logic inputs. This Application Note will briefly describe the methods and techniques recommended by Cobham to mitigate potential problems due to floating inputs for Cobham 8-b MSI and 16-b Logic products.

2.0 Technical Background

Cobham 8-b and 16-b logic devices include both CMOS and TTL input/output (I/O) types. If the device name includes "ACS" in the part name, then the device has CMOS I/O logic buffers and operates with CMOS logic levels. If the device name includes "ACT" in the part name, then the device has TTL I/O buffers and operates with TTL logic levels. This is noted because the input voltage levels (VIL, VIH) can be different between the two I/O logic standards and there can also be minor differences in the response to noise or the floating level of the unused input between parts based on these two standards. The focus of the Application Note will be on CMOS devices, but the findings, methods, and recommendations are also directly applicable to TTL circuits as well. Some of Cobham's 8-b and 16-b logic devices also include Schmitt Trigger inputs. These are provided for applications requiring additional noise immunity and tolerance for slow input rise and fall times (tr, tf). Additional details of Schmitt Trigger inputs are provided below in Section 3.0.

In some cases in application, not all gates or inputs of digital logic devices are used. For example, there may be a configuration where only two inputs of a three input AND gate are used. When this situation occurs, the unused inputs should not be left unconnected because the indeterminate voltages at the external connections will result in undefined operational states. This is a general practice that must be observed for digital logic design under all circumstances.

All unused inputs of digital logic devices must be connected to a logic LO or HI voltage level to prevent them from floating. The logic level (LO or HI) that should be applied to the particular unused input depends on the function of the device. CMOS inputs are High-Z and so even the smallest change in voltage or charge on the open input can result in undesired logic levels. A small change in the charge at the unconnected input, as caused by proximity to another charged object (triboelectric effect), for example, can dramatically change the voltage and logic state of the input buffer and so too the logic output. Additionally, and for the same reasons, unconnected inputs may be influenced by noise, either radiated, or coupled from nearby traces or circuit devices. As a result of this coupled voltage, the behavior at the output of the logic circuit can no longer be predicted for unconnected inputs.

8-Bit MSI & 16-Bit Logic Products with Unused or Floating Logic Inputs

2.1 Definition of Threshold Voltages

The threshold voltage definitions for standard CMOS inputs and Schmitt Trigger inputs are given here and in Figure2 and Figures 3a, 3b.

- Vt+/Vt- are the threshold voltages for standard CMOS input buffers, which are determined by the properties of the P and N MOSFET devices in an inverter, or logic element, and as defined in Figure 2.
- VT+/VT- are the threshold voltages for CMOS Schmitt Trigger input buffers, which determine the hysteresis properties of the buffer, and as defined in Figures 3, 4.

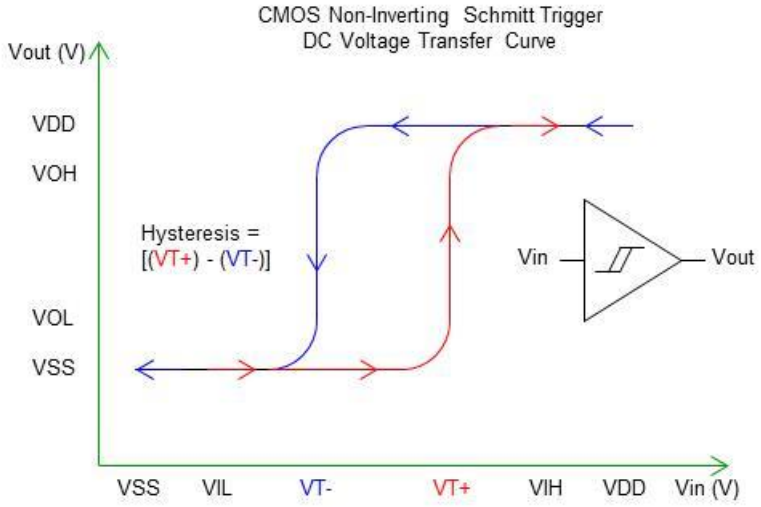

Figure 3: CMOS Non-Inverting Schmitt Trigger DC Voltage Transfer Curve

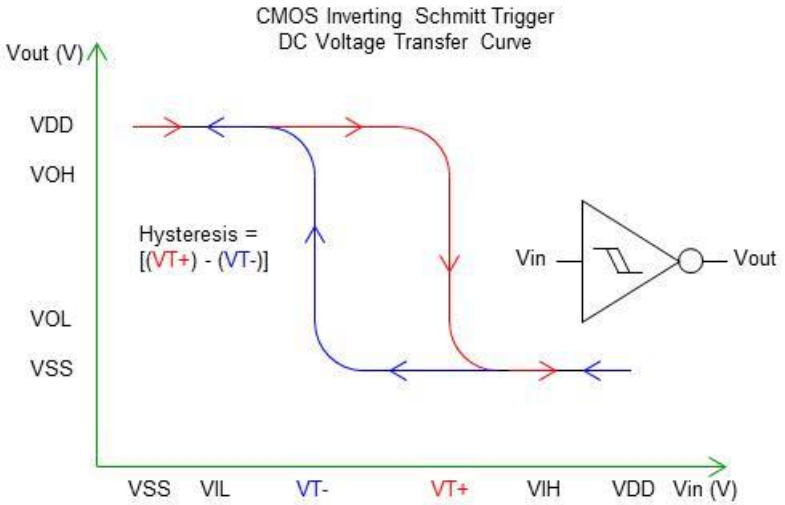

Figure 4: CMOS Inverting Schmitt Trigger DC Voltage Transfer Curve

8-Bit MSI & 16-Bit Logic Products with Unused or Floating Logic Inputs

3.0 Unused or Floating Logic Inputs

The question often arises in practical application of 8-b MSI and 16-b Logic products as to whether or not floating inputs are allowed in circuit design. Owing to the High-Z nature of CMOS logic gate inputs, as described previously in Sections 1.0 and 2.0, above, some considerations of floating inputs are presented here as general design practices.

A floating input can be most any voltage value. This is quasi-Analog operation where a continuous range of voltages is allowed. Digital logic, however, is binary valued (i.e. logic LO (0) or logic HI (1) by definition. These two types of signals (i.e. Analog/Digital) are not directly compatible without ADC/DAC conversion.

This consideration applies to both standard CMOS inputs as well as Schmitt Trigger inputs. Schmitt Trigger inputs include hysteresis for improved noise immunity and a greater tolerance to slow input rise and fall times (tr, tf), but are otherwise functionally equivalent to standard CMOS inputs. Hysteresis enables a Schmitt Trigger input to switch at different trigger voltages (VT+, VT-) for a HI to LO transition vs. a LO to HI transition. The difference between VT+ and VT- is the hysteresis voltage, as shown in Figures 3 and 4.

Figure 3. General "best practices" for digital design dictates that all I/O signals are maintained at known logic values. Pull-up and pull-down resistors are frequently used for this purpose. Since the CMOS logic inputs are High-Z, and do not require current to set the input voltage, these pull-up/pull-down resistors can be high-valued (e.g. ~100kΩ), resulting in a weak pull-up/pull-down action. This is all that is necessary. After the initial charge adjustment, no DC current is required.

Figure 4. Space applications of electronics result in exposure to charging of unconnected signals, metal surfaces and traces, etc. Without a sufficiently low impedance discharge path, this charging effect can be significant due to various space radiation and electric fields. Device charging can result in ESD damage if there is an uncontrolled discharge event. Including pull-up/pull-down resistors (e.g. ~100kΩ) would mitigate charging on the (un-driven) input nodes by draining off any static change in a slow and controlled manner.

The following three cases are circuit operating modes to consider for "floating" inputs.

1. In the best case situation, the 'floating input' voltage potential is well below Vt- or well above Vt+ and there is little or no noise on the floating logic gate input pin. In this case the output remains stable.
2. In the intermediate case, input voltage potential is between Vt- and Vt+ and there is little or no noise at the floating input. In this case with the input voltage at approximately (VDD-VSS)/2, the input buffer now dissipates high DC current (IDDQ), which is normally only flowing during high-speed switching transients. This current dissipates excess power and may damage the logic circuits over time. See Figure 2 for DC voltage and current transfer curves for a CMOS inverter.

As is seen from the curves in Figure 3, if the inverter input voltage is held at an indeterminate value (i.e. between VIL and VIH), then the output voltage will also be indeterminate in accordance with the Vout-Vin relationship of the inverter's transfer curve. This condition not only results in very high static IDDQ current, but the indeterminate inverter output voltage will also propagate to the next stage logic gate operation, resulting in similar anomalous operation for the downstream electronics.

This high current and indeterminate output conditions apply equally to both standard CMOS inputs and Schmitt Trigger inputs, since both types of inputs have similar DC voltage transfer curves and are based on the CMOS inverter circuit. This means that both device types can experience high IDDQ current when inputs are near (VDD-VSS)/2. The peak IDDQ current for a Schmitt Trigger input will be at a different input voltage value than for a standard CMOS input. This is due to the differences between Vt+/Vt- threshold voltages for the standard CMOS inputs (see Figure 2) and VT+/VT- Schmitt Trigger threshold voltages (see Figures 3, 4). The peak IDDQ current will, however, still occur close to the midpoint of the VDD power supply voltage as in the case of the standard CMOS inverter circuit.

8-Bit MSI & 16-Bit Logic Products with Unused or Floating Logic Inputs

3. In the worst-case situation, the floating input voltage potential is between Vt- and Vt+, and with enough noise to cross both thresholds causing not only high DC switching current, but also an output signal that bounces around between logic LO, logic HI, and indeterminate logic states (i.e. above VOL max., but below VOH min.). One generally applies "worst-case" analysis for Hi-Rel applications, since the condition can happen, and would result in the poorest outcome.

If the Designer wants a guarantee that the outputs won't bounce around, then they must add pull-ups or pull-downs to the unused, or otherwise floating input pins so that they will always be in a known (determinate) state. A large value resistor (~100kΩ), providing a weak pull-up/down mechanism is sufficient.

Another possible solution for situations where a single floating logic gate arises is to connect the unused logic input directly to one of the other logic inputs of the same logic gate that is in use. For standard Boolean logic gates, the logic function of the device is unaffected. This circuit arrangement can be used equally well with AND (NAND) or OR (NOR) gates. However, this configuration would result in a 2x increase in load capacitance for the driving circuit since it is now driving two logic inputs. Analysis or simulation would be required to determine if switching speed is still acceptable or not.

4.0 Summary and Conclusion

When using Cobham's 8-b and 16-b Logic products, the following two general recommendations apply for reliable and deterministic operation: 1) No inputs are left floating or otherwise unconnected, and 2) Resistive pull-ups or pull-downs are connected to those input signal pins that are not physically connected (floating), or can be driven by a Tri-State signal, so that they will always be in a known, or determinate state. In this way, the voltage on the outputs won't bounce around indeterminately, or causing device static power supply current (IDDQ) to exceed specified (low) limits. A large value resistor (~100kΩ) provides a weak pull-up/pull-down function, and is sufficient for this purpose.

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