APPLICATION NOTE

RELEASED 12/7/17

Cold and Warm Spare Functionality of the 16-Bit Transceiver Product Family

Table 1: Cross Reference of Applicable Products

Product Name CMOS 16-bit Bi-Directional Multi-Purpose Transceivers With Schmitt Trigger Buffered Inputs	Manufacturer Part Number (UT54ACS)	SMD # (5962-)	Device Type	Internal PIC* #
Low Voltage Transceiver **2.5V/3.3V** Voltage Level Translation Cold Spare-All Inputs & Outputs **Warm Spare**-All Outputs	162245**SLV**	02543	01	WA04 WA05
Transceiver **3.3V/5.0V** Voltage Level Translation Cold Spare-All Inputs & Outputs	164245**S/SE**	98580	01, 02, 03, 04, 05	JM03 JM04 JM06
Transceiver **3.3V/5.0V** Voltage Level Translation Cold Spare-All Inputs & Outputs **Warm Spare**-All Outputs	164245**SEI**	98580	06, 07	JM06
Registered Transceiver **3.3V/5.0V** Voltage Level Translation Cold Spare-All Inputs & Outputs **Warm Spare**-All Outputs	164646**S**	06234	06, 07	KE01

*PIC = Product Identification Code

1.0 Overview

The CAES 16-bit Multi-Purpose transceivers contain cold and warm sparing buffers. These devices are ideal for applications requiring redundant components which remain in a power-off state until needed. This allows a redundant subsystem to be connected to the host system while being electrically isolated from it.

Redundancy of mission critical subsystems is a common practice used to ensure reliable operation of a spacecraft or satellite, for example. When in Cold or Warm Spare Modes, the devices listed above in **Table 1** will maintain a high impedance state on all of the bi-directional I/O signals even when connected to an active address or data bus.

2.0 Technical Background

All of the transceiver devices listed in **Table 1** support voltage translation. Please see device-specific datasheet or SMD for details. Voltage translation requires two different power supply voltages. VDD1 (VDDB) supports data port B, and VDD2 (VDDA) supports data port A. **Figure 1** is a notional block diagram for the UT54ACS162245SLV, UT54ACS164245S/SE, and UT54ACS164245SEI devices. **Figure 2** is a notional block diagram for the UT54ACS164646S device.

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These 16-bit transceiver products contain two separate 8-bit transceivers, which can be operated either as a combined single 16-bit device, or as two independent 8-bit data bus buffers or translators. However, both must always be powered up or powered down together as a single 16-bit transceiver. For the UT54ACS164245-series products, for example, VDD1 (Port B) pins 7 and 18 don't correspond directly to Port B I/O 1B1-1B8 and 2B1-2B8 signals, respectively. Pins 7 and 18 power "quiet" internal logic and "noisy" I/O switching sections of the IC that operate independently, but must always be connected together via low impedance connections and always at the same VDD1 potential. VDD2 (Port A) pins 31 and 42 must similarly always be connected together as well. Do not place any circuit components between pins 7, 18 or pins 31, 42, respectively. This can result in different voltages between different parts of the IC, where instead the same voltage is required at these respective VDD1,2 pins for correct operation.

We recommend using generally accepted power and ground plane design practices, including low inductance PCB layout and low DC impedance connections to all VDD1, VDD2, VSS pins. Do not place resistors, diodes, or other components in series with power/ground pins, unless as part of an upstream power supply filtering network (VDD1, VDD2 egress to PCB), or clamping network for Redundancy/Cold Spare Mode switching. Example components that may be used in a power supply filter include ferrites, inductors, and low value (e.g. 10Ω) resistors. Low on resistance MOSFET switches can be used for clamping VDD1 and VDD2 to VSS during Cold Spare Mode. The UT54ACS164245S/SE has special power sequencing requirements. Please see the respective product datasheet for details.

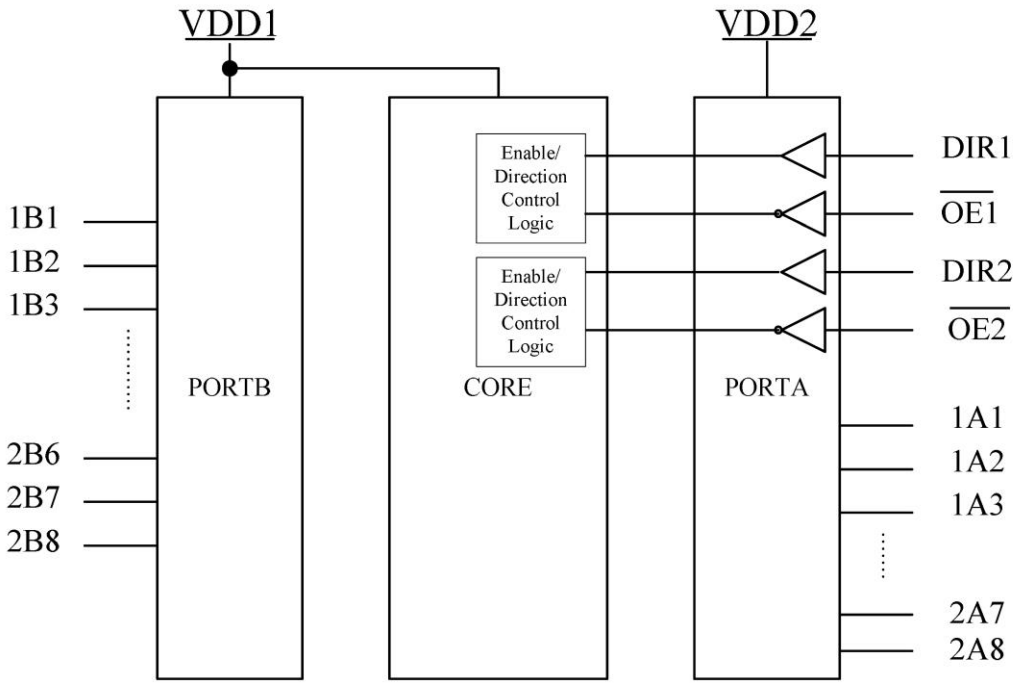

Figure 1. Notional block diagram for UT54ACS162245SLV, UT54ACS164245S/SE, and UT54ACS164245SEI

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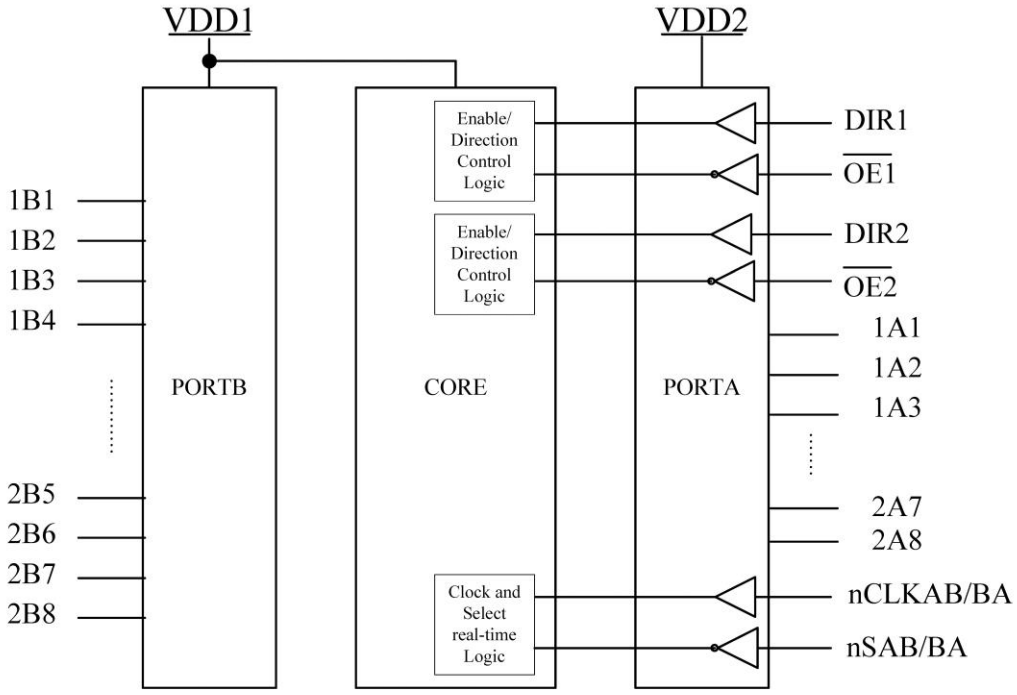

Figure 2. Notional block diagram for UT54ACS164646S

Table 2: 16-bit Transceiver Cold/Warm Spare Capability

CAES Part Number	Cold Spare Function	Warm Spare Function
UT54ACS162245**SLV**	x	x
UT54ACS164245**S/SE**	x	
UT54ACS164245**SEI**	x	x
UT54ACS164646**S**	x	x

16-bit signal states for Cold and Warm Spare modes are briefly summarized here and in **Table 3**.

- Cold Spare Mode (VDD1 = VDD2 = VSS ± 250mV): All bi-directional I/O and control signals are in a high impedance state. See **Table 3**.
- Warm Spare Mode (VDD1 or VDD2 = VSS ± 250mV): The side of the device that has VDD powered on will have the bi-directional signals "actively" tri-stated, because the devices internal output enable (OE) signals are forced to a logic low. The input control signals are active, but high impedance. The side of the device that has VDD powered off will have the bi-directional signals "passively" tri-stated by the cold spare circuitry. The input control signals on the powered off side of the device are inactive and high impedance. See **Table 3**.

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Table 3: 16-bit Transceiver Signal States during Cold/Warm Spare Modes

Sparing Mode	Dual Power Supplies	Bi-Directional I/O		Control Signals
	VDDx	1A1-8, 2A1-8 (Port A/VDD2)	1B1-8, 2B1-8 (Port B/VDD1)	DIRx, /OEx (Port A/VDD2)
Cold Spare (All Devices)	VDD1,2=VSS±0.25V	Passive High-Z	Passive High-Z	Inactive/High-Z
Warm Spare (Table 2)	VDD1=VSS±0.25V VDD2=Operating[1]	Active High-Z	Passive High-Z	Active/High-Z
	VDD1=Operating[1] VDD2=VSS±0.25V	Passive High-Z	Active High-Z	Inactive/High-Z

Notes:
1) VDDx per Power Supply Recommended Operating Conditions. See the respective Data Sheet or SMD document.

3.0 Cold Spare Operation

In applications requiring high reliability, cold sparing enables the designer to tie a redundant device to the data bus with its power supply within ±250mV of VSS. This device can be kept in cold spare mode and powered only when necessary. Activating a cold spared device only when needed allows the system to save power. For an unpowered redundant device to be connected to an active bus, the cold spare device must present a high impedance of approximately 1MΩ in order to avoid adding an unnecessary load to the bus.

The ~1MΩ impedance of the I/O lines for a device in Cold Spare Mode (VDD1, 2 = VSS±250mV) does not add significant loading to the active bus, thus interfering very little with the signal. The ESD structure on a cold spare device is said to be non-typical. CAES 16-Bit Logic products contain proprietary cold-spare input and output buffers. Schematics for these circuits are not available. However, the equivalent circuit behaves like back-to-back diodes, as shown in **Figure 3**.

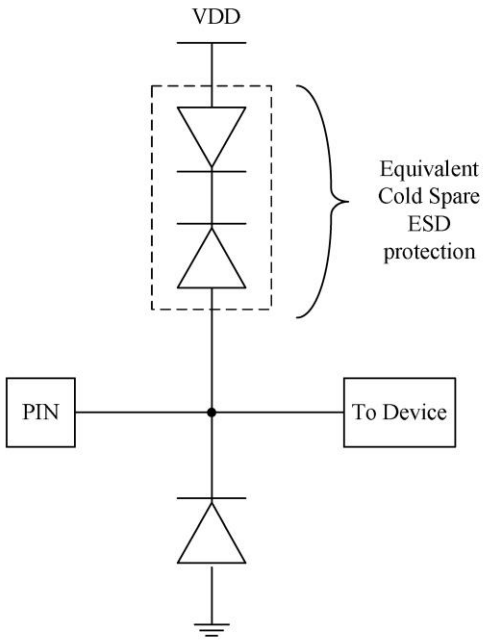

Figure 3. Notional Cold/Warm Spare ESD protection circuit

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3.1 Cold Spare – Implementation

This section provides an example of VDD1, VDD2 connections for Cold Spare Mode.

Each 16-b transceiver part is composed of two 8-bit transceivers (1, 2), which can be operated as two independent 8-bit data bus buffers or translators. However, they both must be powered up or down together as a single 16-bit transceiver. *For the UT54ACS164245-series products, for example, VDD1 pins 7 and 18 and VDD2 pins 31 and 42, respectively, must always be connected together.* This means that the two 8-bit transceivers: 1) 1A1-8/1B1-8 and 2) 2A1-8/2B1-8 cannot be placed in either Cold Spare Mode, or in Normal Operating Mode independently of one another. Cold Spare Mode, or Normal Operating Mode, applies to the entire 16-bit transceiver in all cases. VDD1 and VDD2 must both be set to VSS ± 250mV when enabling Cold Spare Mode. *Neither VDD1, nor VDD2 can be "Floating" or "No-Connect" in Cold Spare Mode.* Both power supplies must be connected to VSS. A low impedance clamp circuit is recommended for implementation. The clamp may be a CMOSFET or other low ON resistance device.

Figure 4 shows an example of VDD1 and VDD2 connections during Cold Spare Mode for the UT54ACS164245S/SE 16-bit transceiver. In this example, single pole, double throw (SPDT) switches are used to toggle between Normal Operating and Cold Spare Modes. Other power supply switching options can be considered, provided VDD1 and VDD2 are clamped to VSS, and not Floating or No-Connect.

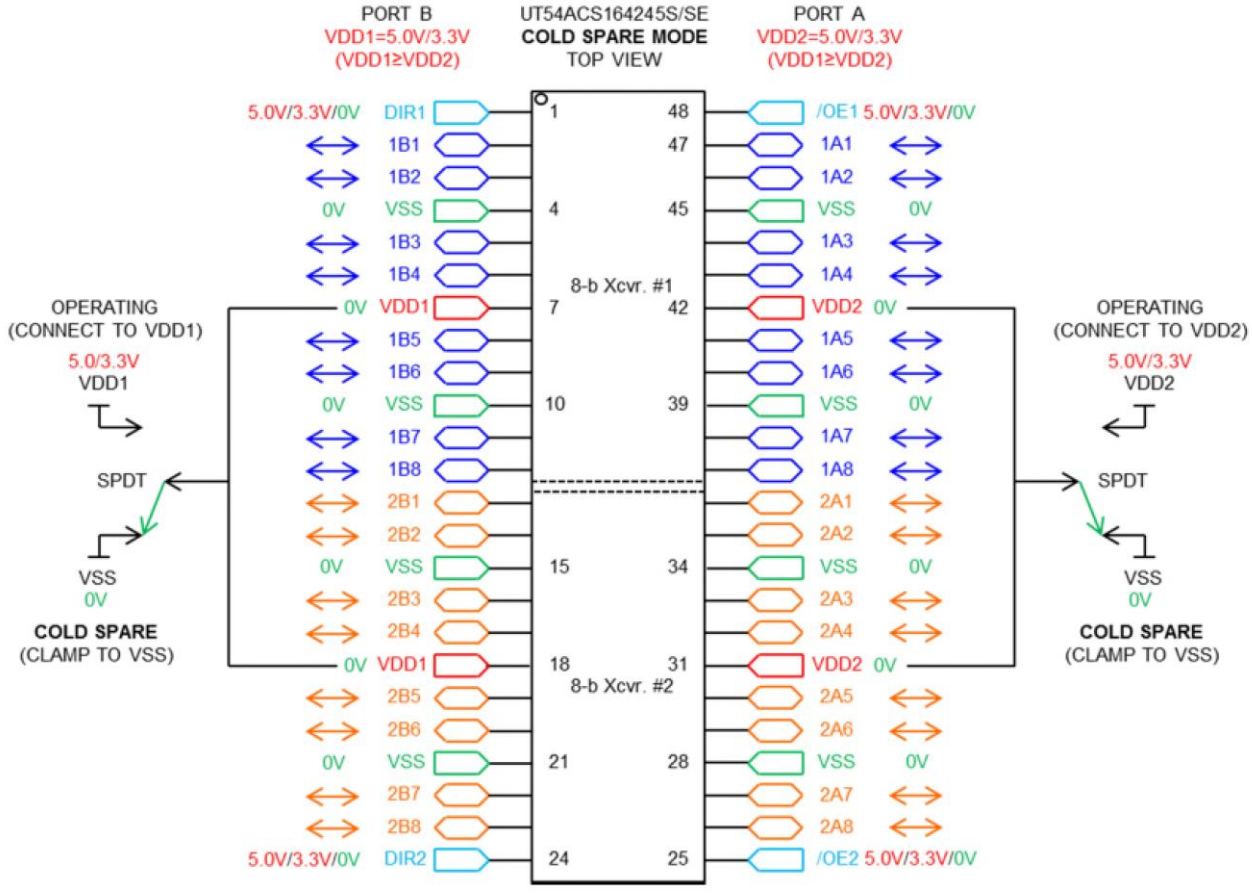

Figure 4. Example UT54ACS164245S/SE VDD1, VDD2 Connections for Cold Spare Mode

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3.2 Consequences of "Floating" or "No-Connect" VDD1, VDD2 during Cold Spare Mode

Floating, or No-Connect VDD1 and/or VDD2 during Cold Spare Mode can allow "sneak" electrical paths from bi-directional I/O pins to VDD1 or VDD2 internal IC power busses via I/O pin ESD protection and Cold Spare circuitry. For a redundant device in Cold Spare Mode, the I/O pins are still connected to the active address or data bus and can have VDD1 or VDD2 voltage applied continuously. A Floating or No-Connect VDD1 and/or VDD2 enables VDD1 or VDD2 to be partially powered up to some intermediate voltage between VSS and VDD1 or VDD2. This intermediate voltage can be greater than (VSS + 250mV) as specified for correct Cold Spare Mode operation. If either VDD1 or VDD2 are greater than (VSS + 250mV), then I/O pins can become low impedance, allowing currents to flow into the I/O pins and to the device VDD1 or VDD2 power busses. This condition is counter to the normal high impedance state of the I/O pins during Cold Spare Mode. The magnitude of these pin currents depends on the voltage applied to the I/O pin and the actual induced VDD1 or VDD2 voltage in a complex way. These currents can potentially exceed electromigration (EM) design limits for the device's internal metallization traces. This in turn can reduce device reliability and lifetime as well as result in additional, but unintended system power dissipation. Needless to say, these parasitic or "sneak" path currents must be avoided.

4.0 Warm Spare Operation

All 16-bit transceiver devices, with the exception of the UT54ACS164245S/SE, support Warm Spare Mode operation. Warm Spare Mode is initiated when one power supply (either VDD1 or VDD2) is set to the normal operating voltage, and the other power supply is set to VSS ± 250mV. *When the device is "warm spared", the bi-directional I/O signals on the side that has VDD set to the operational supply value is "actively" tri-stated, because the devices internal output enable (OE) signals are forced to a logic low. The bidirectional I/O signals on the side of the device that has VDD set to VSS (0V) is "passively" tri-stated by the cold spare circuitry.* All of the recommendations under Section 3.0, Cold Sparing, apply to Warm Spare Mode as well.

5.0 Summary and Conclusion

The CAES 16-Bit transceiver products provide asynchronous, bi-directional communication, signal buffering, and voltage translation functions. They are useful in facilitating high-reliability systems design by providing electrical isolation to a redundant powered-down subsystem without a power penalty in Cold Spare Mode. The Warm Spare function is also provided by these 16-b Transceiver products, with the exception of the UT54ACS164245S/SE devices.

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Appendix A

1) CAES, "UT54ACS164646 16-bit Multi-Purpose Registered Transceiver Datasheet", Colorado Springs, Colorado
2) CAES, "UT54ACS162245SLV 16-bit Multi-Purpose Transceiver – 3 Volt Datasheet", Colorado Springs, Colorado
3) CAES, "UT54ACS164245S/SE 16-bit Multi-Purpose Transceiver – 5 Volt with Cold Spare Datasheet", Colorado Springs, Colorado
4) CAES, "UT54ACS164245SEI 16-bit Multi-Purpose Transceiver – 5 Volt with Cold/Warm Spare Datasheet", Colorado Springs, Colorado

Revision History

Date	Rev. #	Author	Change Description
11/29/2017	2.0.0	BRM	Revision for additional Cold/Warm Spare Description + formatting.
12/07/2017	2.1.0	BRM	Removed version number from footer; new formatting requirement.