Certus™-NX-RT and CertusPro™-NX-RT FPGAs

UT24C407 and UT24CP1008

Frontgrade introduces radiation tolerant (RT) versions of low-power, general purpose FPGAs based on the Lattice Semiconductor Certus™-NX and CertusPro™-NX families. Frontgrade's 40k logic cell Certus™-NX-RT and 100k logic cell CertusPro™-NX-RT are built on the Lattice Nexus™ FPGA platform, using low-power 28 nm FD-SOI technology. They offer the extreme flexibility of an FPGA combined with low power, high-reliability (due to extremely low SER), and strong radiation environment resiliency afforded by FD-SOI technology. Design security features such as AES-256 encryption and ECDSA authentication are also supported. The products are provided in small form-factor, low mass, plastic encapsulated packages with 0.8mm tin-lead (Sn63Pb37) solder ball-grid arrays.

Certus family of FPGAs support a variety of interfaces including PCIe (Gen1, Gen2, and Gen3), Ethernet (up to 10G), SLVS-EC, CoaXPress, eDP/DP, LVDS, Generic 8b10b, LVCMOS (0.9–3.3 V), and more. Processing features include up to 100k logic cells, 156 multipliers (18 × 18), 7.3 Mb of embedded memory (consisting of EBR and LRAM blocks), distributed memory and DRAM interfaces (supporting DDR3, DDR3L, LPDDR2, and LPDDR4 up to 1066 Mbps × 64bit data width).

The Certus FPGAs support fast configuration of the reconfigurable SRAM-based logic fabric, ultra-fast configuration of its programmable sysI/O™ and the TransFR™ field upgrade feature. In addition to the high-reliability inherent to FD-SOI technology, active reliability features such as built-in frame-based soft error detection (SED) / soft error correction (SEC) (for SRAM-based logic fabric), and ECC (for EBR and LRAM) are also supported. Dual 1 MSPS 12 bit analog to digital convertors (ADCs) are available on-chip for system monitoring functions and embedded control applications.

Lattice Radiant® design software enables large complex user designs to be efficiently implemented and library support is available for popular logic synthesis tools. Radiant tools use the synthesis tool output along with constraints from its floor planning tools to place and route the user design into the FPGA. The tools extract timing from the routing and back-annotate it into the design for timing verification.

Frontgrade and Lattice provide many pre-engineered intellectual property (IP) building blocks and development tools, including our proven GR-LIB. By using these configurable soft IP cores as standardized blocks, you are free to concentrate on the unique aspects of your design, increasing your productivity.

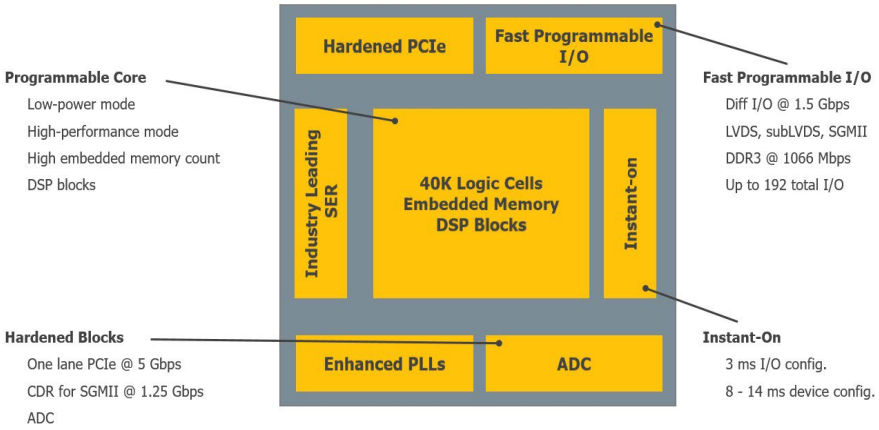

Figure 1. Certus-NX-RT 40K High Level Product Overview

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Product Brief

RELEASED March 2022

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Specifications

	Certus™-NX-RT	CertusPro™-NX-RT
Technology	28nm FDSOI	28nm FDSOI
Logic Cells	39K	96K
Embedded Memory	2.9Mb	7.3Mb
Supply Voltage (V)	1.0 Core, 1.8V Aux	1.0 Core, 1.8V Aux
I/O Voltage (V)	1.0 – 3.3	1.0 – 3.3
PLL	3	4
Primary I/O	LVDS, Soft D-PHY, SGMII, PCIe, GbE	LVDS, Soft D-PHY, SGMII, PCIe, 10GbE
Supported Memory	DDR2/3L, LPDDR2/3 x8, x16	DDR2/3L, LPDDR2/3 x8, x16, x32, x64
Security	Bit stream encryption (AES-256) & authentication (ECDSA)	Bit stream encryption (AES-256 & authentication (ECDSA)
ADC	2x 1 MSPS, 12-bit SAR	2x 1 MSPS, 12-bit SAR
Typical Power (mW)	100	600
Size (mm)	14 x14	19 x19
Temp(^{O}C)	-40 to 125	-40 to 125
Packaging	Plastic package, SnPb balling (x256)	Plastic package, SnPb balling (x484)
TID Target (krad (Si))	100 – 300	100 – 300
SEL Immune Target (MeV-cm^2/mg)	≥80	≥80